PRELIMINARY

Integrated Circuit Systems, Inc.

ICS889834

LOW SKEW, 2-TO-4 LVCMOS/LVTTL-TO-LVPECL/ECL CLOCK MULTIPLEXER

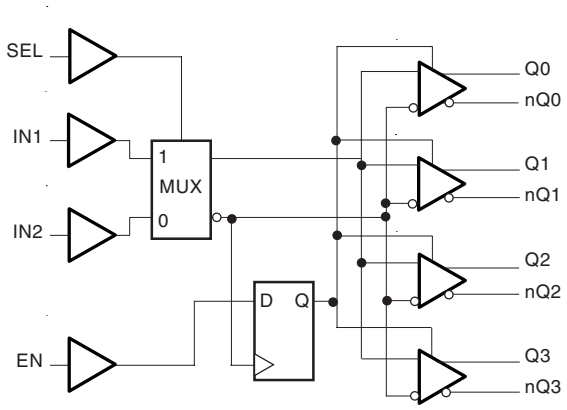
GENERAL DESCRIPTION

The ICS889834 is a high speed 2-to-4 LVCMOS/LVTTL-to-LVPECL/ECL Clock Multiplexer and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS889834 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS889834 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

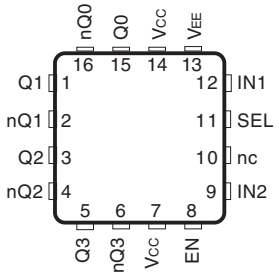
FEATURES

- Four differential LVPECL/ECL outputs
- Two LVCMOS/LVTTL clock inputs
- Output frequency: >1GHz (typical)
- Output skew: TBD
- Part-to-part skew: TBD
- Additive jitter, RMS: <100fs (typical)
- Propagation delay: 420ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.63V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS889834
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q1, nQ1	Output		Differential output pair. LVPECL / ECL interface levels.
3, 4	Q2, nQ2	Output		Differential output pair. LVPECL / ECL interface levels.
5, 6	Q3, nQ3	Output		Differential output pair. LVPECL / ECL interface levels.
7, 14	V_{CC}	Power		Positive supply pins.
8	EN	Input	Pullup	Synchronizing clock enable. When LOW, Q outputs will go LOW and nQ outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{CC}/2V. Includes a 37kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal (IN1, IN2). LVTTL / LVCMOS interface levels.
9	IN2	Input	Pullup	LVCMOS / LVTTL clock input.
10	nc	Unused		No connect.
11	SEL	Input	Pullup	Select input pin. LVCMOS / LVTTL interface levels
12	IN1	Input	Pullup	LVCMOS / LVTTL clock input.
13	V_{EE}	Power		Negative supply pin.
15, 16	Q0, nQ0	Output		Differential output pair. LVPECL / ECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs	
EN	**Selected Source**	**Q0:Q3**	**nQ0:nQ3**
0	IN1, IN2	Disabled; LOW	Disabled; HIGH
1	IN, IN2	Enabled	Enabled

After EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

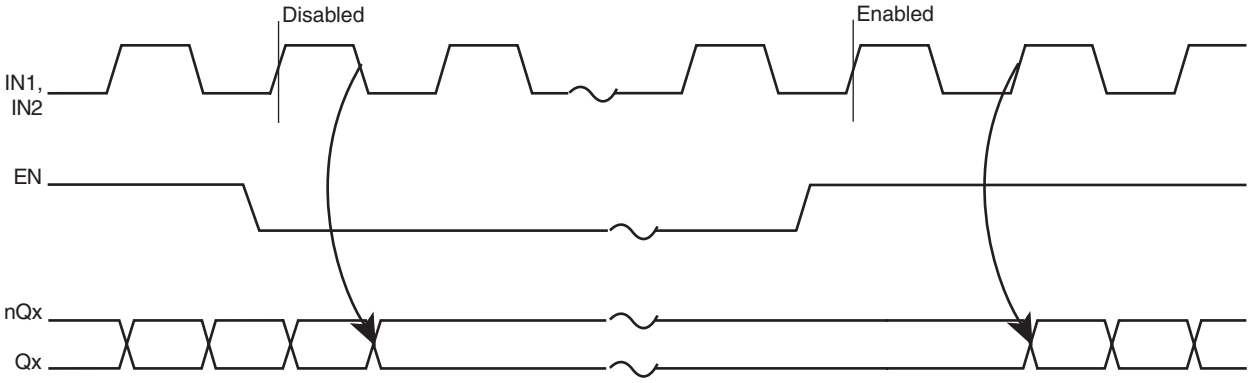


FIGURE 1. EN TIMING DIAGRAM

TABLE 3B. TRUTH TABLE

Inputs				Outputs	
IN1	**IN2**	**EN**	**SEL**	**Q0:Q3**	**nQ0:nQ3**
0	X	1	1	0	1
1	X	1	1	1	0
X	0	1	0	0	1
X	1	1	0	1	0
X	X	0	X	0[1]	0[1]

NOTE 1: On next negative transition of the input signal (IN).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current			45		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 2.5V±5% OR 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IH}	Input High Current		-125		20	µA
I_{IL}	Input Low Current				-300	µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V±5% OR 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.145	V_{CC} - 1.020		V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.945	V_{CC} - 1.820		V
V_{OUT}	Output Voltage Swing		550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1100	1600		mV

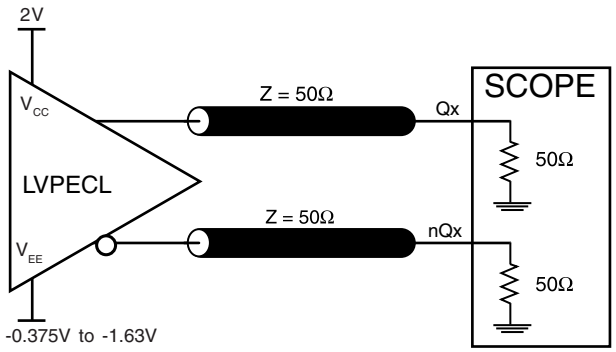
Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 2.5V±5% OR 3.3V±10%, T_A = -40°C TO 85°C

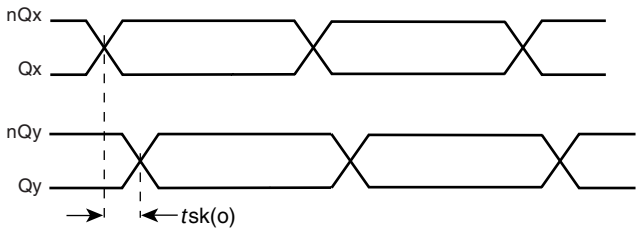
Symbol	Parameter		Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>1.0		GHz
t_{PLH}	Propagation Delay, Low-to-High; NOTE 1				420		ps
t_{PHL}	Propagation Delay, High-to-Low; NOTE 1				420		ps
t_{SW}	Switchover Time	SEL to Q			TBD		ps
*t*sk(o)	Output Skew; NOTE 2, 4				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section				<100		fs
t_R/t_F	Output Rise/Fall Time		20% to 80%		220		ps
t_S	Clock Enable Setup Time	EN to IN1, IN2			TBD		ps
t_H	Clock Enable Hold Time	EN to IN1, IN2			TBD		ps
odc	Output Duty Cycle				50		%

All parameters characterized at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from $V_{CC}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

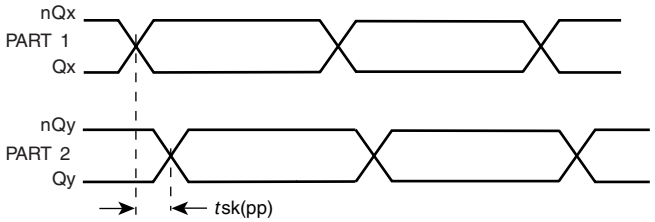
PARAMETER MEASUREMENT INFORMATION



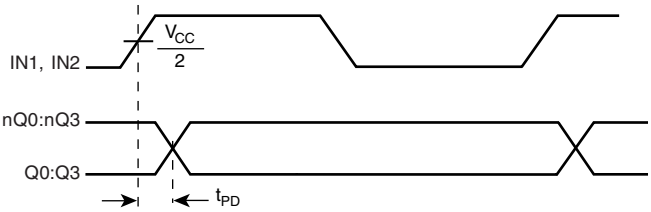
OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

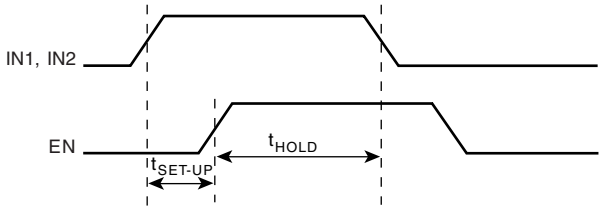


PART-TO-PART SKEW

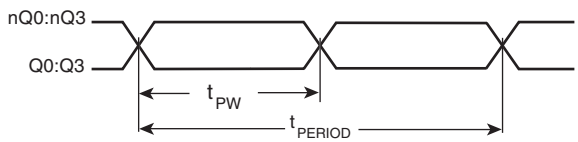


PROPAGATION DELAY

OUTPUT RISE/FALL TIME



SETUP & HOLD TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

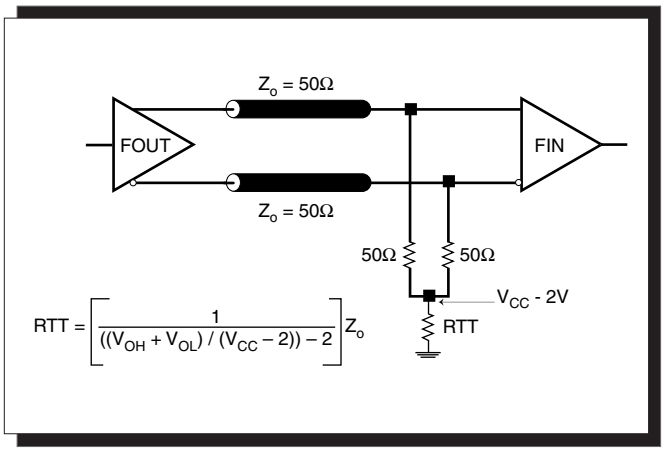


FIGURE 2A. LVPECL OUTPUT TERMINATION

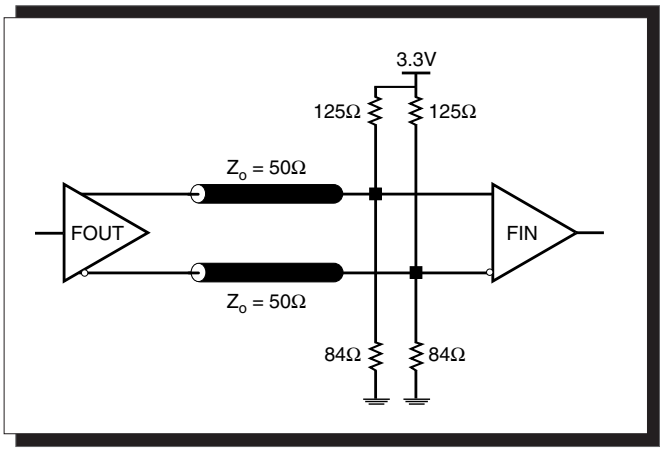


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

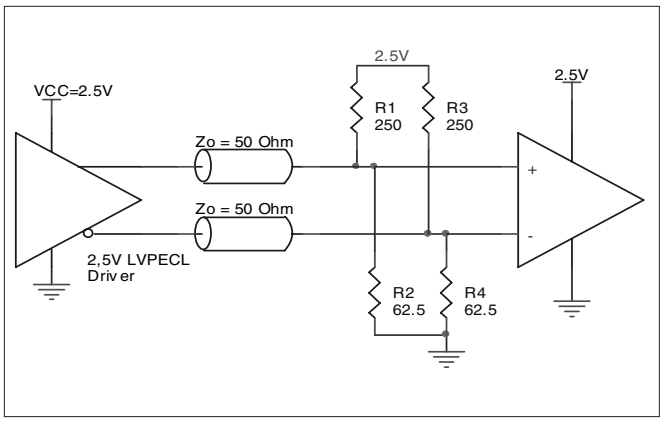


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

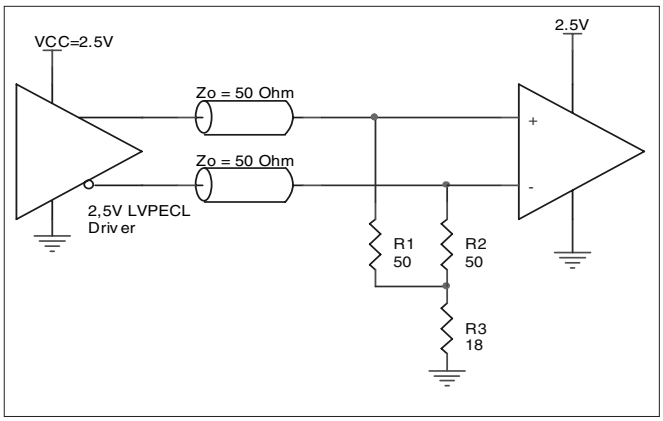


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

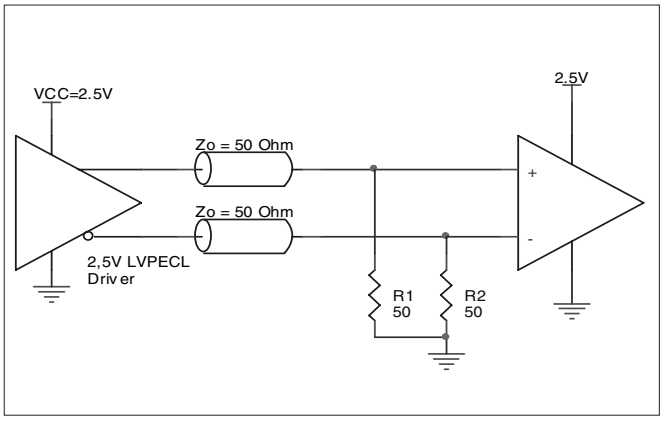


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS889834. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8889834 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.63V * 45mA = **163.4mW**
- Power (outputs)$_{MAX}$ = **27.83mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 27.83mW = **111.3mW**

Total Power$_{_MAX}$ (3.465, with all outputs switching) = 163.4mW + 111.3mW = **274.7mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a 0 air flow and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.275W * 51.5°C/W = 99.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} at 0 Airflow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

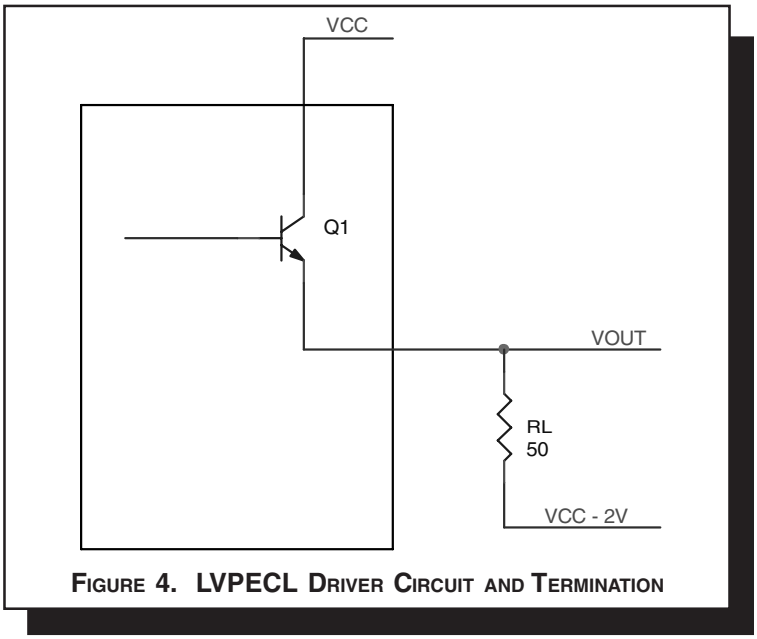


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.005V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.005}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.78V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.78V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1.005V)/50\Omega] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.78V)/50\Omega] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Airflow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS889834 is: 259

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

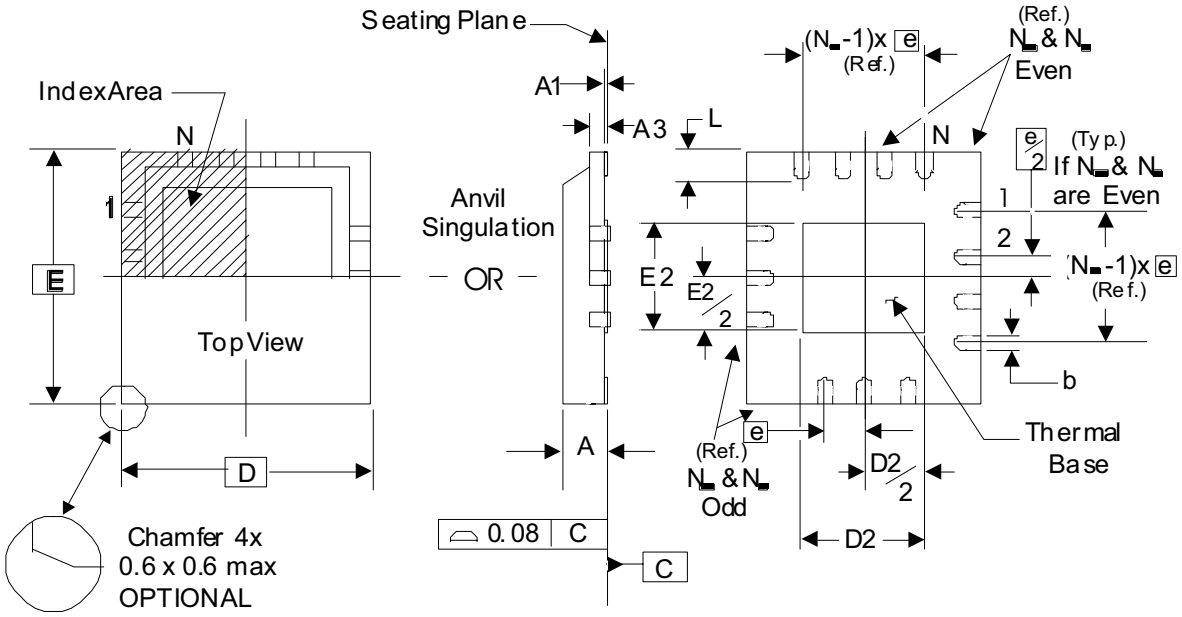


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS889834AK	834A	16 Lead VFQFN	tube	-40°C to 85°C
ICS889834AKT	834A	16 Lead VFQFN	2500 tape & reel	-40°C to 85°C
ICS889834AKLF	TBD	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS889834AKLFT	TBD	16 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.