PRELIMINARY

ICS85354-01

DUAL 2:1/1:2 DIFFERENTIAL-TO-LVPECL/ECL MULTIPLEXER

GENERAL DESCRIPTION

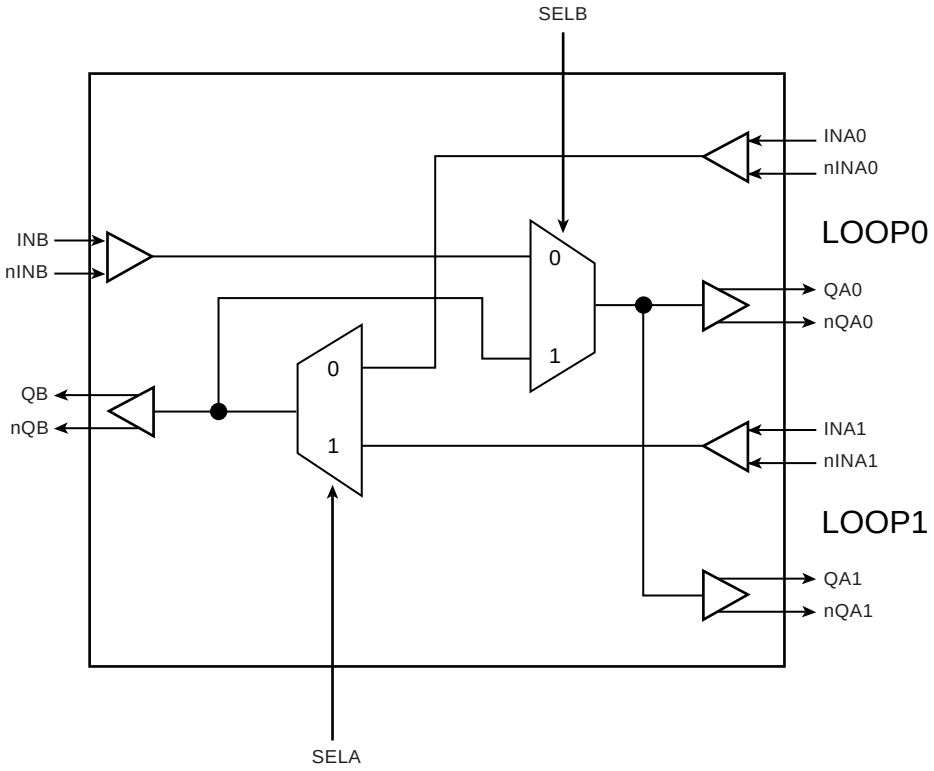
The ICS85354-01 is a 2:1/1:2 Multiplexer and a member of the HiPerClockS™ family of high performance clock solutions from IDT. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device may be useful for multiplexing multi-rate Ethernet Phys which have 100Mbit and 1000Mbit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. A 3rd mode allows loop back testing and allows the output of a phy transmit pair to be routed to the phy input pair. For examples, please refer to the Application Block diagrams on pages 2-3 of the data sheet.

The ICS85354-01 is optimized for applications requiring very high performance and has a maximum operating frequency in 2.5GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

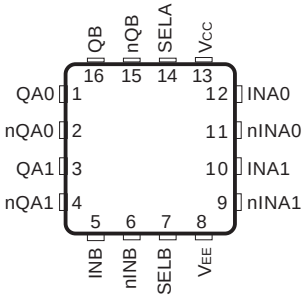
FEATURES

- Dual 2:1/1:2 MUX
- Threee differential LVPECL outputs
- Three differential LVPECL clock inputs
- CLKx pair can accept the following differential input levels: LVPECL, LVDS, CML
- Loopback test mode available
- Maximum output frequency: 2.5GHz
- Part-to-part skew: 85ps (typical)
- Additive jitter, RMS: 0.05ps (typical)
- Propagation delay: 440ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



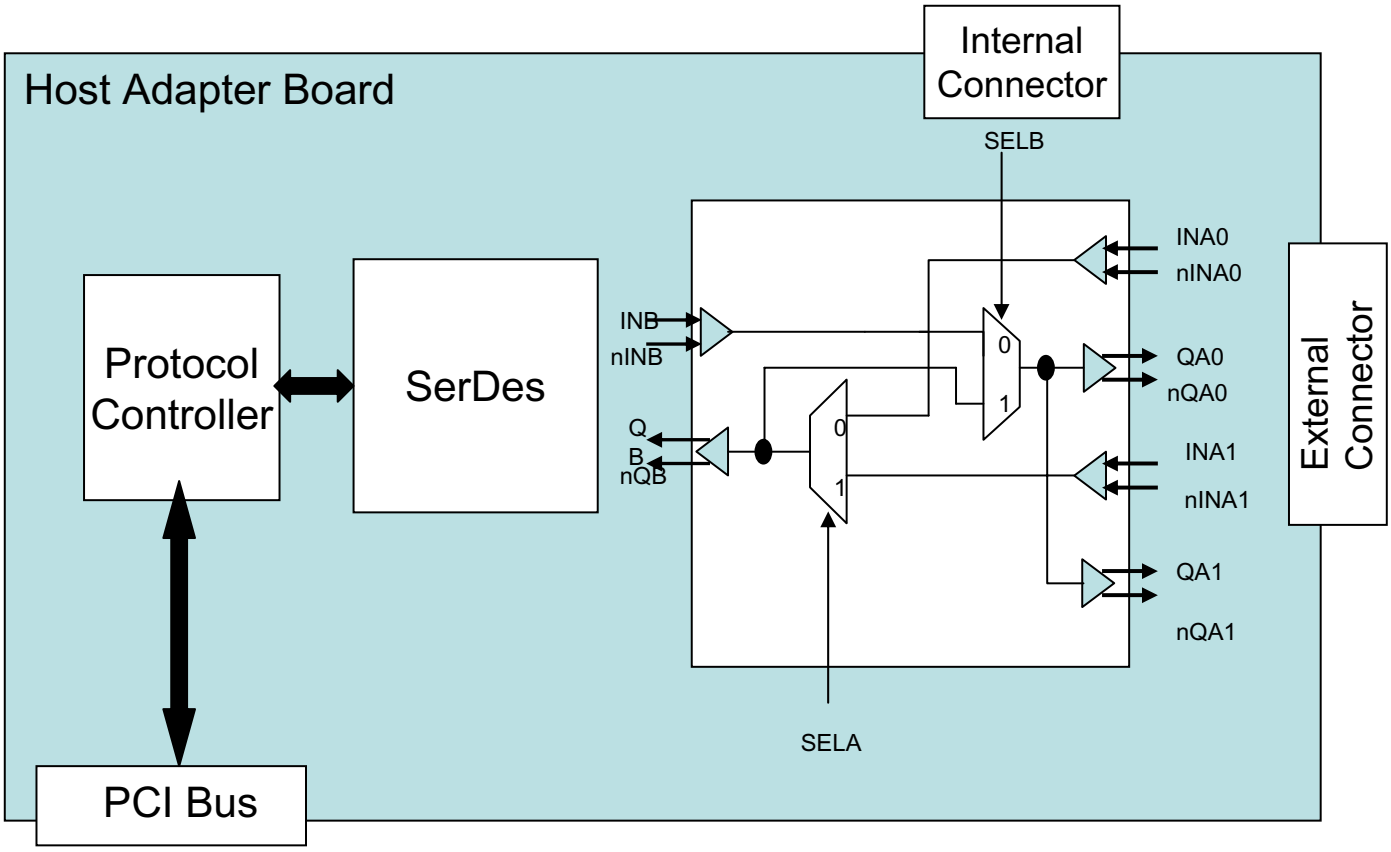
PIN ASSIGNMENT



ICS85354-01
16-Lead VFQFN
3mm x 3mm x 0.925 package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

HOST BUS ADAPTER BOARDS FOR ROUTING BETWEEN INTERNAL AND EXTERNAL CONNECTORS



HOT-SWAPPABLE LINKS TO REDUNDANT SWITCH FABRIC CARDS

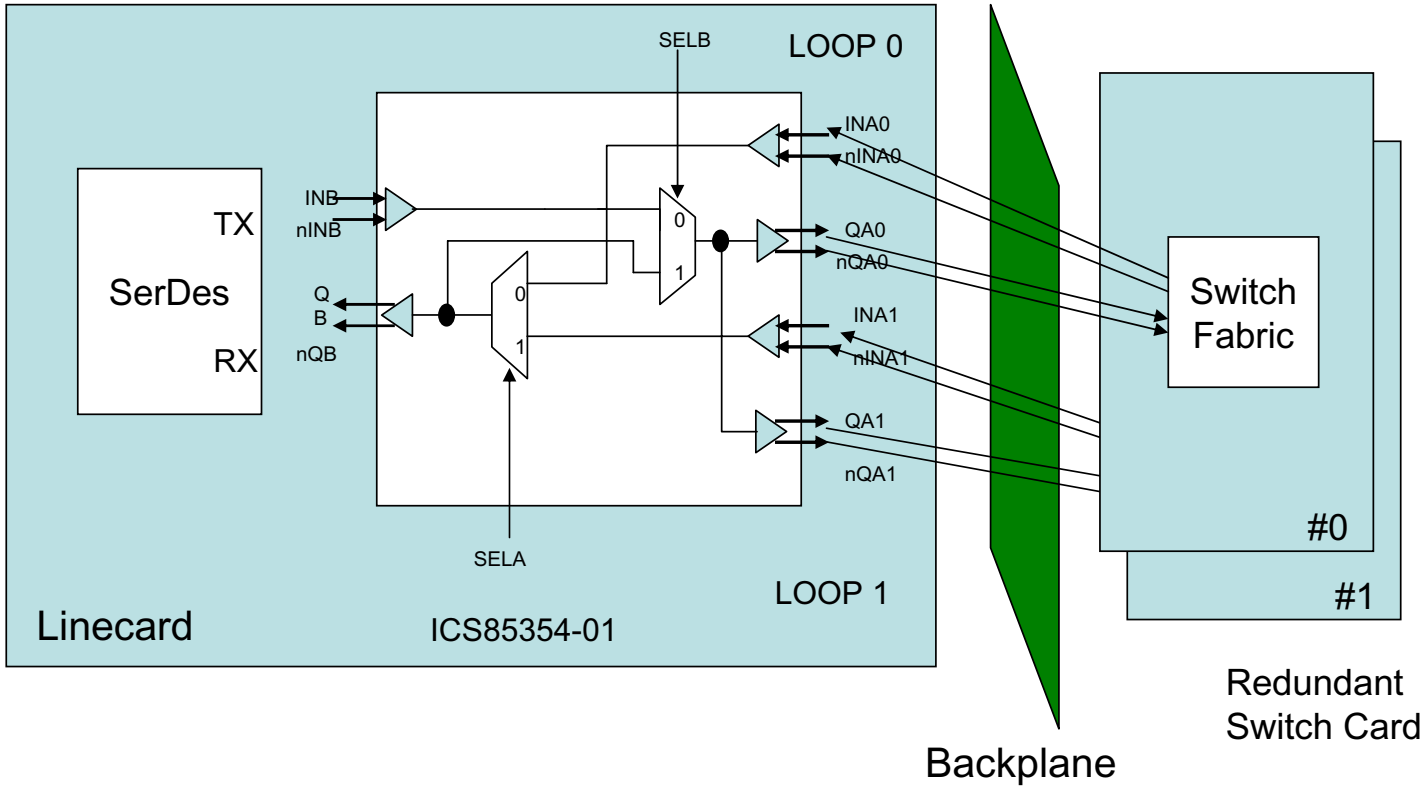


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	QA1, nQA1	Output		Differential output pair. LVPECL/ECL interface levels.
5	INB	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
6	nINB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
7	SELB	Input	Pulldown	Clock select pin for QBx outputs. When HIGH, selects QB1, nQB1 outputs. When LOW, selects QB0, nQB0 outputs. LVCMOS/LVTTL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	nINA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
10	INA1	Input	Pulldown	Non-inverting LVPECL differential clock input.
11	nINA0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
12	INA0	Input	Pulldown	Non-inverting LVPECL differential clock input.
13	V_{CC}	Power		Positive supply pin.
14	SELA	Input	Pulldown	Clock select pin for QA outputs. When HIGH, selects QA output. When LOW, selects nQA output. LVCMOS/LVTTL interface levels.
15, 16	nQB, QB	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			37.5		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			37.5		kΩ

TABLE 3. INPUT CONTROL FUNCTION TABLE

Control Inputs		Mode
SELA	SELB	
0	0	LOOP0 selected
0	1	LOOP1 selected
1	0	Loopback mode: LOOP0
1	1	Loopback mode: LOOP1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.465V, V_{EE} = 0V OR V_{CC} = 0V, V_{EE} = -3.465V TO -2.375V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current			40		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.465V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	0		0.8	V
			V_{CC} = 2.625V	0		0.7	V
I_{IH}	Input High Current	SELA, SELB	V_{CC} = V_{IN} = 3.465V, V_{CC} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	SELA, SELB	V_{CC} = 3.465 or 2.625V, V_{IN} = 0V	-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V, V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		V_{CC}-1.125	V_{CC}-1.025	V_{CC}-0.92	V_{CC}-1.075	V_{CC}-1.005	V_{CC}-0.93	V_{CC}-1.005	V_{CC}-0.97	V_{CC}-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC}-1.895	V_{CC}-1.755	V_{CC}-1.62	V_{CC}-1.875	V_{CC}-1.78	V_{CC}-1.685	V_{CC}-1.86	V_{CC}-1.765	V_{CC}-1.67	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	INAx, INB nINAx, nINB			150			150			150	µA
I_{IL}	Input Low Current	INAx, INB	-10			-10			-10			µA
		nINAx, nINB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.165V to -0.925V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for INAx, nINAx and INB, nINB is V_{CC} + 0.3V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{EE} = -3.465V TO -2.375V, V_{CC} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2V		V_{CC}	V_{EE}+1.2V		V_{CC}	V_{EE}+1.2V		V_{CC}	V
I_{IH}	Input High Current	INAx, INB nINAx, nINB			150			150			150	µA
I_{IL}	Input Low Current	INAx, INB	-10			-10			-10			µA
		nINAx, nINB	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for INAx, nINAx and INB, nINB is V_{CC} + 0.3V.

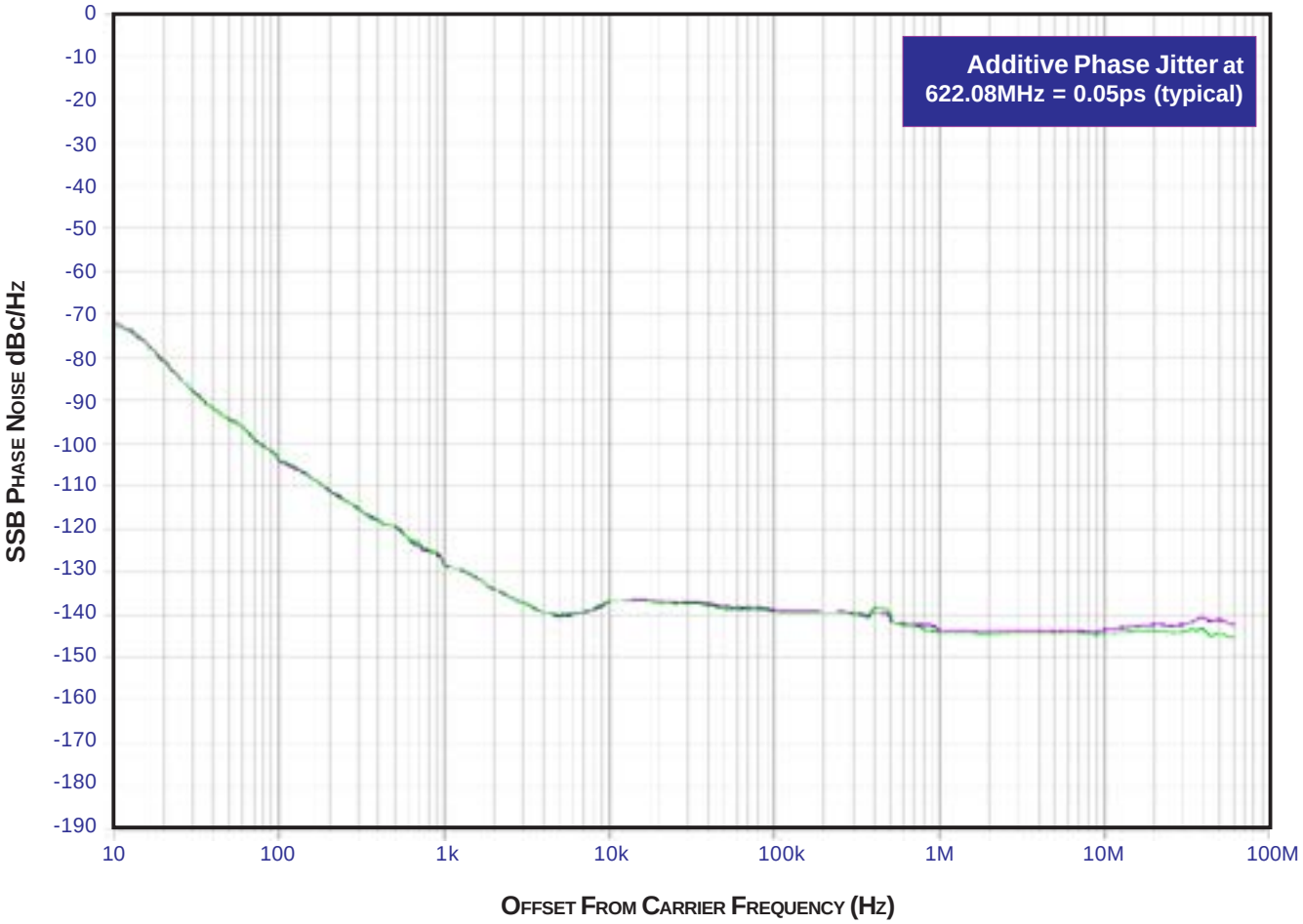
TABLE 5. AC CHARACTERISTICS, V_{CC} = 2.375V TO 3.465V, V_{EE} = 0V OR V_{CC} = 0V, V_{EE} = -3.465V TO -2.375V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1			440		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			85		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	622.08MHz (12kHz - 20MHz)		0.05		ps
	MUX Isolation			55		dB
t_R/t_F	Output Rise/Fall Time	20% to 80%		170		ps

All parameters are measured ≤ 1.3GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

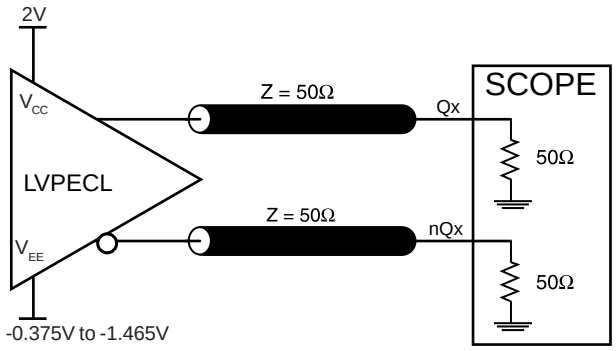
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

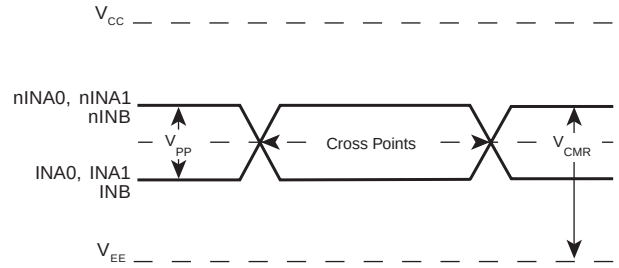


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

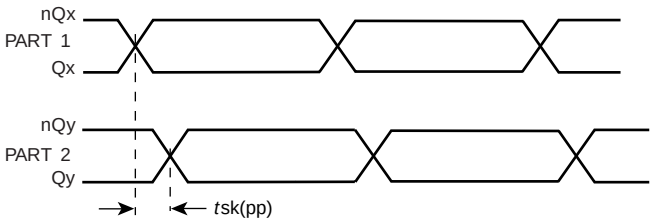
PARAMETER MEASUREMENT INFORMATION



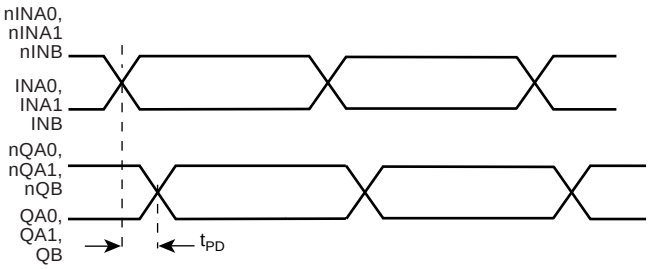
OUTPUT LOAD AC TEST CIRCUIT



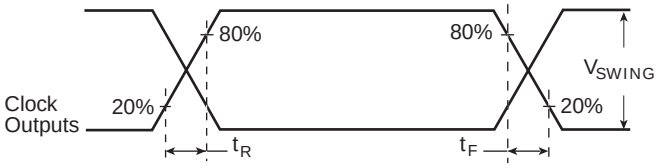
DIFFERENTIAL INPUT LEVEL



PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

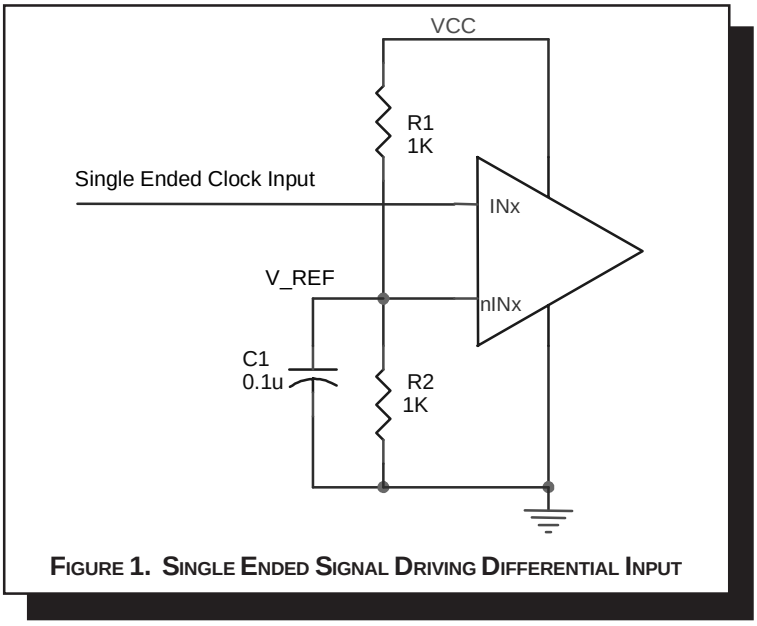


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

In/nIn INPUT:
For applications not requiring the use of the differential input, both IN and nIN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from IN to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL(DIFFERENTIAL) CLOCK INPUT INTERFACE

The IN/nIN accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS IN/nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

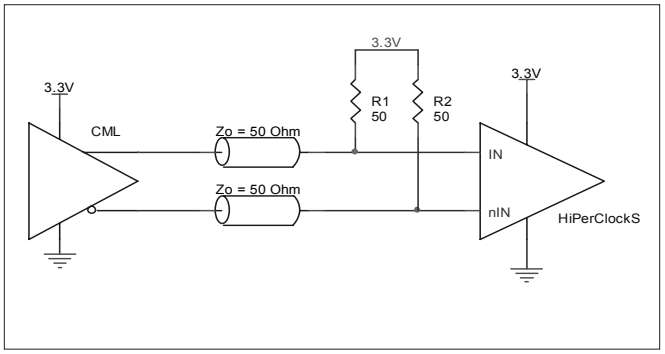


FIGURE 2A. HIPERCLOCKS IN/NIN INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

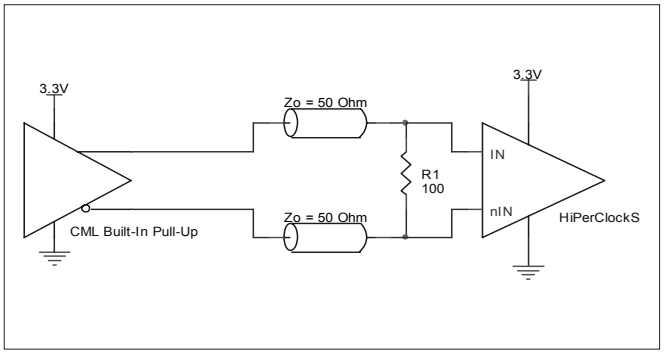


FIGURE 2B. HIPERCLOCKS IN/NIN INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

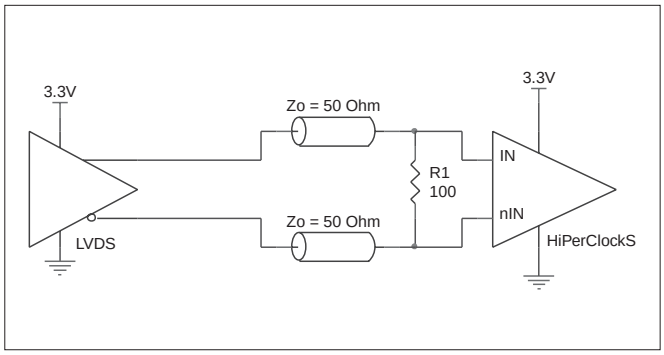


FIGURE 2C. HIPERCLOCKS IN/NIN INPUT DRIVEN BY A 3.3V LVPECL DRIVER

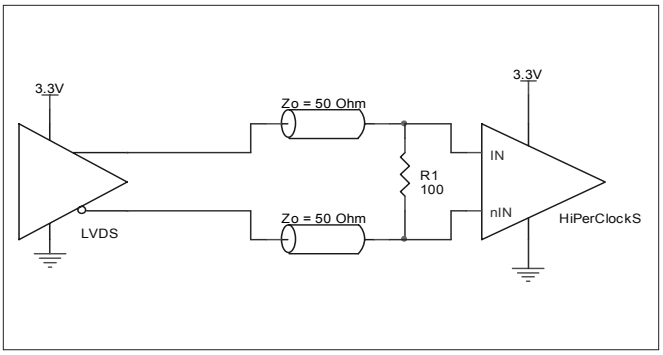


FIGURE 2D. HIPERCLOCKS IN/NIN INPUT DRIVEN BY A 3.3V LVDS DRIVER

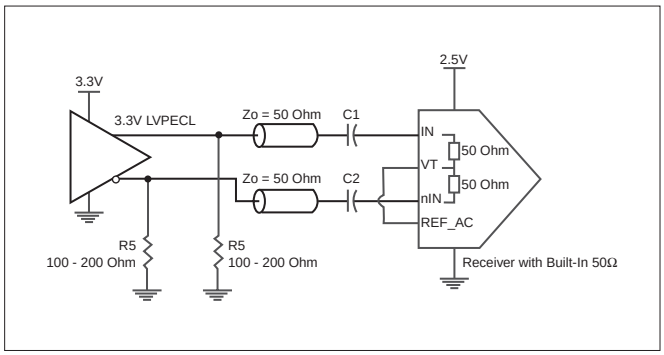


FIGURE 2E. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A 3.3V LVPECL DRIVER

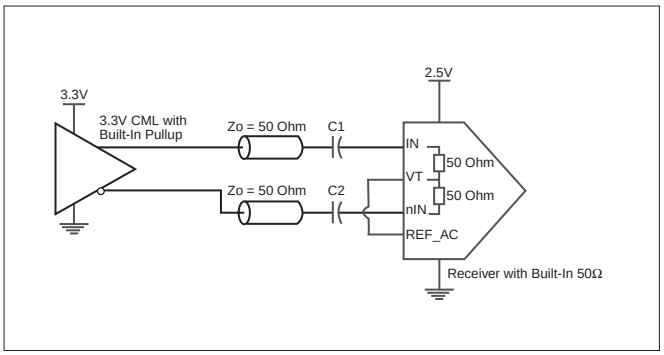


FIGURE 2F. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A 3.3V CML DRIVER WITH BUILT-IN PULLUP

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

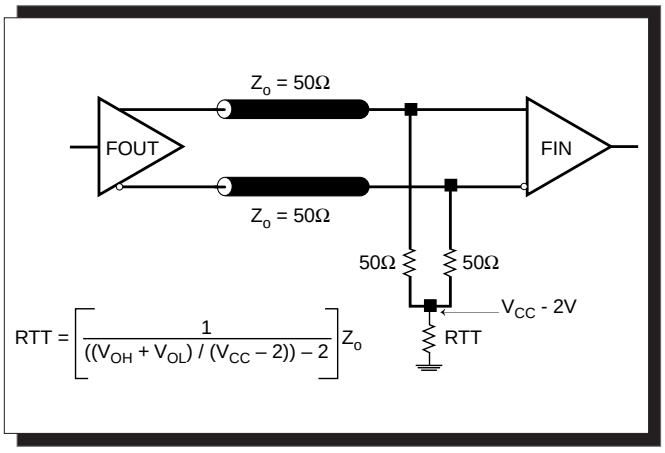


FIGURE 3A. LVPECL OUTPUT TERMINATION

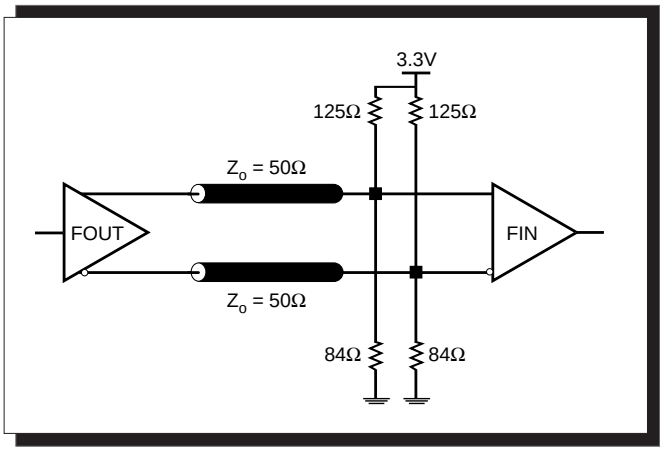


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

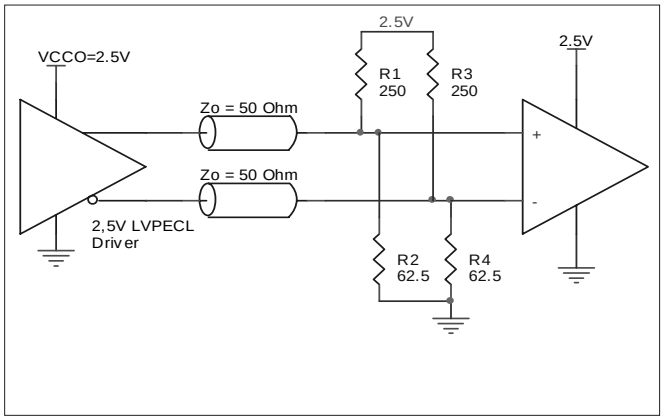


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

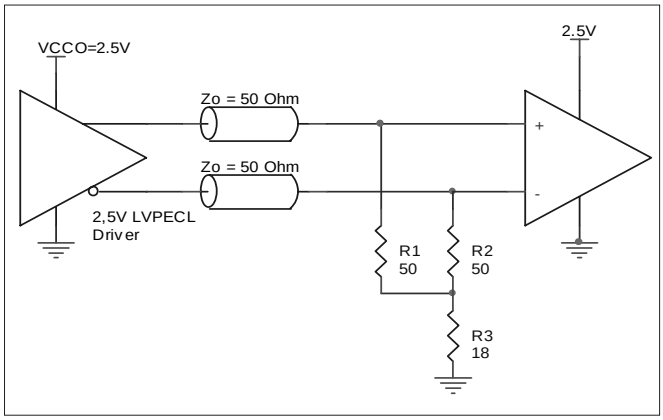


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

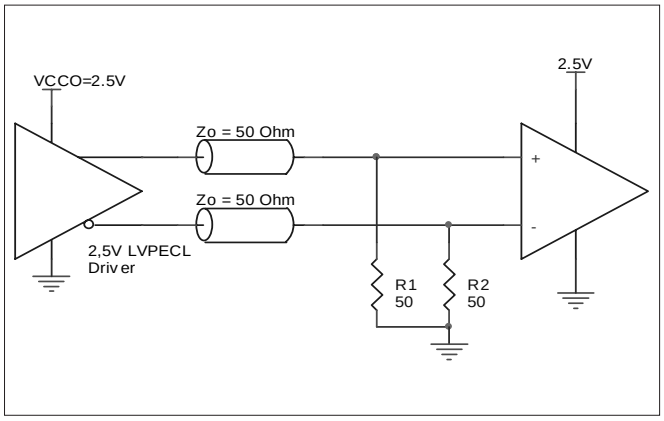


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85354-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85354-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 40mA = **138.6mW**
- Power (outputs)$_{MAX}$ = **30.92mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30.92mW = **92.76mW**

Total Power $_{MAX}$ (3.465, with all outputs switching) = 138.6mW + 92.76mW = **231.4mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used.
Assuming 0 air flow and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.231W * 51.5°C/W = 96.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow,
and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

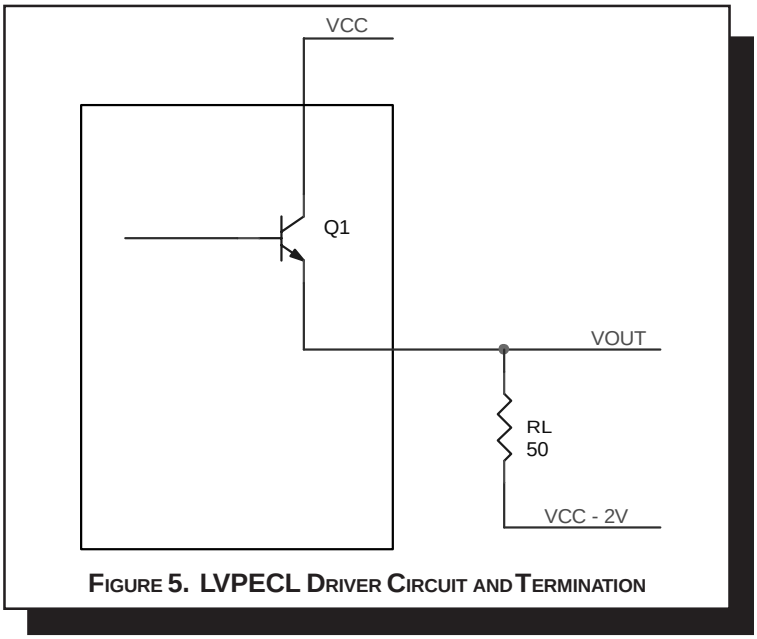


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.935V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.935}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.67V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DD\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50Ω] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50Ω] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.92mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS85354-01 is: 210

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

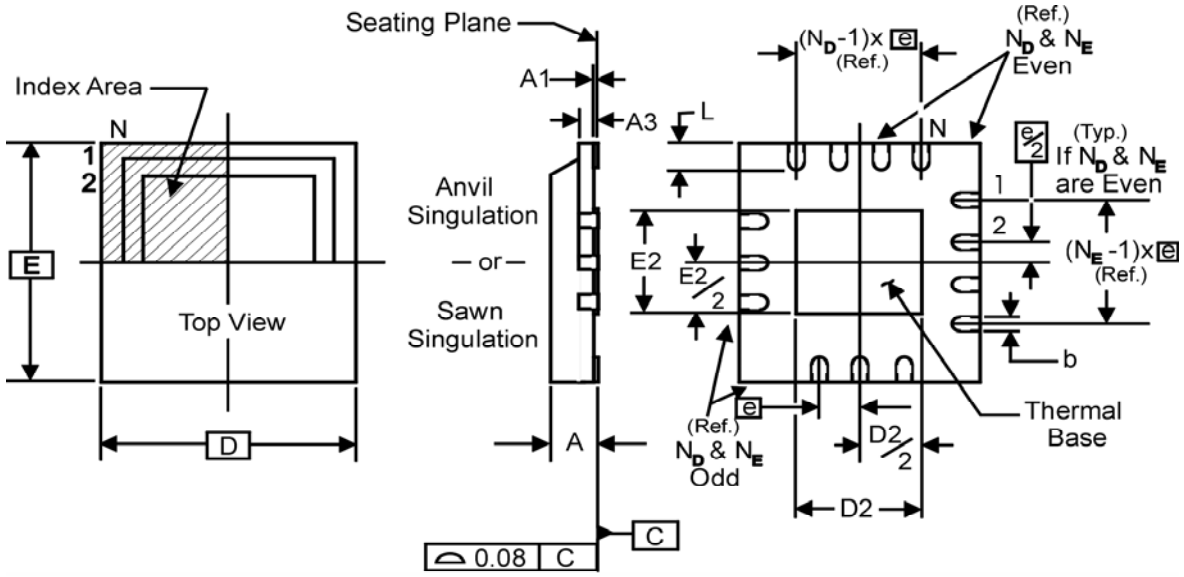


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85354AK-01	4A01	16 Lead VFQFN	Tube	-40°C to 85°C
ICS85354AK-01T	4A01	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS85354AK-01LF	A01L	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
ICS85354AK-01LFT	A01L	16 Lead "Lead-Free" VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-free configuration and are RoHS compliant.