

## 2:1 LVDS MULTIPLEXER WITH 1:2 FANOUT AND INTERNAL TERMINATION

ICS889474

### GENERAL DESCRIPTION

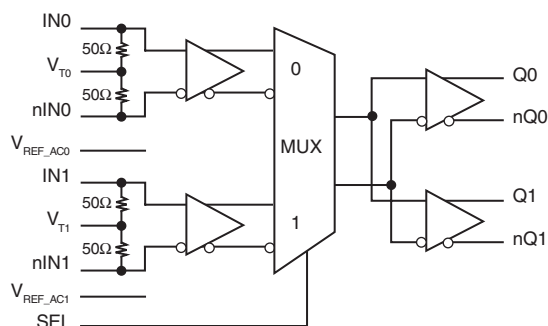


The ICS889474 is a high speed 2-to-1 differential multiplexer with integrated 2 output LVDS fanout buffer and internal termination and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS889474 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and  $V_{REF\_AC}$  pins allow other differential signal families such as LVPECL, LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The ICS889474 is packaged in a small 4mm x 4mm 24-pin VFQFN package which makes it ideal for use in space-constrained applications.

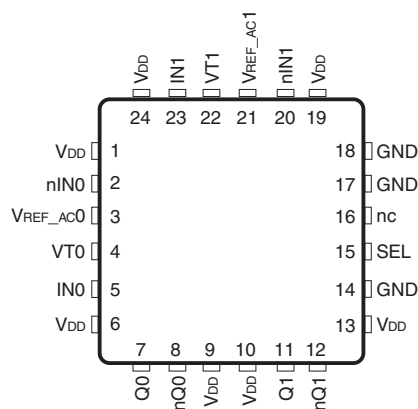
### FEATURES

- Two differential LVDS outputs
- $INx$ ,  $nINx$  pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, CML
- $50\Omega$  internal input termination to  $V_T$
- Maximum output frequency: 2GHz (maximum)
- Additive phase jitter, RMS: 0.06ps (typical)
- Output skew: 20ps (maximum)
- Propagation delay: 700ps (maximum)
- 2.5V operating supply
- $-40^\circ\text{C}$  to  $85^\circ\text{C}$  ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**ICS889474**

**24-Lead VFQFN**

4mm x 4mm x 0.925mm package body

**K Package**

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6, 9, 10, 13, 19, 24	$V_{DD}$	Power		Positive supply pins.
2, 20	nIN0, nIN1	Input		Inverting differential clock inputs. 50Ω internal input termination to $V_T$ .
3, 21	$V_{REF\_AC0}$ , $V_{REF\_AC1}$	Output		Reference voltage for AC-coupled applications.
4, 22	$V_{T0}$ , $V_{T1}$	Input		Termination inputs.
5, 23	IN0, IN1	Input		Non-inverting differential clock inputs. 50Ω internal input termination to $V_T$ .
7, 8	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
11, 12	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
14, 17, 18	GND	Power		Power supply ground.
15	SEL	Input	Pullup	Input select pin. LVCMOS/LVTTL interface levels.
16	nc	Unused		No connect.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLUP}$	Input Pullup Resistor			25		kΩ

TABLE 3. TRUTH TABLE

Inputs					Outputs	
IN0	nIN0	IN1	nIN1	SEL	Q0:Q1	nQ0:nQ1
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5\text{ V}$
Outputs, $I_O$ (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Input Current, $I_{INx}$ , $nI_{INx}$	$\pm 50\text{mA}$
$V_T$ Current, $I_{VT}$	$\pm 100\text{mA}$
Input Sink/Source, $I_{REF\_AC}$	$\pm 0.5\text{mA}$
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient)	49.5°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5\text{V} \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				80	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = 2.5\text{V} \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		0		0.7	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 2.625\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 2.5\text{V} \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Input Resistance	IN-to- $V_T$	45	50	55	$\Omega$
$R_{DIFF\_IN}$	Differential Input Resistance	$I_{INx}$ , $nI_{INx}$	90	100	110	$\Omega$
$V_{IH}$	Input High Voltage	$I_{INx}$ , $nI_{INx}$	1.2		$V_{DD}$	V
$V_{IL}$	Input Low Voltage	$I_{INx}$ , $nI_{INx}$	0		$V_{IN} - 0.1$	V
$V_{IN}$	Input Voltage Swing	$I_{INx}$ , $nI_{INx}$	0.1		$V_{DD}$	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing	$I_{INx}$ , $nI_{INx}$	0.2			V
$V_{T\_IN}$	IN-to- $V_T$	$I_{INx}$ , $nI_{INx}$			1.28	V
$V_{REF\_AC}$	Output Reference Voltage		$V_{DD} - 1.4$	$V_{DD} - 1.3$	$V_{DD} - 1.2$	V

**TABLE 4D. LVDS DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ;  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OUT}$	Output Voltage Swing		340	400		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing		680	800		mV
$V_{OCM}$	Output Common Mode Voltage		1.10		1.35	V
$\Delta V_{OCM}$	Change in Common Mode Voltage		-50		50	mV

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ;  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				4	Gpbs
		Q0:1/nQ0:1			2	GHz
$t_{PD}$	Propagation Delay, (Differential); NOTE 1	IN-to-Q	400		700	ps
		SEL-to-Q	250		600	ps
$tsk(o)$	Output Skew; NOTE 2, 4				20	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				200	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section, NOTE 5	155.52MHz, 12kHz – 20MHz		0.06		ps
$MUX_{ISOLATION}$	Mux Isolation			55		dB
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	70		220	ps

NOTE: All parameters are characterized at  $\leq 1GHz$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

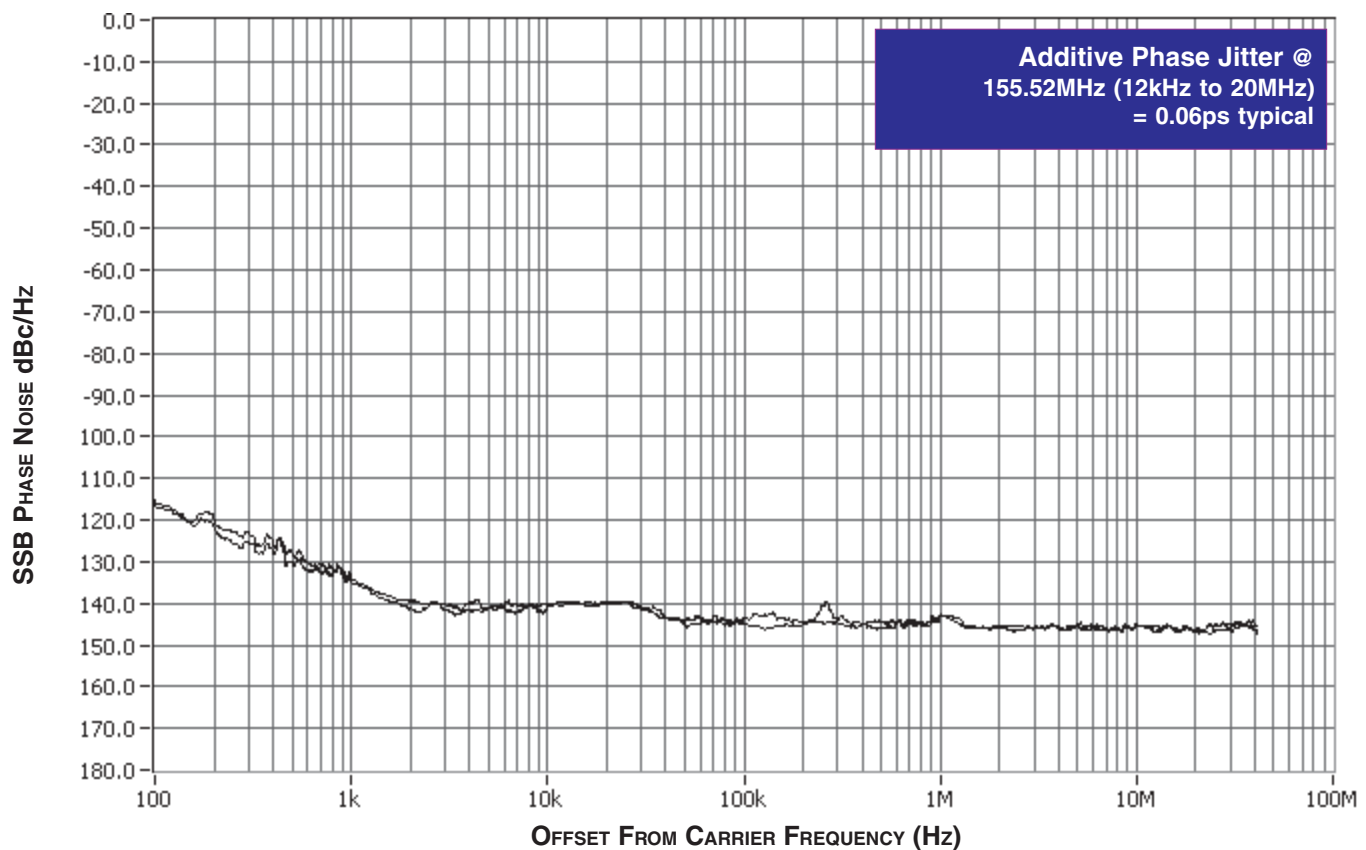
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Driving only one input clock.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz

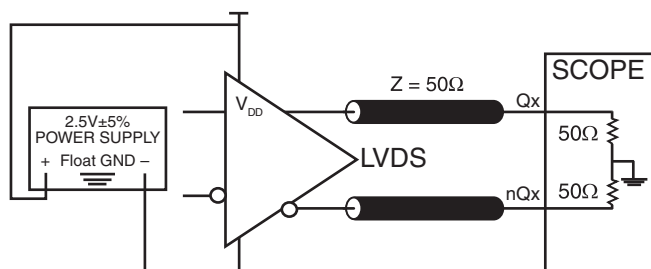
band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



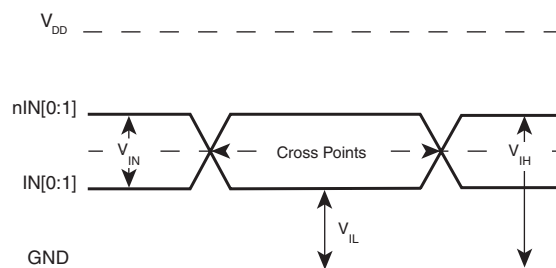
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the

device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

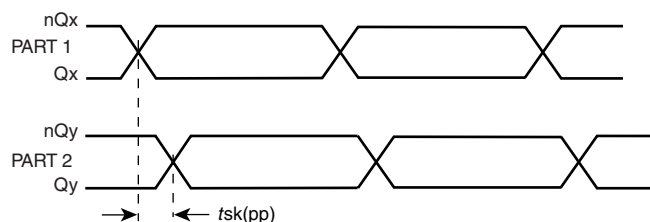
## PARAMETER MEASUREMENT INFORMATION



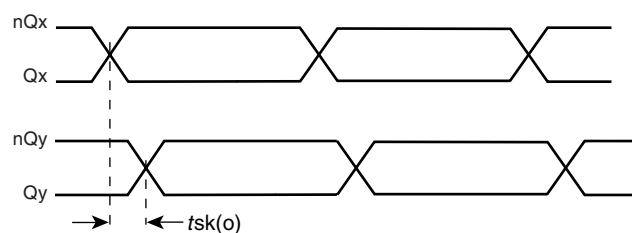
### OUTPUT LOAD AC TEST CIRCUIT



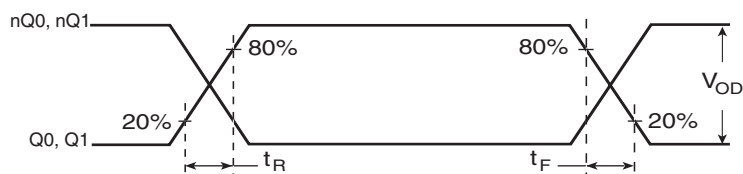
### DIFFERENTIAL INPUT LEVEL



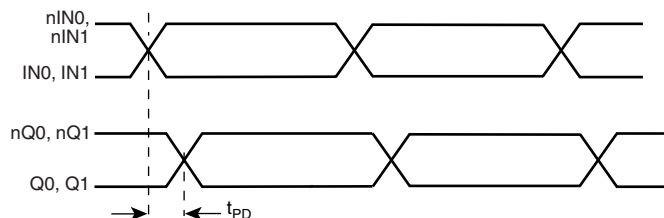
## PART-TO-PART SKEW



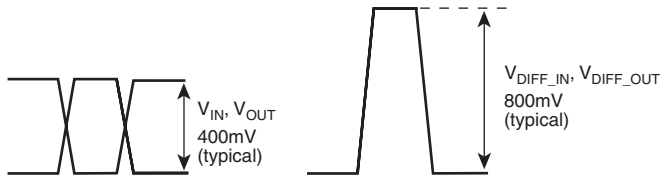
## OUTPUT SKEW



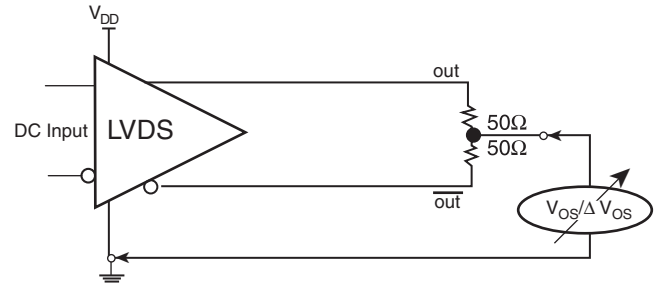
### OUTPUT RISE/FALL TIME



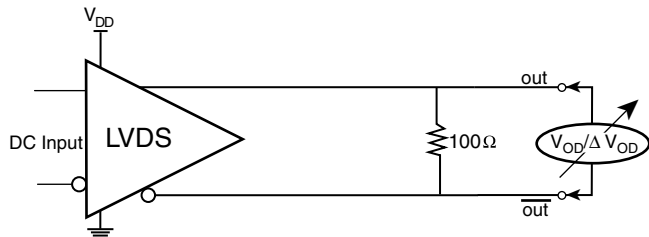
## PROPAGATION DELAY



SINGLE ENDED &amp; DIFFERENTIAL INPUT VOLTAGE SWING



OFFSET VOLTAGE SETUP



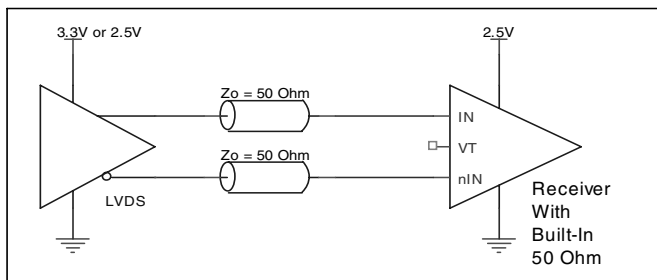
DIFFERENTIAL OUTPUT VOLTAGE SETUP

## APPLICATION INFORMATION

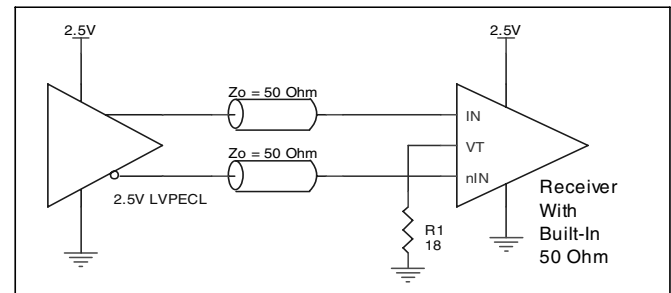
### LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, CML and other differential signals. The signal must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 1A to 1E show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The

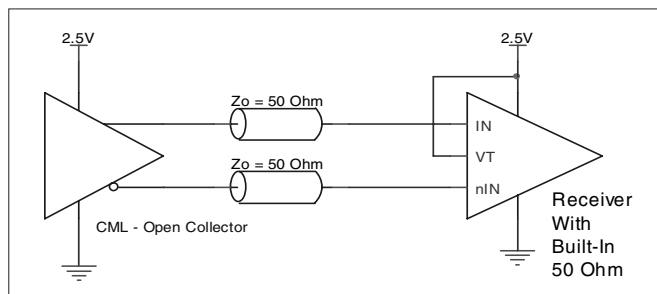
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



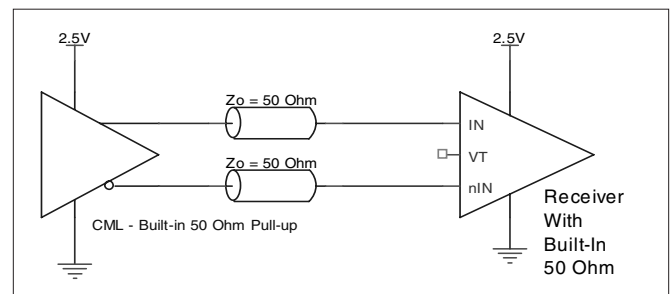
**FIGURE 1A. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER**



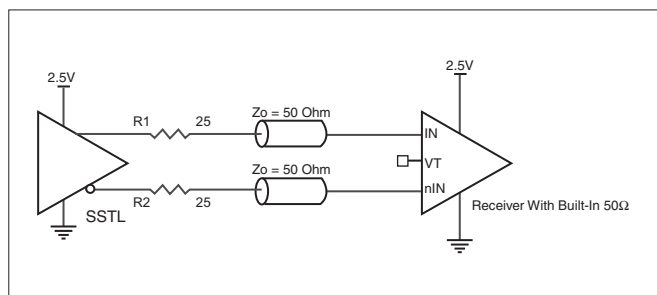
**FIGURE 1B. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER**



**FIGURE 1C. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER**



**FIGURE 1D. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP**



**FIGURE 1E. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER**



## RECOMMENDATIONS FOR UNUSED OUTPUT PINS

### INPUTS:

#### IN/nIN INPUTS

For applications not requiring the use of the differential input, both IN and nIN can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from IN to ground.

### OUTPUTS:

#### LVDS OUTPUTS

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, there should be no trace attached.

## 2.5V LVDS DRIVER TERMINATION

Figure 2 shows a typical termination for LVDS driver in characteristic impedance of 100 $\Omega$  differential (50 $\Omega$  single)

transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

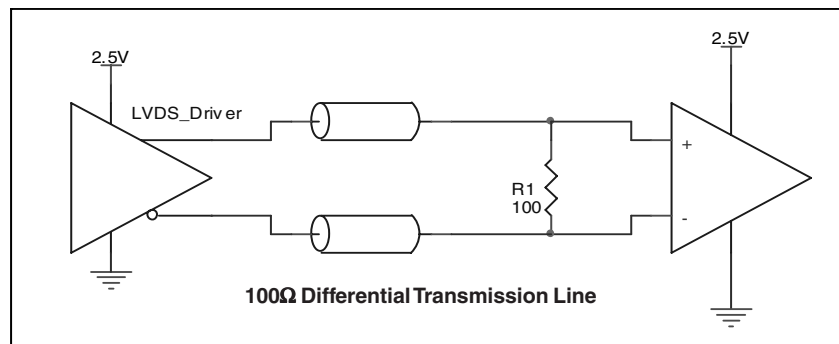


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

## 2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50 $\Omega$ TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pull up and pull down connect to true and complement of the unused input as shown in Figure 3.

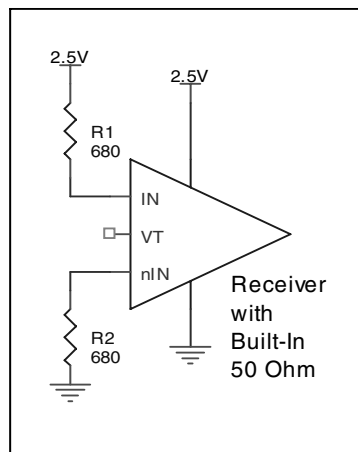


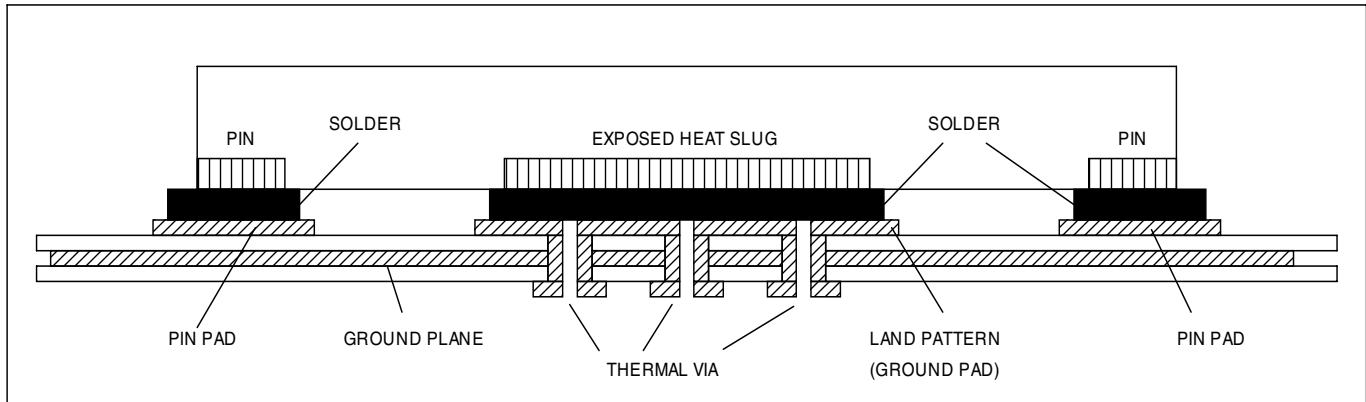
FIGURE 3. UNUSED INPUT HANDLING

### VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”)

are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**FIGURE 4. P.C. ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS889474. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS889474 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 2.625V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 80mA = \mathbf{210mW}$
- Power Dissipation at built-in terminations: Assume the input is driven by a 2.5V SSTL driver as shown in Figure 1E and estimated approximately 1.75V drop across IN and nIN.

Total Power Dissipation for the two 50Ω built-in terminations is:  $(1.75V)^2 / (50\Omega + 50\Omega) = \mathbf{30.6mW}$

Input pair for both inputs is  $2 * 30.6mW = 61.2mW$

**Total Power**<sub>MAX</sub> (2.625V, with all outputs switching) =  $210mW + 61.2mW = 271.2mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.271W * 49.5^\circ C/W = 98.4^\circ C$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-PIN VFQFN, FORCED CONVECTION**

$\theta_{JA}$ vs. 0 Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 24 LEAD VFQFN

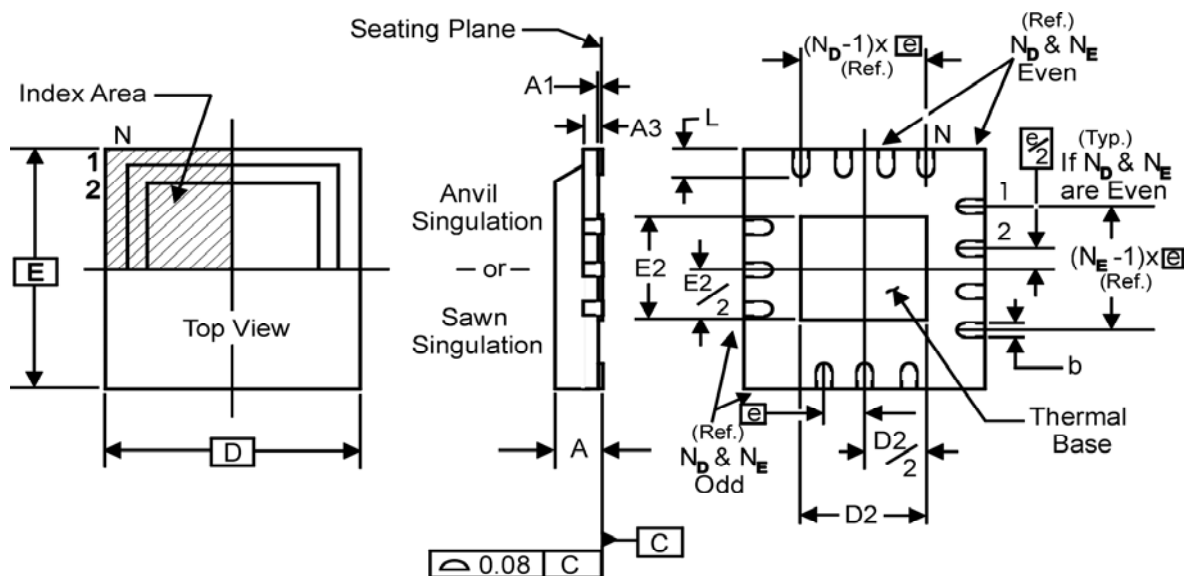
$\theta_{JA}$ vs. 0 Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

### TRANSISTOR COUNT

The transistor count for ICS889474 is: 367

Pin compatible with SY89474U

## PACKAGE OUTLINE - K SUFFIX FOR 24 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of

this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	24	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N <sub>D</sub>	6	
N <sub>E</sub>	6	
D	4	
D2	2.30	2.55
E	4	
E2	2.30	2.55
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
889474AK	89474A	24 Lead VFQFN	tube	-40°C to 85°C
889474AKT	89474A	24 Lead VFQFN	2500 tape & reel	-40°C to 85°C
889474AKLF	9474AL	24 Lead VFQFN "Lead-Free"	tube	-40°C to 85°C
889474AKLFT	9474AL	24 Lead VFQFN "Lead-Free"	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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