Integrated Circuit Systems, Inc.

ICS9179-03

Low Skew Fan Out Buffers

General Description

The **ICS9179-03** generates low skew clock buffers required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Outputs will handle up to 133MHz clocks. An output enable is provided for testability.

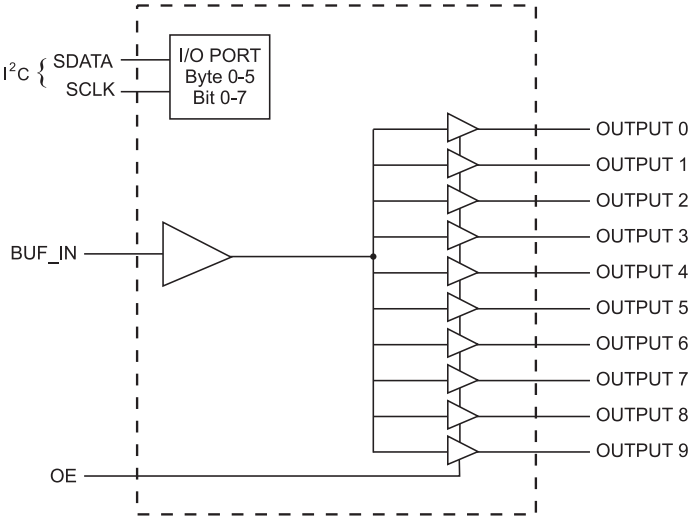
The device is a buffer with low output to output skew. This is a Fanout buffer device, not using an internal PLL. This buffer can also be a feedback to an external PLL stage for phase synchronization to a master clock. There are a total of ten outputs, sufficient for feedback to a PLL source and to drive four small outline DIMM modules (S.O. DIMM) at 2 clocks each. Or a total of ten outputs as a Fanout buffer from a common clock source.

The individual clock outputs are addressable through I^2C to be enabled, or stopped in a low state for reduced EMI when the lines are not needed.

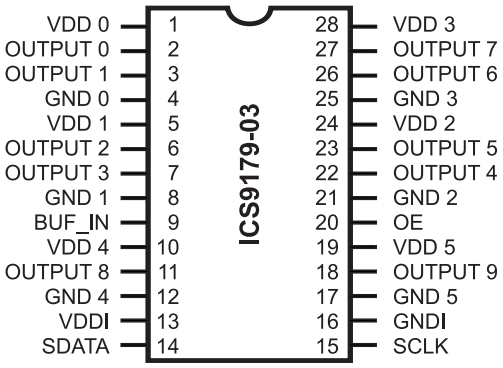
Features

- Ten High speed, low noise non-inverting buffers for (to 133MHz), clock buffer applications.
- Output slew rate faster than 1.5V/ns into 20pF
- Supports up to four small outline DIMMS (S.O. DIMM).
- Synchronous clocks skew matched to 250 ps window on OUTPUTs (0:9).
- I^2C Serial Configuration interface to allow individual OUTPUTs to be stopped low.
- Multiple VDD, VSS pins for noise reduction
- Tri-state pin for testing
- 3.0V – 3.7V supply range
- 28-pin (209 mil) SSOP and (6.1mm) TSSOP package

Block Diagram



Pin Configuration



28-Pin SSOP & TSSOP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 3	OUTPUT (0:1)	OUT	Clock outputs[1], uses VDD0, GND0
6, 7	OUTPUT (2:3)	OUT	Clock outputs[1], uses VDD1, GND1
22, 23	OUTPUT (4:5)	OUT	Clock outputs[1] uses VDD2, GND2
26, 27	OUTPUT (6:7)	OUT	Clock output[1] uses VDD3, GND3
11	OUTPUT8	OUT	Clock output[1] uses VDD4, GND4
18	OUTPUT9	OUT	Clock output[1] uses VDD5, GND5
9	BUF_IN	IN	Input for buffers
20	OE	IN	Tri-states all outputs when held LOW. Has internal pull-up.[2]
14	SDATA	I/O	Data pin for I^2C circuitry[3]
15	SCLK	I/O	Clock pin for I^2C circuitry[3]
1, 5, 10, 19, 24, 28	VDD (0:5)	PWR	3.3V Power supply for OUTPUT buffers
4, 8, 12, 16, 17, 21, 25	GND (0:5)	PWR	Ground for OUTPUT buffers
13	VDDI	PWR	3.3V Power supply for I^2C circuitry and internal logic
16	GNDI	PWR	Ground for I^2C circuitry and internal logic

Notes:

1. At power up all ten OUTPUTs are enabled and active.
2. OE has a 100K Ohm internal pull-up resistor to keep all outputs active.
3. The SDATA and SCLK inputs both also have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.

Power Groups

VDD (0:5), GND (0:5) = Power supply for OUTPUT buffer

VDDI, GNDI = Power supply for I^2C circuitry

Technical Pin Function Descriptions

VDD
This is the power supply to the internal core logic of the device as well as the clock output buffers for OUTPUT (0:9).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

OUTPUT (0:9)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the OUTPUTs output is controlled by the supply voltage that is applied to VDD of the device, operates at 3.3 volts.

I^2C
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

BUF_IN
Input for Fanout buffers (OUTPUT 0:9).

OE
OE tristates all outputs when held low.

VDD1
This is the power supply to I^2C circuitry.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controler (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmaps

Byte 0: OUTPUT Clock Register (Default=0)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	1	Reserved
Bit6	-	1	Reserved
Bit5	-	1	Reserved
Bit4	-	1	Reserved
Bit3	7	1	OUTPUT3
Bit2	6	1	OUTPUT2
Bit1	3	1	OUTPUT1
Bit0	2	1	OUTPUT0

Notes: 1 = Enabled; 0 = Disabled, outputs held low
Note: PWD = Power-Up Default

Byte 1: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	27	1	OUTPUT7 (Act/Inact)
Bit 6	26	1	OUTPUT6 (Act/Inact)
Bit 5	23	1	OUTPUT5 (Act/Inact)
Bit 4	22	1	OUTPUT4 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes: 1 = Enabled; 0 = Disabled, outputs held low
Note: PWD = Power-Up Default

Byte 2: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	18	1	OUTPUT9 (Act/Inact)
Bit 6	11	1	OUTPUT8 (Act/Inact)
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes: 1 = Enabled; 0 = Disabled, outputs held low

ICS9179-03 Power Management

The values below are estimates of target specifications.

Condition	Max 3.3V supply consumption Max discrete cap loads VDD = 3.465V All static inputs = VDD or GND
No Clock Mode (BUF_IN - VDD1 or GND) I²C Circuitry Active	3mA
Active 66MHz (BUF_IN = 66.66MHz)	230mA
Active 100MHz (BUF_IN = 100.00MHz)	360mA
Active 133MHz (BUF_IN = 133.33MHz)	460mA

Functionality

OE#	OUTPUT (0:9)
0	Hi-Z
1	1 X BUF_IN

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	uA
Input Low Current	I_{IL}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA
	I_{IL}	V_{IN} = 0 V; Inputs with 100K pull-up resistors	-60	-33		uA
Operating Supply Current	I_{DD1}	C_L = 0 pF; F_{IN} @ 66M		80	120	mA
	I_{DD2}	C_L = 0 pF; F_{IN} @ 100M		120	180	mA
	I_{DD3}	C_L = 0 pF; F_{IN} @ 133M		170	240	mA
	I_{DD4}	C_L = 30 pF; RS=33Ω; F_{IN} @ 66M		180	260	mA
	I_{DD5}	C_L = 30 pF; RS=33Ω; F_{IN} @ 100M		240	360	mA
	I_{DD6}	C_L = 30 pF; RS=33Ω; F_{IN} @ 133M		350	460	mA
Input frequency	F_i[1]	V_{DD} = 3.3 V; All Outputs Loaded	10		133	MHz
Input Capacitance	C_{IN}[1]	Logic Inputs			5	pF

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - Outputs

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN}	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH}	I_{OH} = -30 mA	2.3	3		V
Output Low Voltage	V_{OL}	I_{OL} = 23 mA		0.27	0.4	V
Output High Current	I_{OH}	V_{OH} = 2.0 V		-115	-54	mA
Output Low Current	I_{OL}	V_{OL} = 0.8 V	40	57		mA
Rise Time[1]	T_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.95	1.33	ns
Fall Time[1]	T_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.95	1.33	ns
Duty Cycle[1]	D_t	V_T = 1.5 V	45	50	55	%
Skew[1]	T_{sk}	V_T = 1.5 V		110	250	ps
Propagation[1,2]	T_{PHL1}	V_T = 1.5 V	1	5.2	5.5	ns
	T_{PLH1}	V_T = 1.5 V	1	5.2	5.5	ns
	T_{PHL2}	50% Buffer In to 90% Out	1	4.3	5	ns
	T_{PLH2}	50% Buffer In to 10% Out	1	4.3	5	ns
	T_{EN}	V_T = 1.5 V	1		8	ns
	T_{DIS}	V_T = 1.5 V	1		8	ns

Note1: Paramater is guaranteed by design and characterization for all operating frequencies, (10MHz - 133MHz). Not 100% tested in production

Note2: Duty cycle of input clock is 47.5% to 52.5%. Input edge rate is for propagation delay ≥ 1V/ns

General Layout Precautions:

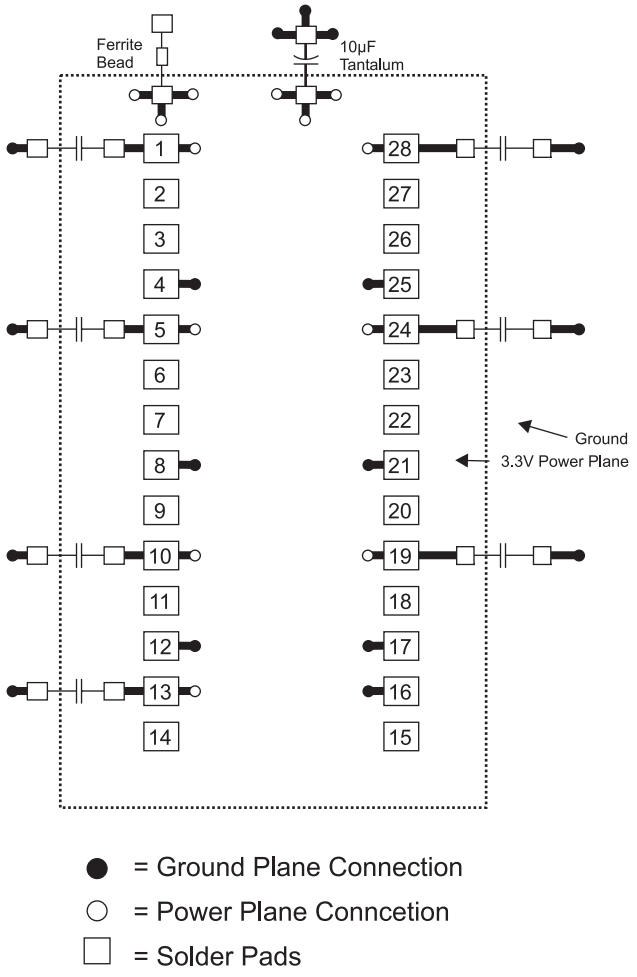
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

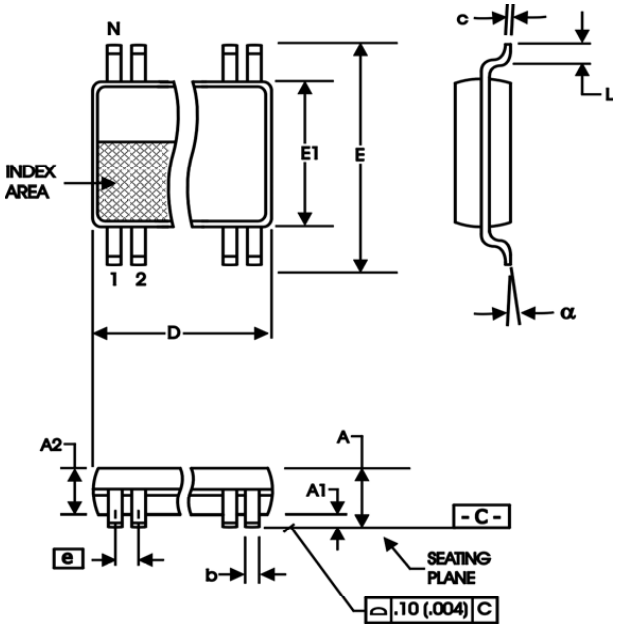
Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.

Capacitor Values:

All unmarked capacitors are 0.01µF ceramic





209 mil SSOP

209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

9179yF-03LF-T

Example:

XXXX y F - PPPLF - T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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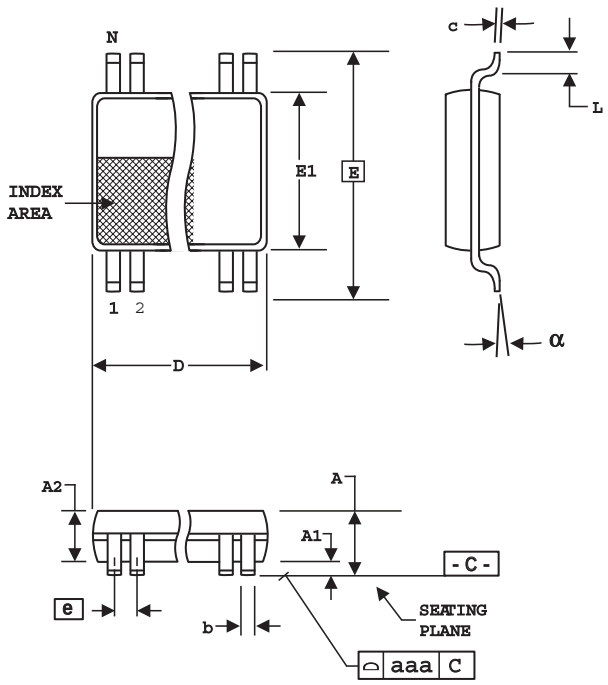

6.10 mm. Body, 0.65 mm. Pitch TSSOP
(240 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0038

Ordering Information

9179yG-03LF-T

Example:

XXXX y G - PPPLF - T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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Revision History

Rev.	Issue Date	Description	Page #
J	8/29/2005	Added LF Ordering Information.	9, 10
K	12/15/2008	Removed ICS prefix from ordering information	9, 10