LOW SKEW, PCI-X 1-TO-4 FANOUT BUFFER

ICS830584I

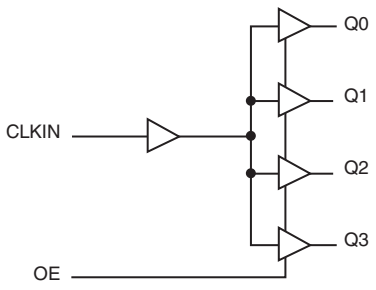
General Description

The ICS830584I is a low skew, general purpose PCI-X 1-to-4 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Guaranteed output and part-to-part skew characteristics make the ICS830584I ideal for those clock distribution applications demanding well defined performance and repeatablility. The ICS830584I is designed and characterized from -40°C to 85°C for industrial applications and is packaged in an 8 TSSOP package.

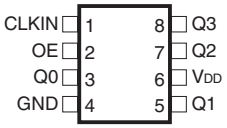
Features

- General purpose and PCI-X 1:4 clock buffer
- Four single-ended LVCMOS/LVTTL clock outputs
- One single-ended LVCMOS/LVTTL clock input
- Maximum output frequency: 140MHz
- Output enable control (outputs disabled in logic low state)
- Output skew: 100ps (maximum)
- Part-to-part skew: 400ps (maximum)
- Additive phase jitter, RMS: 0.15ps (typical)
- Space-saving 8 lead TSSOP package
- Full 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS830584I
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLKIN	Input		Single-ended clock input reference signal. LVCMOS/LVTTL interface levels.
2	OE	Input		Output enable control input pin. See Table 3, Function Table. LVCMOS / LVTTL interface levels.
3, 5, 7. 8	Q0, Q1, Q2, Q3	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
4	GND	Power		Power supply ground.
6	V_{DD}	Power		Positive supply pin.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3. FUNCTION TABLE

Inputs		Outputs
OE	CLKIN	Q0:Q3
0	0	0
0	1	0
1	0	0
1	1	1

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	121.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Recommended Operating Conditions, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage		0.7*V_{DD}			V
V_{IL}	Low Level Input Voltage				0.3*V_{DD}	V
V_I	Input Voltage		0		V_{DD}	V
I_{OH}	High-Level Output Current				-24	mA
I_{OL}	Low-Level Output Current				24	mA
T_A	Operating Free-Air Temperature		-40		85	°C

Table 4B. DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical†	Maximum	Units
V_{IK}	Input Voltage	I_I = -18mA			–1.2	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{DD} – 0.2			V
		I_{OH} = -24mA	2			V
		I_{OH} = -12mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.2	V
		I_{OL} = 24mA			0.8	V
		I_{OL} = 12mA			0.55	V
I_{OH}	Output High Current	V_O = 1V	–50			mA
		V_O = 1.65V		–55		mA
I_{OL}	Output Low Current	V_O = 2V	60			mA
		V_O = 1.65V		70		mA
I_I	Input Current	V_I = 0V or V_{DD}			±150	µA
I_{DD}	Dynamic Current	f = 67MHz			37	mA
C_i	Input Capacitance	V_I = 0V or V_{DD}		3		pF
C_o	Output Capacitance	V_I = 0V or V_{DD}		3.2		pF

†All typical values are at respective nominal V_{DD} and 25°C.

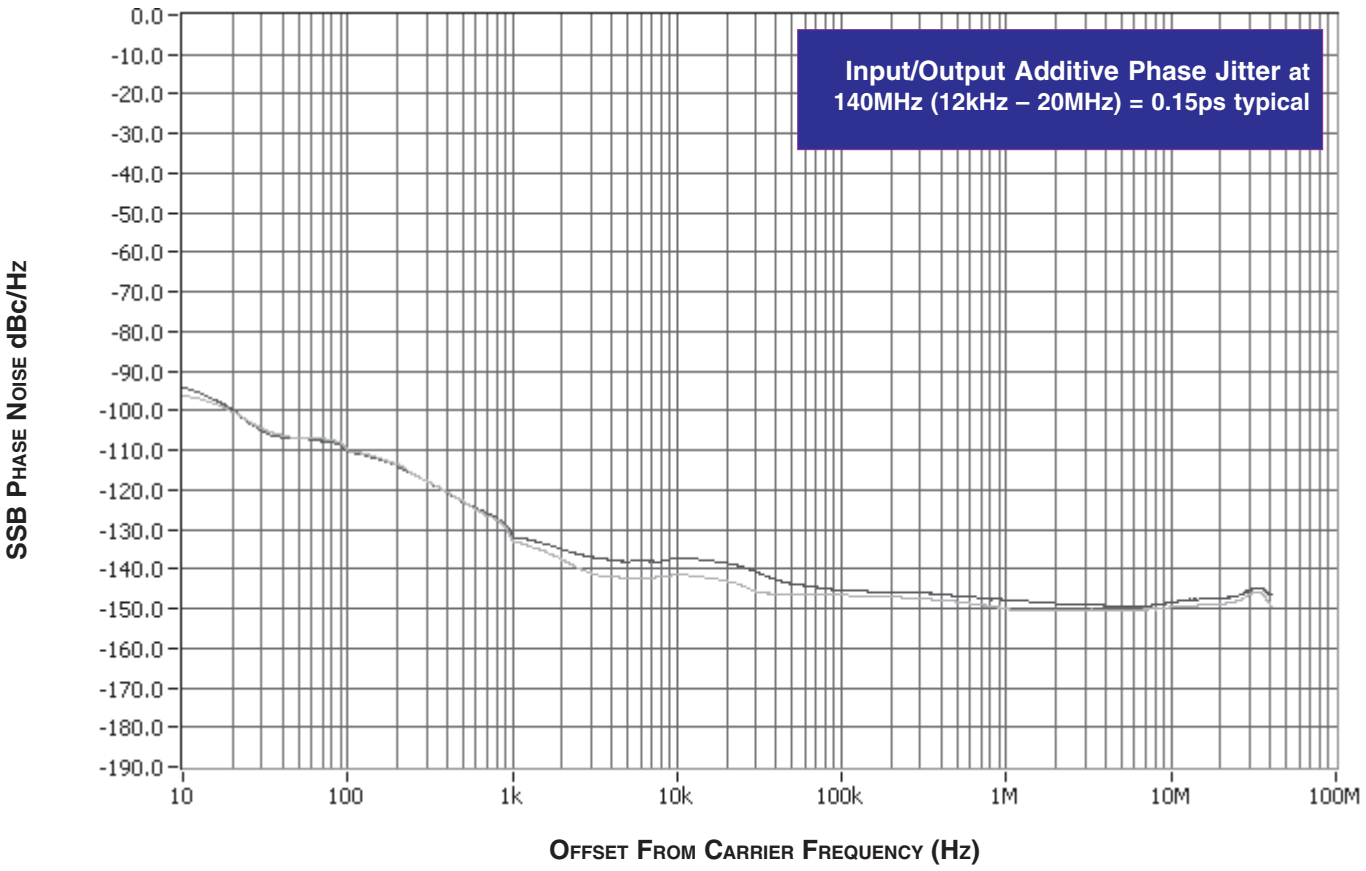
TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V ± 0.3V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical†	Maximum	Units
f_{clk}	Clock Frequency; NOTE 1		0		140	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 2		1.8	2.5	3	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 2		1.8	2.4	3	ns
*t*sk(o)	Output Skew; NOTE 3, 4			50	100	ps
*t*sk(p)	Pulse Skew	140MHz			170	ps
*t*sk(pr)	Process Skew			200	300	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5			250	400	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	140MHz, Integration Range: 10kHz – 20MHz		0.15		ps
T_{high}	CLK High Time	66MHz	6			ns
		140MHz	3			ns
T_{low}	CLK Low Time	66MHz	6			ns
		140MHz	3			ns
t_R	Output Rise Slew Rate‡	0.2V_{DD} to 0.6V_{DD}	1.5	2.7	4	V/ns
t_F	Output Fall Slew Rate‡	0.6V_{DD} to 0.2V_{DD}	1.5	2.7	4	V/ns

†All typical values are at respective nominal V_{DD}.
‡This symbol is according to PCI-X terminology.
NOTE 1: Switching characteristics over recommended ranges of supply voltages and operating free-air temperature, C_L = 10pF, V_{DD} = 3.3V ± 0.3V.
NOTE 2: Measured from $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DD}/2$.

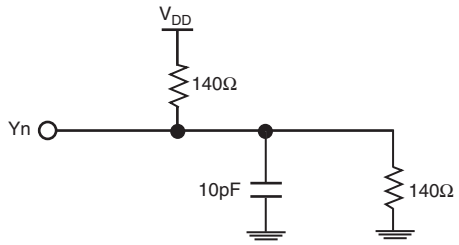
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

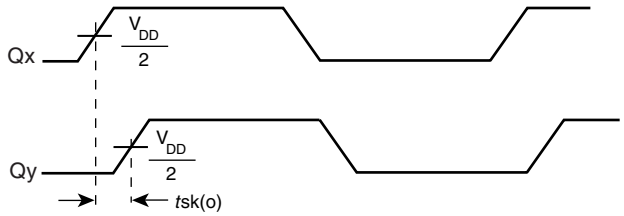


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

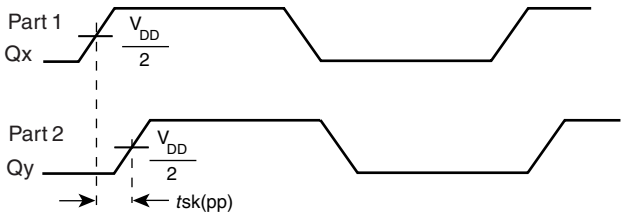
Parameter Measurement Information



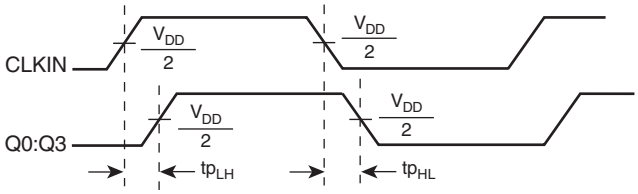
3.3V Core/3.3V Output Load AC Test Circuit



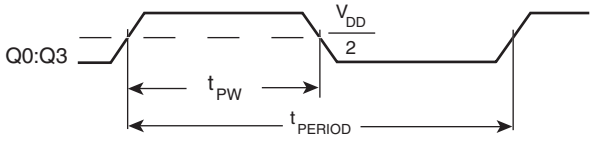
Output Skew



Part-to-Part Skew

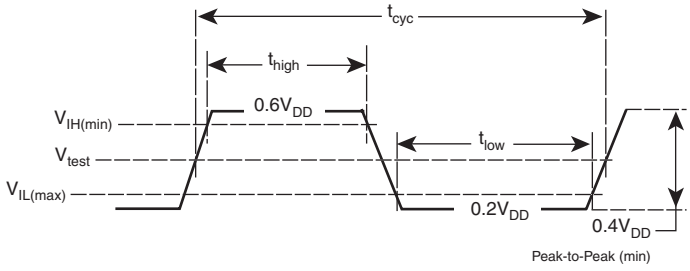


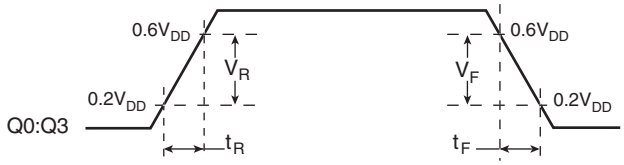
Propagation Delay



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period





Parameter	Value	Unit
$V_{IH(min)}$	$0.5V_{DD}$	V
$V_{IL(max)}$	$0.35V_{DD}$	V
V_{test}	$0.4V_{DD}$	V

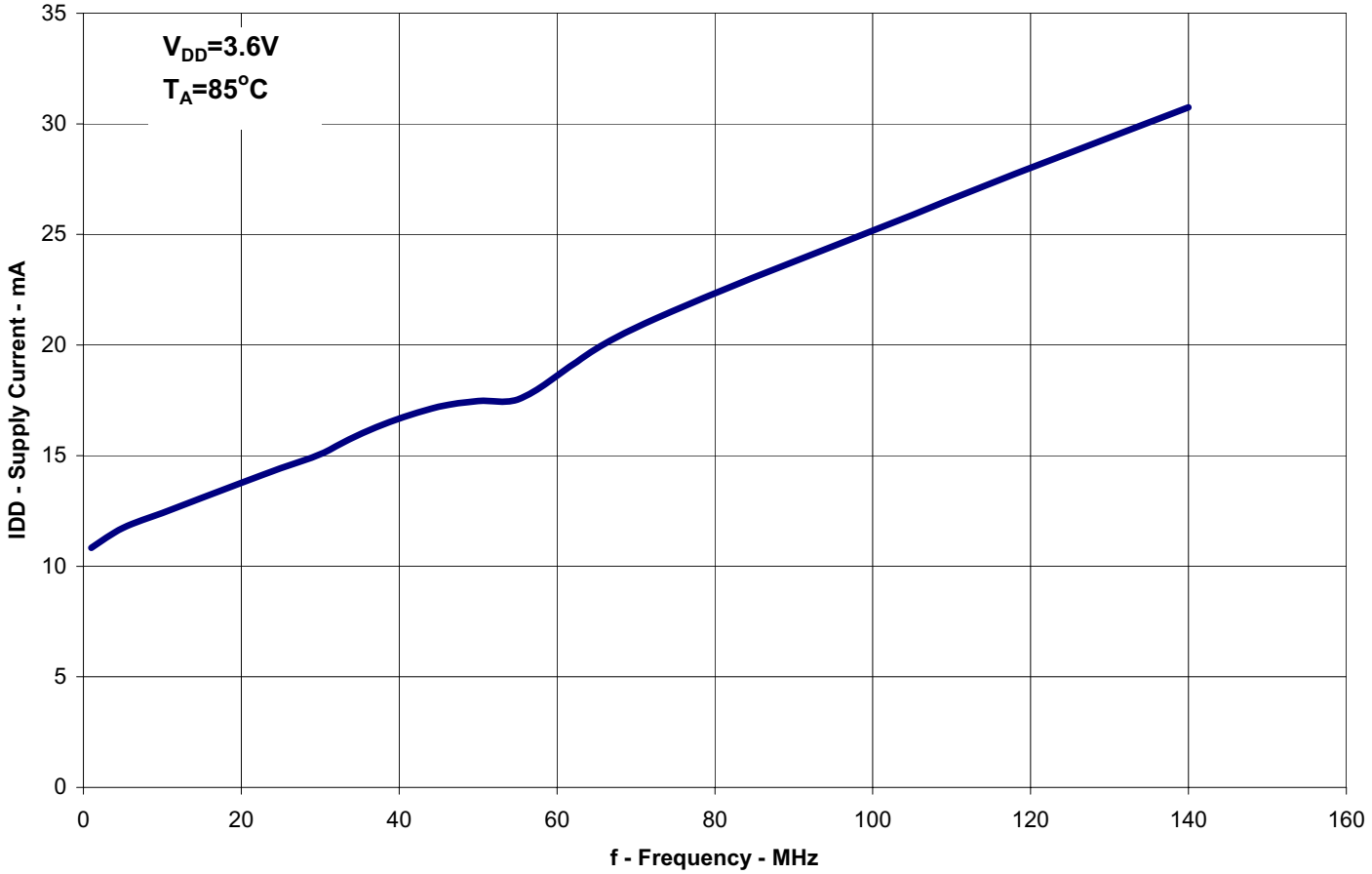
NOTE: All parameters are according to PCI-X 1.0 specifications

Output Rise/Fall Slew Rates

Clock Waveform

PARAMETER MEASUREMENT INFORMATION, CONTINUED

Supply Current vs Frequency



Application Information

Recommendations for Unused Input and Output Pins

Inputs:

OE Input
The OE pin must be tied either HIGH or LOW. Do not leave floating.

Outputs:

LVCMOS Outputs
All unused LVCMOS outputs can be left floating. We recommend that there is no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 8 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	121.5°C/W	117.3°C/W	115.3°C/W

Transistor Count
The transistor count for ICS830584I is: 307

Package Outline - G Suffix for 8 Lead TSSOP

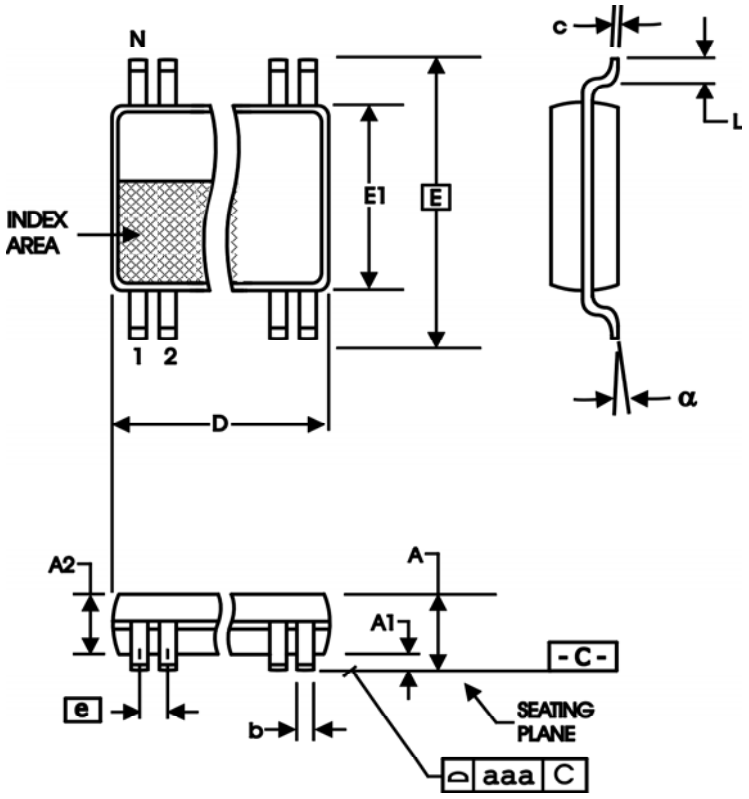


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
830584AGILF	84AIL	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
830584AGILFT	84AIL	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4B	3	DC Characteristics Table - corrected Input Current typo from ±5µA max. to ±150µA max.	3/18/08

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