Integrated Circuit Systems, Inc.

ICS8547

HEX, LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-LVDS CLOCK BUFFERS

GENERAL DESCRIPTION

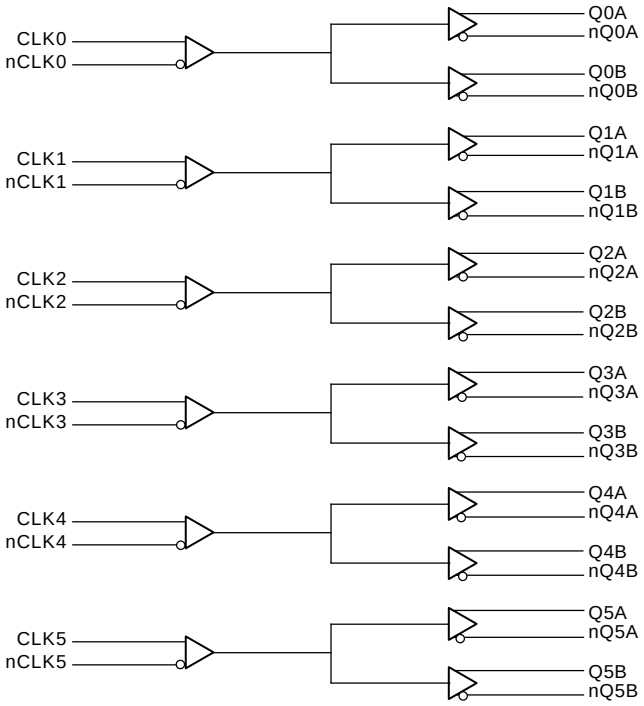
The ICS8547 is a Hex low skew, high performance 1-to-2 Differential-to-LVDS Clock Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8547 provides a low power, low noise, point-to-point solution for distributing clock signals over controlled impedances of 100Ω. The ICS8547 has six selectable clock inputs. The CLKx, nCLKx pairs can accept any differential input levels and translates them to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew specifications make the ICS8547 ideal for those applications demanding well defined performance and repeatability.

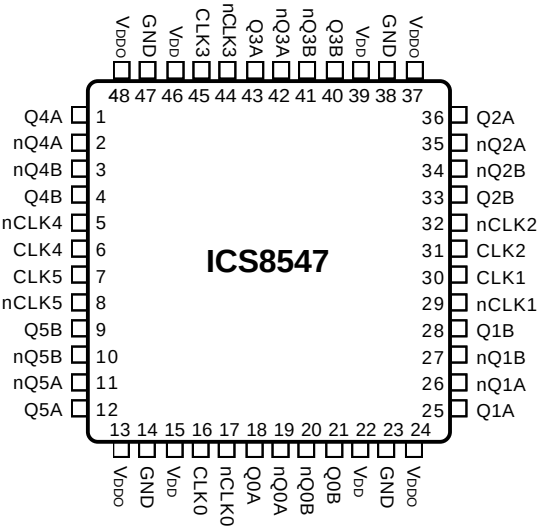
FEATURES

- 12 LVDS outputs
- Selectable CLKx, nCLKx inputs
- CLKx, nCLKx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, DCM) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLKx input
- Output skew: 250ps (maximum)
- Bank skew: 15ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.8ns (maximum)
- 3.3V operating supply
- 0°C to 85°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q4A, nQ4A	Output		Differential output pair. LVDS interface levels.
3, 4	nQ4B, Q4B	Output		Differential output pair. LVDS interface levels.
5	nCLK4	Input	Pullup	Inverting differential clock input.
6	CLK4	Input	Pulldown	Non-inverting differential clock input.
7	CLK5	Input	Pulldown	Non-inverting differential clock input.
8	nCLK5	Input	Pullup	Inverting differential clock input.
9, 10	Q5B, nQ5B	Output		Differential output pair. LVDS interface levels.
11, 12	nQ5A, Q5A	Output		Differential output pair. LVDS interface levels.
13, 24, 37, 48	V_{DDO}	Power		Output supply pins.
14, 23, 38, 47	GND	Power		Power supply ground.
15, 22, 39, 46	V_{DD}	Power		Core supply pins.
16	CLK0	Input	Pulldown	Non-inverting differential clock input.
17	nCLK0	Input	Pullup	Inverting differential clock input.
18, 19	Q0A, nQ0A	Output		Differential output pair. LVDS interface levels.
20, 21	nQ0B, Q0B	Output		Differential output pair. LVDS interface levels.
25, 26	Q1A, nQ1A	Output		Differential output pair. LVDS interface levels.
27, 28	nQ1B, Q1B	Output		Differential output pair. LVDS interface levels.
29	nCLK1	Input	Pullup	Inverting differential clock input.
30	CLK1	Input	Pulldown	Non-inverting differential clock input.
31	CLK2	Input	Pulldown	Non-inverting differential clock input.
32	nCLK2	Input	Pullup	Inverting differential clock input.
33, 34	Q2B, nQ2B	Output		Differential output pair. LVDS interface levels.
35, 36	nQ2A, Q2A	Output		Differential output pair. LVDS interface levels.
40, 41	Q3B, nQ3B	Output		Differential output pair. LVDS interface levels.
42, 43	nQ3A, Q3A	Output		Differential output pair. LVDS interface levels.
44	nCLK3	Input	Pullup	Inverting differential clock input.
45	CLK3	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Capacitance Power Dissipation			1		pF

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLKx	nCLKx	Q0A:Q5A, Q0B:Q5B	nQ0A:nQ5A, nQ5B:nQ5B		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				22	mA
I_{DDO}	Output Supply Current				18	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKx	$V_{IN} = V_{DD}$ = 3.465V			150	µA
		nCLKx	$V_{IN} = V_{DD}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLKx	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLKx	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Voltage Range			0.5		V_{DD} - 0.85	V

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 85°C

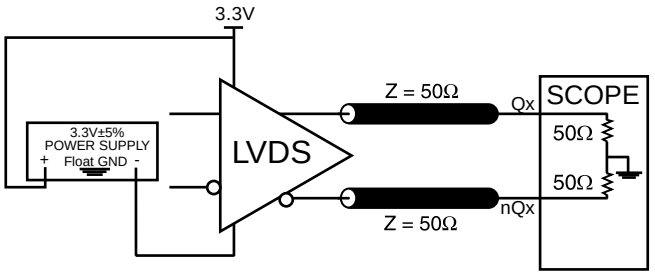
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		175	275	375	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.0	1.3	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV
I_{OFF}	Power Off Leakage		-1		+1	µA
I_{OSD}	Differential Output Short Circuit Current				-5.5	mA
I_{OS}/I_{OSB}	Output Short Circuit Current				-12	mA

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = 0°C TO 85°C

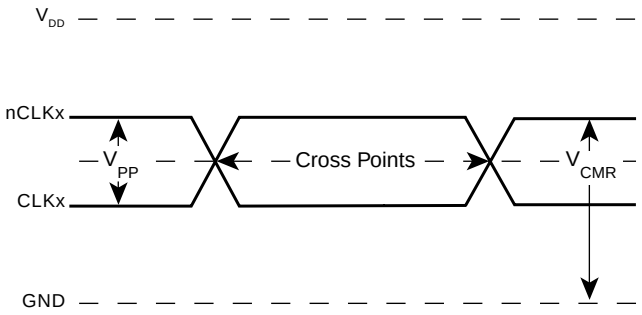
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 500MHz	1.2	1.5	1.8	ns
*t*sk(o)	Output Skew; NOTE 2, 5				250	ps
*t*sk(b)	Bank Skew; NOTE 3, 5				15	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5				500	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle	$f \leq$ 300MHz	45	50	55	%
		300MHz < $f \leq$ 500MHz	40		60	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured from at the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 4: Defined as between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

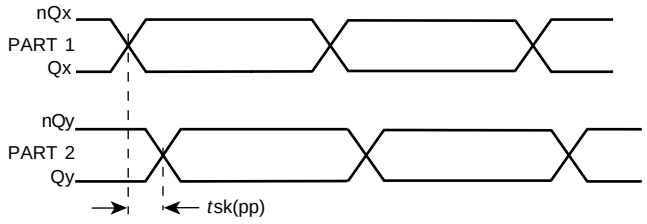
PARAMETER MEASUREMENT INFORMATION



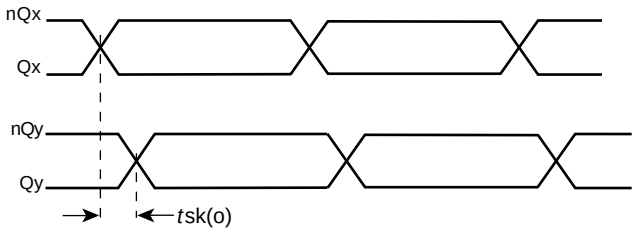
3.3V OUTPUT LOAD AC TEST CIRCUIT



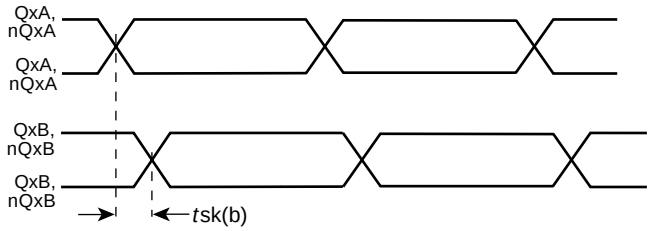
DIFFERENTIAL INPUT LEVEL



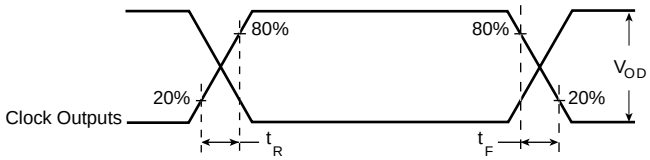
PART-TO-PART SKEW



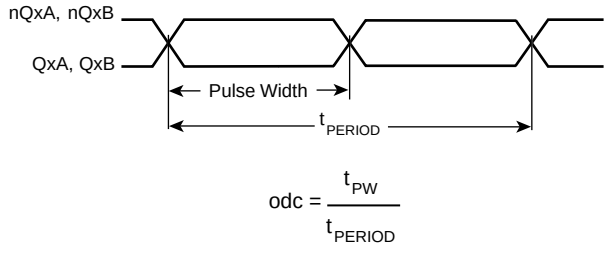
OUTPUT SKEW



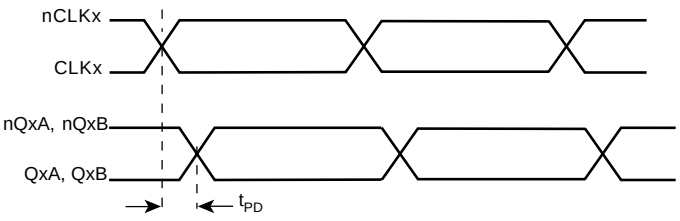
BANK SKEW



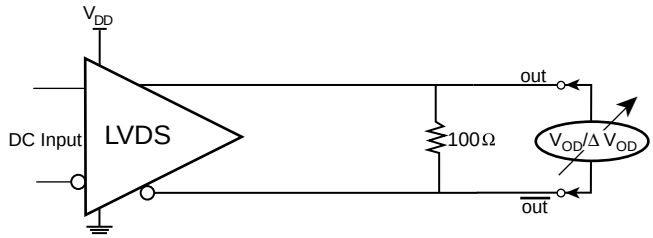
OUTPUT RISE/FALL TIME



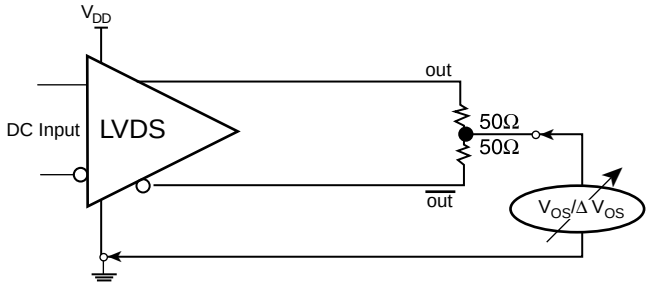
odc & t_{PERIOD}



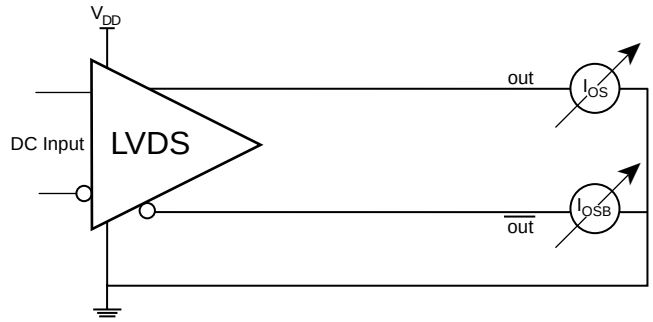
PROPAGATION DELAY



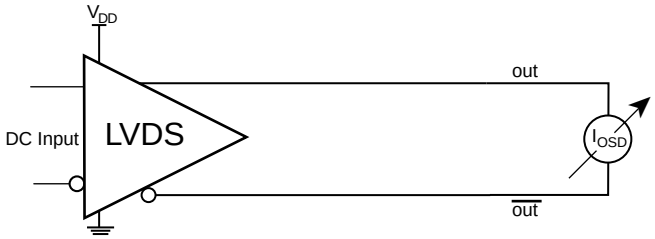
V_{OD} / ΔVOD SETUP



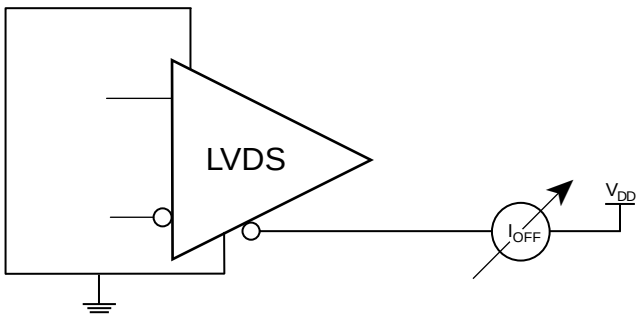
V_{OS} / ΔVOS SETUP



I_{OS} SETUP



I_{OSD} SETUP



I_{OFF} SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

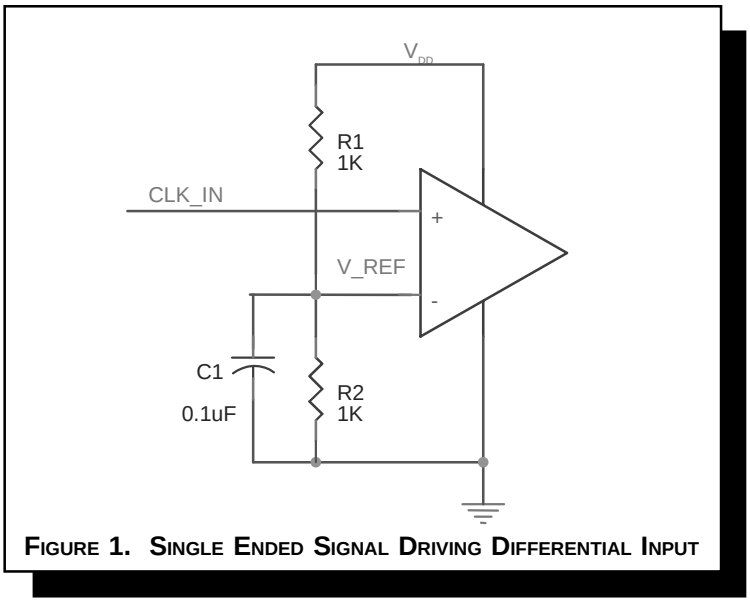


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2 to 5 show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

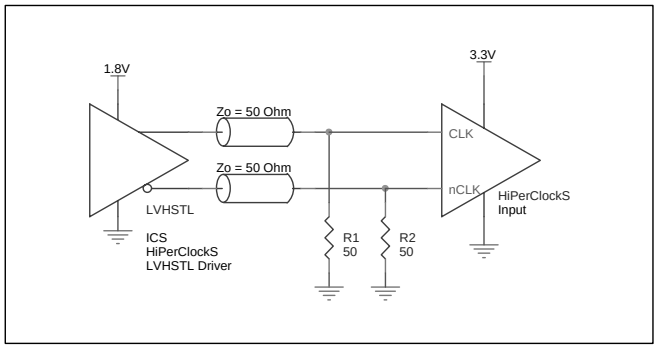


FIGURE 2. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

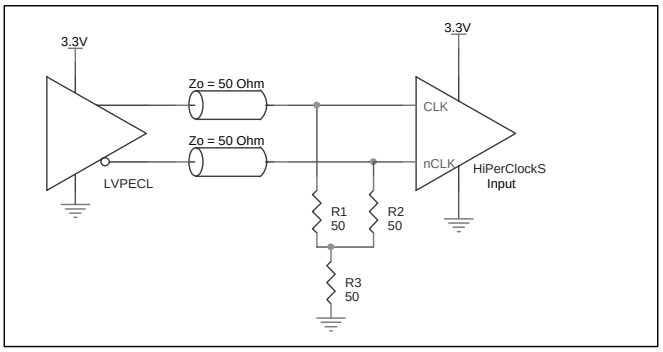


FIGURE 3. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

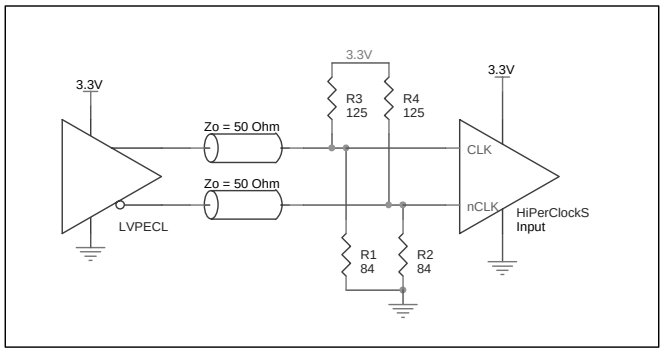


FIGURE 4. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

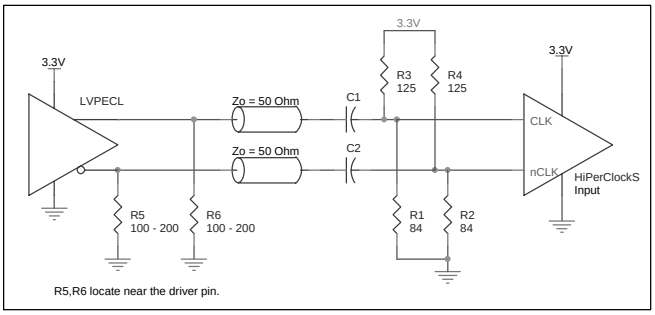


FIGURE 5. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

LVDS DRIVER TERMINATION

Figure 6 shows typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

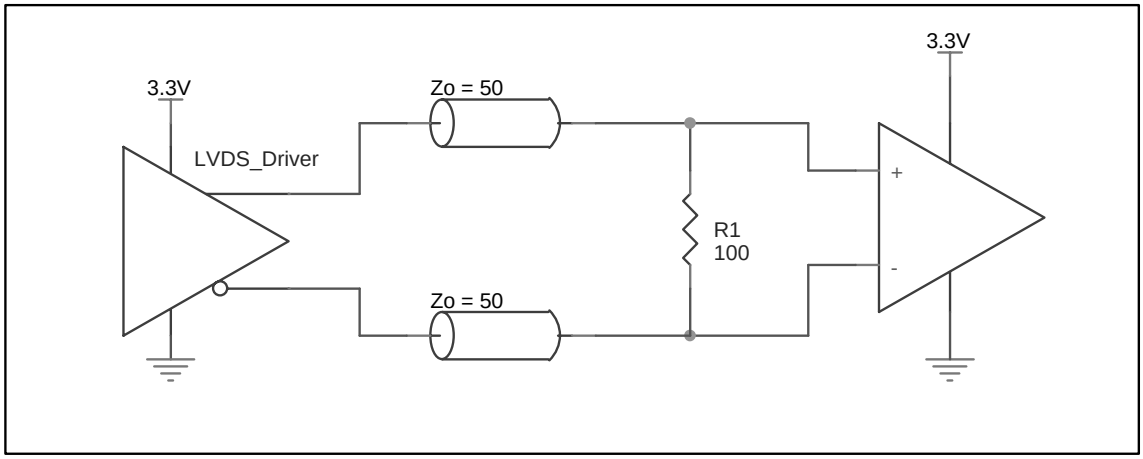


FIGURE 6. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8547 is: 1117

PACKAGE OUTLINE - Y SUFFIX

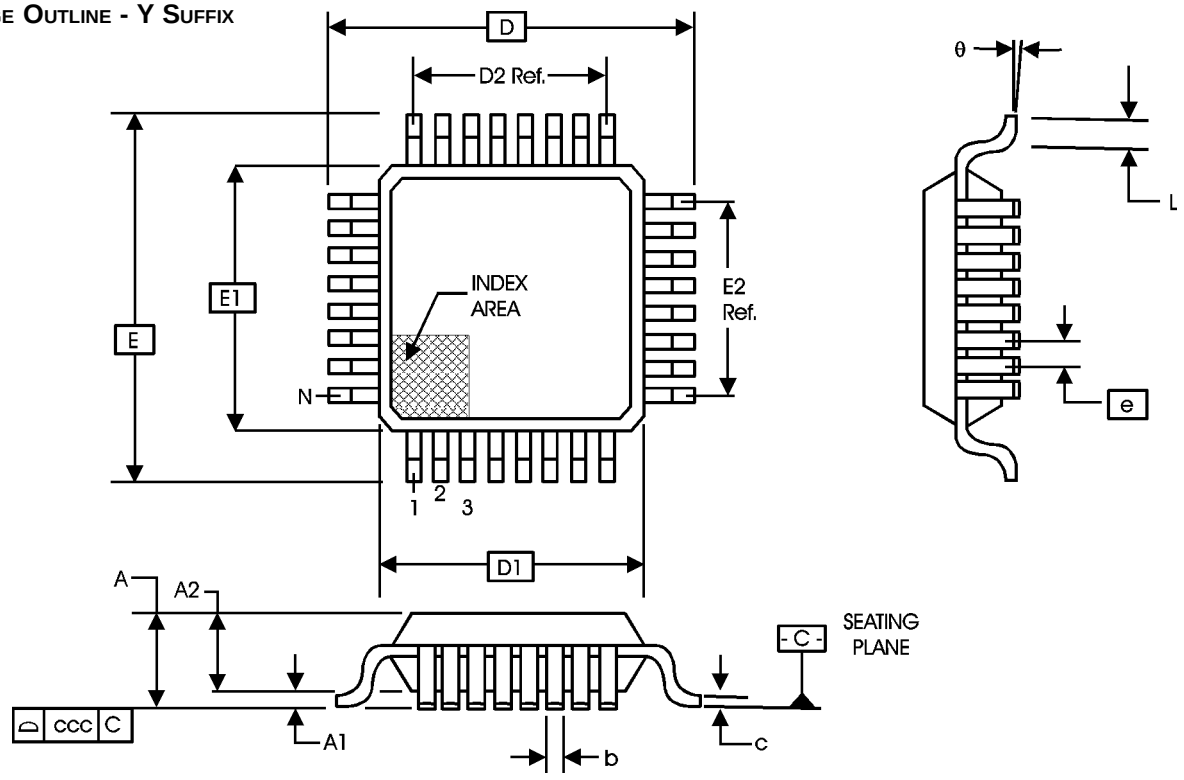


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8547AY	ICS8547AY	48 Lead LQFP	250 per tray	0°C to 85°C
ICS8547AYT	ICS8547AY	48 Lead LQFP on Tape and Reel	1000	0°C to 85°C