

# 1:18 Clock Distribution Buffer

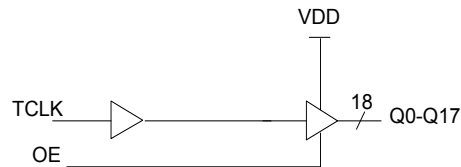
## Features

- Operational range: Up to 200 MHz
- LVCMOS/LVTTL clock input
- LVCMOS-/LVTTL-compatible logic input
- 18 clock outputs: Drive up to 36 clock lines
- Output-to-output Skew: 110 ps (typical)
- Output enable control
- Supply voltage: 2.5 V or 3.3 V
- Temperature range: Commercial and Industrial
- 32-pin LQFP package
- Pin compatible with MPC942C

## Functional Description

The CY29942 is a low voltage clock distribution buffer with an LVCMOS or LVTTL compatible clock input. The output enable control input is LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS or LVTTL compatible, operate up to 200 MHz, and can drive 50  $\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces, giving the devices an effective fanout of 1:36. Low output-to-output skews make the CY29942 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

## Logic Block Diagram



Pinouts

Figure 1. Pin Configuration

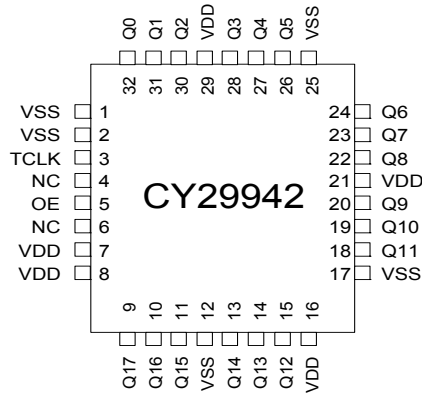


Table 1. Pin Description

Pin	Name	I/O	Description
3	TCLK	Input	<b>External reference/Test clock input.</b> Weak internal pull-down resistor.
5	OE	Input	<b>Output enable.</b> When HIGH, all outputs are enabled. When set LOW, the outputs are at high impedance. Weak internal pull-up resistor.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	Output	<b>Clock outputs</b>
7, 8, 16, 21, 29	V <sub>DD</sub>		<b>2.5 V or 3.3 V power supply</b>
1, 2, 12, 17, 25	V <sub>SS</sub>		<b>Ground</b>
4, 6	NC		<b>No connection</b>

### Absolute Maximum Ratings<sup>[1]</sup>

Maximum input voltage relative to  $V_{SS}$ :.....  $V_{SS} - 0.3\text{ V}$   
 Maximum input voltage relative to  $V_{DD}$ :.....  $V_{DD} + 0.3\text{ V}$   
 Storage temperature:.....  $-65\text{ °C}$  to  $150\text{ °C}$   
 Operating temperature: .....  $-40\text{ °C}$  to  $85\text{ °C}$   
 Maximum ESD protection.....  $2\text{ kV}$   
 Maximum power supply:.....  $5.5\text{ V}$   
 Maximum input current: .....  $\pm 20\text{ mA}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, I/O voltages should be constrained to the range:

$$V_{SS} < V_{I/O} < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

### DC Electrical Specifications

$V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$  over the specified temperature range.

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low voltage		$V_{SS}$	–	0.8	V
$V_{IH}$	Input high voltage		2.0	–	$V_{DD}$	V
$I_{IL}$	Input low current <sup>[2]</sup>		–	–	–200	$\mu\text{A}$
$I_{IH}$	Input high current <sup>[2]</sup>		–	–	200	$\mu\text{A}$
$V_{OL}$	Output low voltage <sup>[3]</sup>	$I_{OL} = 20\text{ mA}$	–	–	0.5	V
$V_{OH}$	Output high voltage <sup>[3]</sup>	$I_{OH} = -20\text{ mA}, V_{DD} = 3.3\text{ V}$	2.4	–	–	V
		$I_{OH} = -16\text{ mA}, V_{DD} = 2.5\text{ V}$	2.0	–	–	V
$I_{DDQ}$	Quiescent supply current	$OE = V_{SS}$	–	5	7	mA
$I_{DD}$	Dynamic supply current	$V_{DD} = 3.3\text{ V}$ , Outputs at 150 MHz, $CL = 15\text{ pF}$	–	285	–	mA
		$V_{DD} = 3.3\text{ V}$ , Outputs at 200 MHz, $CL = 15\text{ pF}$	–	335	–	mA
		$V_{DD} = 2.5\text{ V}$ , Outputs at 150 MHz, $CL = 15\text{ pF}$	–	200	–	mA
		$V_{DD} = 2.5\text{ V}$ , Outputs at 200 MHz, $CL = 15\text{ pF}$	–	240	–	mA
$Z_{out}$	Output impedance	$V_{DD} = 3.3\text{ V}$	8	12	16	$\Omega$
		$V_{DD} = 2.5\text{ V}$	10	15	20	$\Omega$
$C_{in}$	Input capacitance		–	4	–	pF

**Notes**

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Inputs have pull-up/pull-down resistors that effect input current.
3. Driving series or parallel terminated 50 $\Omega$  (or 50  $\Omega$  to  $V_{DD}/2$ ) transmission lines.

### AC Electrical Specifications

$V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$  over the specified temperature range<sup>[4]</sup>

Parameter	Description	Conditions	Min	Typ	Max	Unit
Fmax	Input frequency		–	–	200	MHz
tpd	TTL_CLK to Q delay <sup>[5, 6]</sup>	$V_{DD} = 3.3\text{ V}$	1.8	3.3	3.8	ns
		$V_{DD} = 2.5\text{ V}$	2.3	3.8	4.4	ns
DC	Output duty cycle <sup>[5, 6, 7]</sup>	Measured at $V_{DD}/2$	45	–	55	%
tsk(0)	Output-to-output skew <sup>[5, 6]</sup>		–	110	200	ps
tskew(pp)	Part-to-part skew <sup>[8]</sup>	$V_{DD} = 3.3\text{ V}$	–	–	1.0	ns
		$V_{DD} = 2.5\text{ V}$	–	–	1.3	ns
tskew(pp)	Part-to-part skew <sup>[9]</sup>		–	–	600	ps
tr/tf	Output clocks rise/fall time <sup>[5, 6]</sup>	0.8 V to 2.0 V, $V_{DD} = 3.3\text{ V}$ ; 0.5 V to 1.8 V, $V_{DD} = 2.5\text{ V}$	0.2	–	1.1	ns

Figure 2. LVCMOS\_CLK CY29942 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$

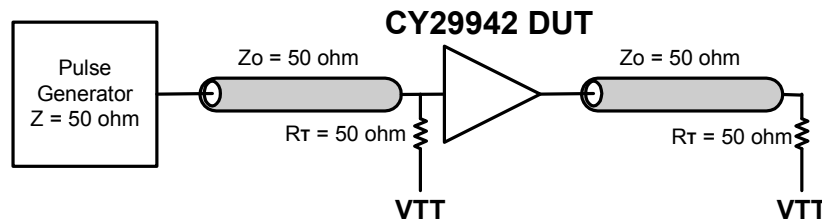
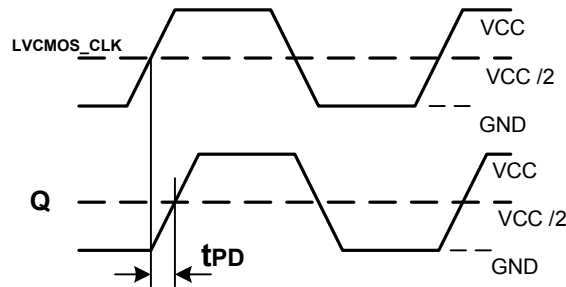


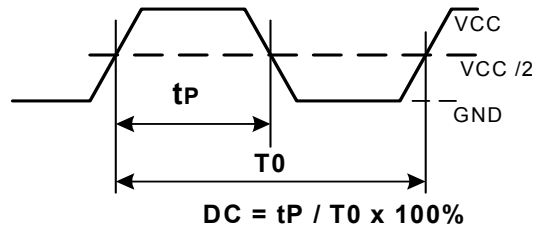
Figure 3. LVCMOS Propagation Delay (tpd) Test Reference



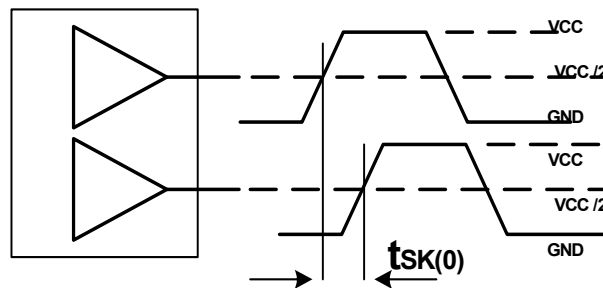
**Notes**

- 4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
- 5. Outputs driving 50Ω transmission lines.
- 6. See Figure 2.
- 7. 50% input duty cycle.
- 8. Across temperature and voltage ranges, includes output skew.
- 9. For a specific temperature and voltage, includes output skew.

**Figure 4. Output Duty Cycle (DC)**



**Figure 5. Output-to-Output Skew tsk(0)**

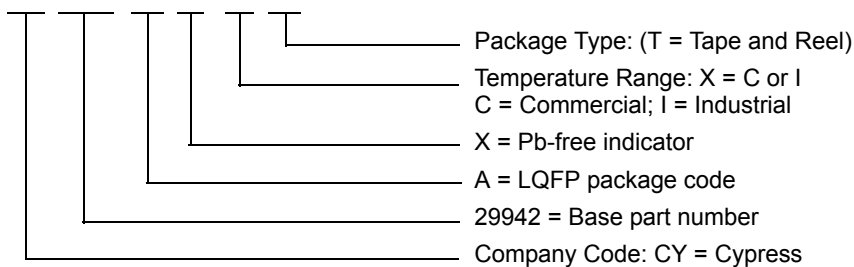


## Ordering Information

Part Number	Package Type	Production Flow
CY29942AI	32-pin LQFP	Industrial, -40 °C to 85 °C
CY29942AIT	32-pin LQFP – Tape and Reel	Industrial, -40 °C to 85 °C
<b>Pb-free</b>		
CY29942AXI	32-pin LQFP	Industrial, -40 °C to 85 °C
CY29942AXIT	32-pin LQFP – Tape and Reel	Industrial, -40 °C to 85 °C
CY29942AXC	32-pin LQFP	Commercial, 0 °C to 70 °C
CY29942AXCT	32-pin LQFP – Tape and Reel	Commercial, 0 °C to 70 °C

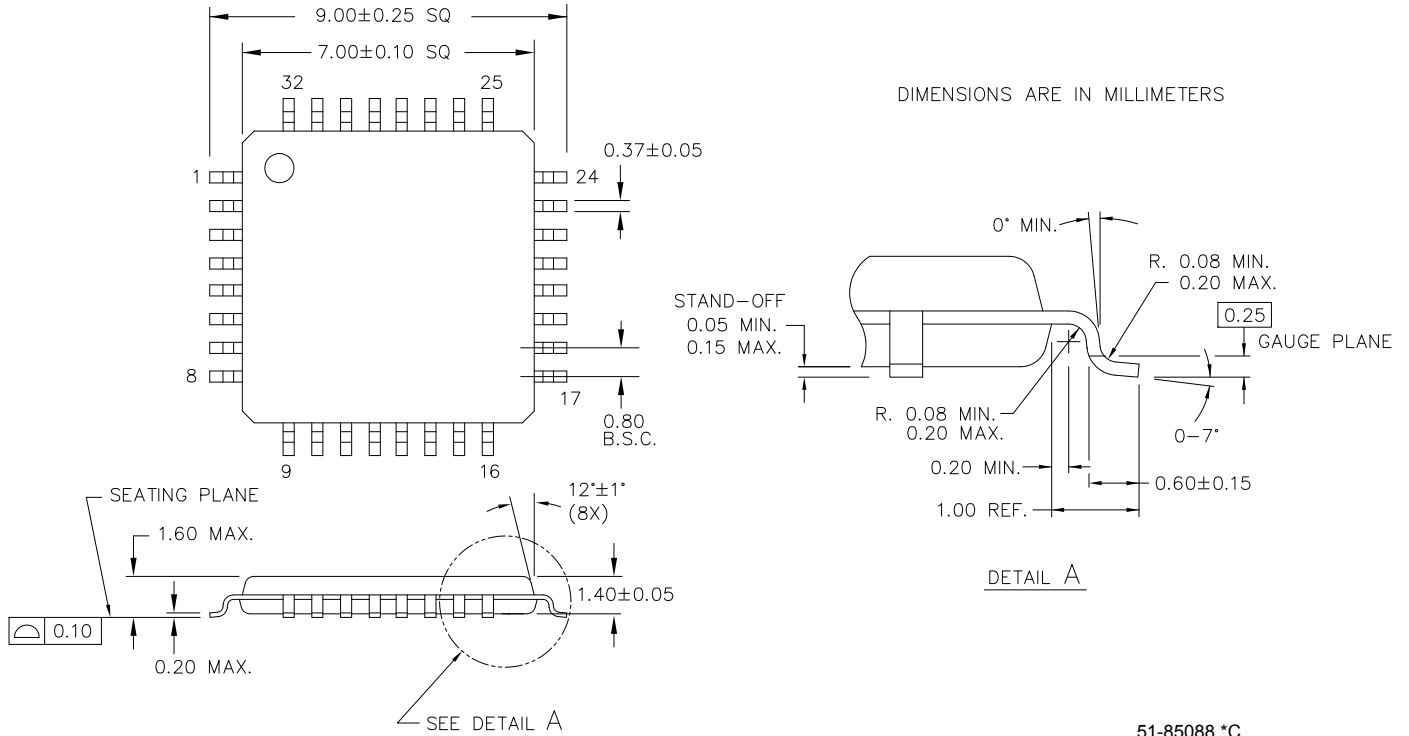
## Ordering Code Definitions

CY 29942 A X - X T



Package Drawing and Dimensions

Figure 6. 32-pin Thin Plastic Quad Flatpack 7 × 7 × 1.4 mm A32.14, 51-85088



## Acronyms

Acronym	Description
LQFP	low-profile quad flat package
LVC MOS	low voltage complementary metal oxide semiconductor
LV TTL	low voltage transistor transistor logic
OE	output enable
PLL	phase-locked loop
TQFP	thin quad flat pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Ω	ohms
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
ms	milli seconds
mW	milli Watts
ns	nano seconds
%	percent
pF	pico Farads
ps	pico seconds
V	Volts
kV	kilo Volts

Document History Page

Document Title: CY29942 1:18 Clock Distribution Buffer Document Number: 38-07284				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	111095	BRK	02/07/02	New datasheet
*A	116777	HWT	08/14/02	Added a Commercial Temp. Range in the Ordering Information
*B	122876	RBI	12/21/02	Add power up requirements to maximum rating information.
*C	334117	RGL	See ECN	Added Lead-free devices Added typical value for output-output skew
*D	2761988	KVM	09/10/09	Ordering Information table: fixed typo and removed obsolete CY29942ACT. Changed Lead-free to Pb-free.
*E	2899304	BASH/CXQ	03/25/2010	Removed CY29942AC part from Ordering Information. Updated package diagram.
*F	3034172	CXQ	09/21/2010	Changed spec title. Updated format of "Features", changed wording in "Functional Description". Removed note 1, added info into Table 1 directly. Removed reference to multiple supplies, power supply sequencing from Absolute Maximum Ratings. Removed reference to $V_{DDC}$ from AC/DC Electrical Specs tables. Added condition $OE = V_{SS}$ for $I_{DDQ}$ in DC Electrical Specs table. Fixed formatting in AC/DC Electrical specs tables. Changed $t_{SKEW}$ to $t_{SK(O)}$ to match Figure 6. Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> sections. Minor edits.



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