



GENERAL DESCRIPTION

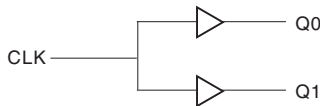


The ICS8302I is a low skew, 1-to-2 LVCMOS Fanout Buffer and a member of the HiPerClockSTM family of High Performance Clock Solutions from ICS. The ICS8302I has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTTL input levels. The ICS8302I features a pair of LVCMOS outputs. The ICS8302I is characterized at full 3.3V for input V_{DD} , and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8302I ideal for clock distribution applications demanding well defined performance and repeatability.

FEATURES

- 2 LVCMOS / LVTTTL outputs
- LVCMOS / LVTTTL clock input accepts LVCMOS or LVTTTL input levels
- Maximum output frequency: 200MHz
- Output skew: 40ps (typical)
- Part-to-part skew: 250ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V or 3.3V core, 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|-----------|---|---|-----------|
| V_{DDO} | 1 | 8 | Q0 |
| V_{DD} | 2 | 7 | GND |
| CLK | 3 | 6 | V_{DDO} |
| GND | 4 | 5 | Q1 |

ICS8302I 8-Lead SOIC

3.8mm x 4.8mm, x 1.47mm package body

M Package
Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|-----------|--------|----------|--|
| 1, 6 | V_{DDO} | Power | | Output supply pins. |
| 2 | V_{DD} | Power | | Core supply pin. |
| 3 | CLK | Input | Pulldown | LVCMOS / LVTTTL clock input. |
| 4,7 | GND | Power | | Power supply ground. |
| 5 | Q1 | Output | | Single clock output. LVCMOS / LVTTTL interface levels. |
| 8 | Q0 | Output | | Single clock output. LVCMOS / LVTTTL interface levels. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|--|-------------------------------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 4 | | pF |
| C_{PD} | Power Dissipation Capacitance (per output) | $V_{DD}, V_{DDO} = 3.465V$ | | 22 | | pF |
| | | $V_{DD} = 3.465V, V_{DDO} = 2.625V$ | | 16 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k Ω |
| R_{OUT} | Output Impedance | | | 7 | | Ω |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_i | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_o | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 112.7°C/W (0 lfm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 14 | mA |
| I_{DDO} | Output Supply Current | | | | 5 | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 14 | mA |
| I_{DDO} | Output Supply Current | | | | 5 | mA |

TABLE 3C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|---------------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 1.3 | V |
| I_{IH} | Input High Current | CLK $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | 50Ω to $V_{DDO}/2$ | 2.6 | | | V |
| | | $I_{OH} = -100\mu A$ | 2.9 | | | V |
| V_{OL} | Output Low Voltage | 50Ω to $V_{DDO}/2$ | | | 0.5 | V |
| | | $I_{OL} = 100\mu A$ | | | 0.2 | V |



TABLE 3D. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|---------------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 1.3 | V |
| I_{IH} | Input High Current | CLK $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | 50Ω to $V_{DDO}/2$ | 1.8 | | | V |
| | | $I_{OH} = -100\mu A$ | 2.2 | | | V |
| V_{OL} | Output Low Voltage | 50Ω to $V_{DDO}/2$ | | | 0.5 | V |
| | | $I_{OL} = 100\mu A$ | | | 0.2 | V |

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|--|--------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 200 | MHz |
| tp_{LH} | Propagation Delay, Low-to-High; NOTE 1 | $f \leq 200MHz$ | 1.9 | 2.35 | 2.8 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | 40 | 105 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | 250 | 800 | ps |
| t_R | Output Rise Time | 20% to 80% | 300 | | 800 | ps |
| t_F | Output Fall Time | 20% to 80% | 300 | | 800 | ps |
| odc | Output Duty Cycle | $f \leq 133MHz$ | 45 | | 55 | % |
| | | $133MHz < f \leq 200MHz$ | 40 | | 60 | % |

Parameters measured at f_{MAX} unless otherwise noted.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

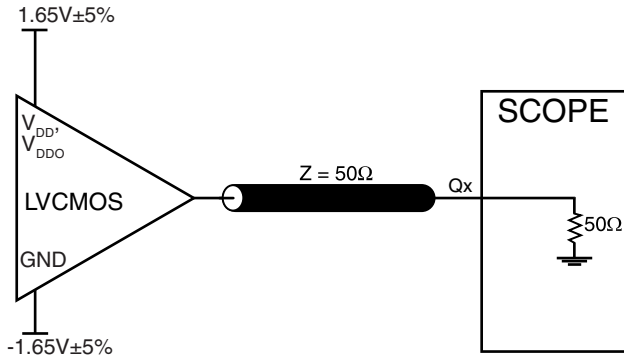
TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|--|--------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 200 | MHz |
| tp_{LH} | Propagation Delay, Low-to-High; NOTE 1 | $f \leq 200MHz$ | 2.3 | | 3.3 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 110 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | 250 | 800 | ps |
| t_R | Output Rise Time | 20% to 80% | 250 | | 650 | ps |
| t_F | Output Fall Time | 20% to 80% | 250 | | 650 | ps |
| odc | Output Duty Cycle | $f \leq 133MHz$ | 45 | | 55 | % |
| | | $133MHz < f \leq 200MHz$ | 40 | | 60 | % |

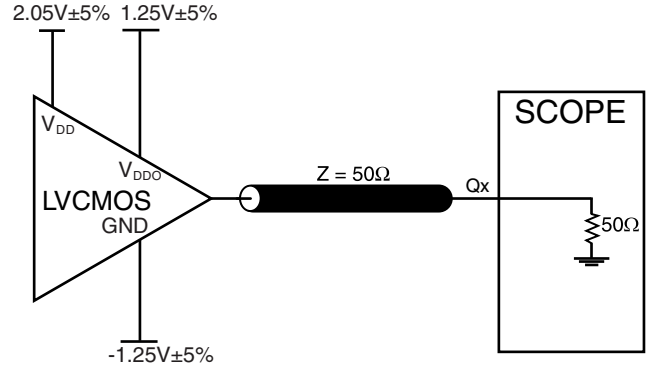
See Table 4A above for notes.



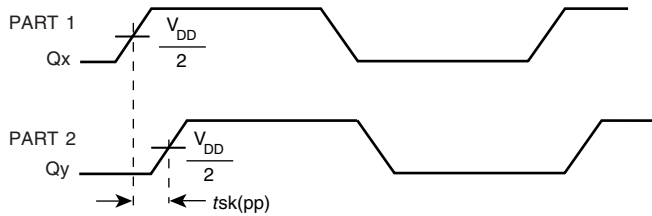
PARAMETER MEASUREMENT INFORMATION



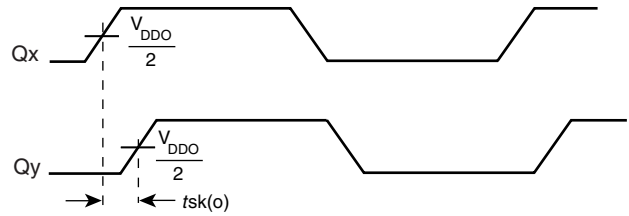
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



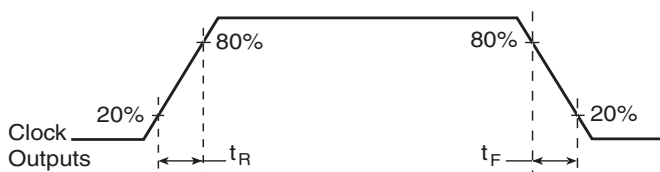
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



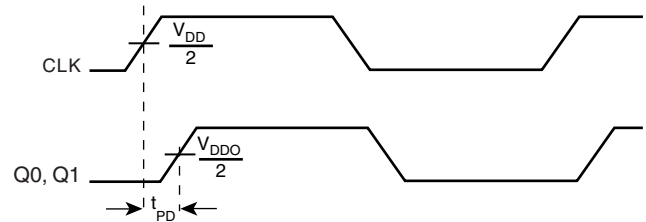
PART-TO-PART SKEW



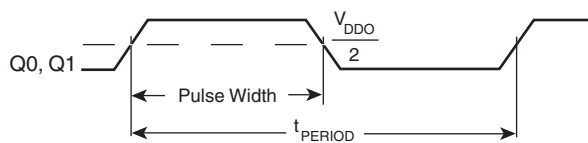
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8302I is: 322



PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

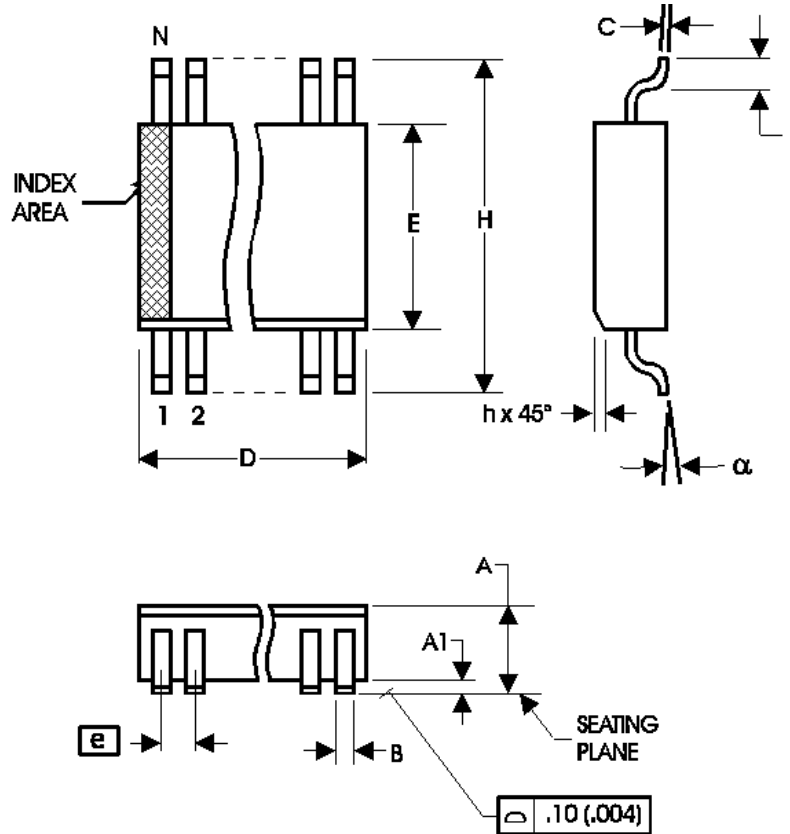


TABLE 6. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|--------|-------------|---------|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012



Integrated
Circuit
Systems, Inc.

ICS8302I
LOW SKEW, 1-TO-2
LVCMOS / LVTTTL FANOUT BUFFER

TABLE 7. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|-------------------------|--------------------|---------------|
| 8302AMI | 8302AMI | 8 lead SOIC | tube | -40°C to 85°C |
| 8302AMIT | 8302AMI | 8 lead SOIC | 2500 tape & reel | -40°C to 85°C |
| 8302AMILF | 8302AMIL | 8 lead "Lead-Free" SOIC | tube | -40°C to 85°C |
| 8302AMILFT | 8302AMIL | 8 lead "Lead-Free" SOIC | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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ICS8302I
LOW SKEW, 1-TO-2
LVCMOS / LVTTTL FANOUT BUFFER

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|--------|---|---------|
| Rev | Table | Page | Description of Change | Date |
| A | T7 | 1 8 | Features Section - added Lead-Free bullet. Ordering Information Table - added Lead-Free part number. | 3/24/05 |
| | | | | |
| | | | | |