18 Output PCIe G2/QPI Differential Buffer with 2:1 input mux

ICS9EX21801A

Description

The **ICS9EX21801** provides 18 output clocks for PCIe Gen2 (100MHz) or QPI (133MHz) applications. The **9EX21801** has 4 selectable SMBus addresses, and dedicated CKPWRGD/PD# and VDDA pins for easy board design. A differential CPU clock from a CK410B+ main clock generator, such as the **ICS932S421**, drives the **ICS9EX21801**. In fanout mode, the **9EX21801** provides outputs up to 400MHz.

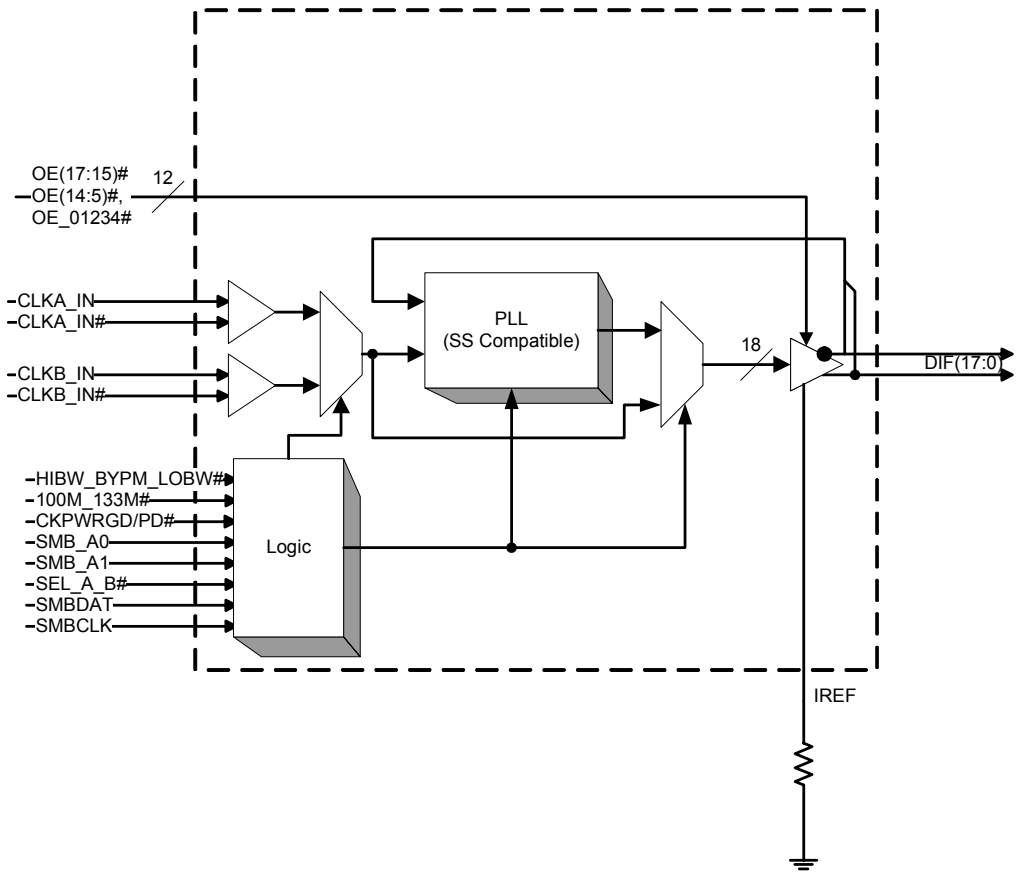
Features/Benefits

- Supports output clock frequencies up to 400 MHz
- 4 Selectable SMBus addresses
- SMBus address is independent of PLL operating mode
- Dedicated CKPWRGD/PD# and VDDA pins ease board design

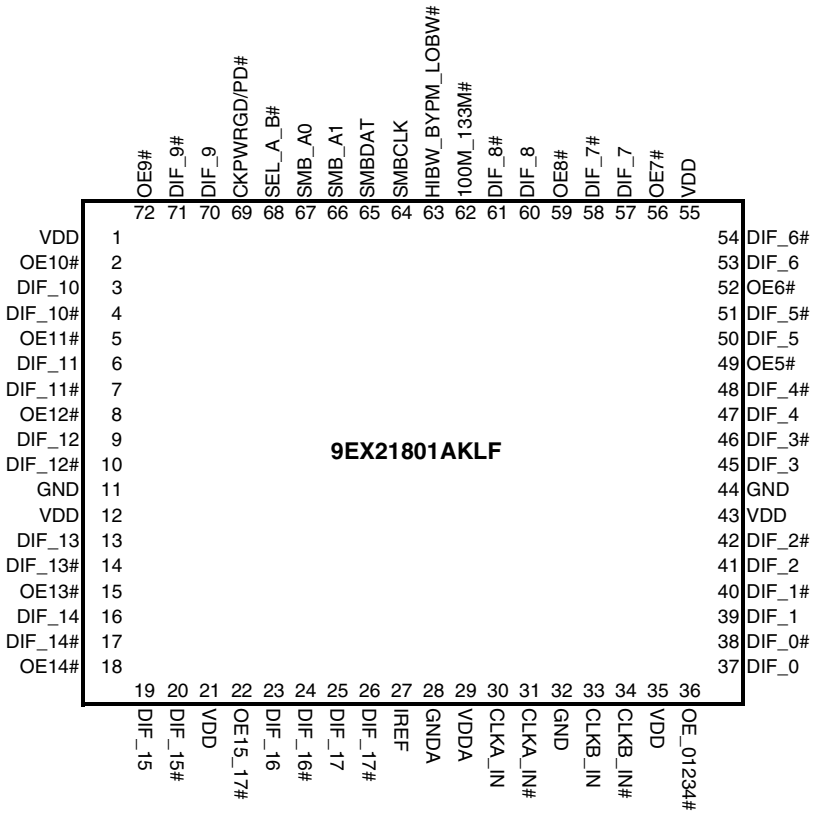
Key Specifications

- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 150 ps
- PCIe Gen2 compliant phase noise
- QPI 133MHz compliant phase noise

Funtional Block Diagram



Pin Configuration



72-pin MLF

Frequency/Functionality Table

Byte 0, bit 2 (100_133M# Latch)	Byte 0, bit 1 FSB	Byte 0, bit 0 FSA	Input MHz	DIF_x MHz	Notes
1	**0**	**1**	**100.00**	**100.00**	1
0	**0**	**1**	**133.33**	**133.33**	1
0	1	1	166.67	166.67	2
0	1	0	200.00	200.00	2
0	0	0	266.67	266.67	2
1	0	0	333.33	333.33	2
1	1	0	400.00	400.00	2
1	1	1	Reserved		

Notes:100M_133M#
1. Latch selects between 100 and 133 MHz.
   This is equivalent to FSC in CK410B+/CK509B FS table.
2. Writing Byte 0 bits (2:0) can select other frequencies.
   These frequencies are not characterized in PLL Mode

HIBW_BYPM_LOBW# Selection (Pin 63)

State	Voltage	Mode
Low	<0.8V	Low BW
Mid	1.2<Vin<1.8V	Bypass
High	Vin > 2.0V	High BW

Power Groups

Pin Number		Description
VDD	GND	
29	28	Main PLL, Analog
1,12,21,35,43,55	11,32,44	DIF clocks

Power Down Functionality

INPUTS		OUTPUTS	PLL State
CKPWRGD/PD#	Input	DIF_x	
1	Running	Running	ON
0	X	Hi-Z	OFF

SMBus Address Selection (pins 66, 67)

SMB_A1	SMB_A0	Address
0	0	D4
0	1	D6
1	0	D8
1	1	DA

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	OE10#	IN	Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs
3	DIF_10	OUT	0.7V differential true clock output
4	DIF_10#	OUT	0.7V differential complement clock output
5	OE11#	IN	Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs
6	DIF_11	OUT	0.7V differential true clock output
7	DIF_11#	OUT	0.7V differential complement clock output
8	OE12#	IN	Active low input for enabling DIF pair 12. 1 = tri-state outputs, 0 = enable outputs
9	DIF_12	OUT	0.7V differential true clock output
10	DIF_12#	OUT	0.7V differential complement clock output
11	GND	PWR	Ground pin.
12	VDD	PWR	Power supply, nominal 3.3V
13	DIF_13	OUT	0.7V differential true clock output
14	DIF_13#	OUT	0.7V differential complement clock output
15	OE13#	IN	Active low input for enabling DIF pair 13. 1 = tri-state outputs, 0 = enable outputs
16	DIF_14	OUT	0.7V differential true clock output
17	DIF_14#	OUT	0.7V differential complement clock output
18	OE14#	IN	Active low input for enabling DIF pair 14. 1 = tri-state outputs, 0 = enable outputs
19	DIF_15	OUT	0.7V differential true clock output
20	DIF_15#	OUT	0.7V differential complement clock output
21	VDD	PWR	Power supply, nominal 3.3V
22	OE15_17#	IN	Active low input for enabling DIF pairs 15, 16 and 17 1 = tri-state outputs, 0 = enable outputs
23	DIF_16	OUT	0.7V differential true clock output
24	DIF_16#	OUT	0.7V differential complement clock output
25	DIF_17	OUT	0.7V differential true clock output
26	DIF_17#	OUT	0.7V differential complement clock output
27	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
28	GNDA	PWR	Ground pin for the PLL core.
29	VDDA	PWR	3.3V power for the PLL core.
30	CLKA_IN	IN	True Input for differential reference clock.
31	CLKA_IN#	IN	Complement Input for differential reference clock.
32	GND	PWR	Ground pin.
33	CLKB_IN	IN	True Input for differential reference clock.
34	CLKB_IN#	IN	Complement Input for differential reference clock.
35	VDD	PWR	Power supply, nominal 3.3V
36	OE_01234#	IN	Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 = tri-state outputs, 0 = enable outputs

Pin Description (continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	DIF_0	OUT	0.7V differential true clock output
38	DIF_0#	OUT	0.7V differential complement clock output
39	DIF_1	OUT	0.7V differential true clock output
40	DIF_1#	OUT	0.7V differential complement clock output
41	DIF_2	OUT	0.7V differential true clock output
42	DIF_2#	OUT	0.7V differential complement clock output
43	VDD	PWR	Power supply, nominal 3.3V
44	GND	PWR	Ground pin.
45	DIF_3	OUT	0.7V differential true clock output
46	DIF_3#	OUT	0.7V differential complement clock output
47	DIF_4	OUT	0.7V differential true clock output
48	DIF_4#	OUT	0.7V differential complement clock output
49	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
50	DIF_5	OUT	0.7V differential true clock output
51	DIF_5#	OUT	0.7V differential complement clock output
52	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
53	DIF_6	OUT	0.7V differential true clock output
54	DIF_6#	OUT	0.7V differential complement clock output
55	VDD	PWR	Power supply, nominal 3.3V
56	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
57	DIF_7	OUT	0.7V differential true clock output
58	DIF_7#	OUT	0.7V differential complement clock output
59	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
60	DIF_8	OUT	0.7V differential true clock output
61	DIF_8#	OUT	0.7V differential complement clock output
62	100M_133M#	IN	Input to select operating frequency 0 = 133MHz (QPI), 1 = 100.00MHz (PCIe Gen2)
63	HIBW_BYPM_LOBW#	IN	Trilevel input to select High BW, Bypass Mode or Low BW. 0 = Low BW Mode, Mid= Bypass Mode, 1 = High Bandwidth
64	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
65	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
66	SMB_A1	IN	SMBus address bit 1
67	SMB_A0	IN	SMBus address bit 0 (LSB)
68	SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. 0 = Input B selected, 1 = Input A selected.
69	CKPWRGD/PD#	IN	Notifies the clock to sample latched inputs on the rising edge, and to power down on the falling edge.
70	DIF_9	OUT	0.7V differential true clock output
71	DIF_9#	OUT	0.7V differential complement clock output
72	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A		GND - 0.5		V_{DD} + 0.5	V	1
3.3V Logic Supply Voltage	VDD		GND - 0.5		V_{DD} + 0.5	V	1
Storage Temperature	Ts		-65		150	°C	1
Ambient Operating Temp	Tambient		0		70	°C	1
Case Temperature	Tcase				115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	3.3 V +/-5%	GND - 0.3		0.8	V	
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	
Digital Supply Current	$I_{DD3.3D}$	Full Active, C_L = Full load;			450	mA	1
Analog Supply Current	$I_{DD3.3A}$	Full Active, C_L = Full load;			40	mA	1
Digital Powerdown Current	$I_{DD3.3DPD}$	all differential pairs tri-stated			15	mA	1
Analog Powerdown Current	$I_{DD3.3APD}$	all differential pairs tri-stated			20	mA	1
Input Frequency	F_{iPLL}	PLL Mode	80		150	MHz	1
	$F_{iBYPASS}$	Bypass Mode	33		400	MHz	1
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1
Allowable Spread Modulation Frequency	f_{MOD}	Triangular Modulation	30		33	kHz	1,3
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,2
Tdrive_PD	t_{DRVPD}	DIF output enable after PD de-assertion			300	us	1,2
Tfall	t_F	Fall time of OE#			5	ns	1
Trise	t_R	Rise time of OE#			5	ns	

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Time from deassertion until outputs are >200 mV

[3]For which spread spectrum tracking error spec will be met.

Electrical Characteristics - Clock Input Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - DIF 0.7V Current Mode Differential Pairs

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, R_{REF}=475Ω, 10 inch transmission lines

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode			50	ps	1,5
		BYPASS mode as additive jitter			50	ps	1,4

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK509B accuracy requirements. The 9EX21801 itself does not contribute to ppm error.

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Applies to Bypass Mode Only

Electrical Characteristics - Skew and Differential Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

Group	Parameter	Description	Min	TYP	Max	Units	Notes
CLK_IN, DIF[x:0]	$t_{SPO\_PLL100M}$	Input-to-Output Skew in PLL mode (1:1 only), nominal value @ 25°C, 3.3V, 100MHz	950	1000	1125	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	$t_{SPO\_PLL133M}$	Input-to-Output Skew in PLL mode (1:1 only), nominal value @ 25°C, 3.3V, 133MHz	1100	1125	1175	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode (1:1 only), nominal value @ 25°C, 3.3V	4	4.7	5.2	ns	1,2,3,5
CLK_IN, DIF [x:0]	Δt_{SPO_PLL}	Input-to-Output Skew Variation in PLL mode (over specified voltage / temperature operating ranges)		|250|	|350|	ps	1,2,4,5,6, 10
CLK_IN, DIF [x:0]	Δt_{PD_BYP}	Input-to-Output Skew Variation in Bypass mode (over specified voltage / temperature operating ranges)		|800|	|900|	ps	1,2,3,4,5, 6,10
DIF[17:0]	t_{SKEW_A19}	Output-to-Output Skew across all 18 outputs (Common to Bypass and PLL mode - all outputs at same gear)		100	150	ps	1,2,3
DIF[17:0]	t_{JPH}	Differential Phase Jitter (RMS Value)		2	10	ps	1,4,7
DIF[17:0]	$t_{SSTERROR}$	Differential Spread Spectrum Tracking Error (peak to peak)		20	80	ps	1,4,9

NOTES:

1. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point
3. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
4. This parameter is deterministic for a given device
5. Measured with scope averaging on to find mean value.
6. Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.
7. This parameter is measured at the outputs of two separate ICS9EX21801 devices driven by a single CK410B+. The ICS9EX21801's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22Mhz and 11-33Mhz.
8. t is the period of the input clock
9. Differential spread spectrum tracking error is the difference in spread spectrum tracking between two ICS9EX21801 devices This parameter is measured at the outputs of two separate ICS9EX21801 devices driven by a single CK410B+ in Spread Spectrum mode. The ICS9EX21801's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33KHz modulation frequency, linear profile.
10. This parameter is an absolute value. It is not a double-sided figure.

Electrical Characteristics - Phase Jitter (PLL Mode)

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP.	MAX	UNITS	NOTES
PLL Bandwidth	BWH	High Bandwidth Selected	2	3	4	MHz	
PLL Bandwidth	BWL	Low Bandwidth Selected	0.7	1	2	MHz	
PLL Jitter Peaking	jPKH	High Bandwidth Selected		2.5	3	dB	
PLL Jitter Peaking	jPKL	Low Bandwidth Selected		2	2.5	dB	
Jitter, Phase	tjphase_LoBW	PCIe Gen 1 (1.5 - 22 MHz)		36/42	108	ps	1,2
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Lo-band content (10kHz to 1.5MHz)		1.1/1.2	3	ps rms	1,2
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Hi-band content (1.5MHz to Nyquist)		2.0/2.1	3.1	ps rms	1,2
		QPI_133MHz (4.8Gb, 12 UI)		0.24/0.25	0.5	ps rms	2, 3
		QPI_133MHz (6.4Gb, 12 UI)		0.18/0.19	0.5	ps rms	2, 3
	tjphase_HIBW	PCIe Gen 1 (1.5 - 22 MHz)		28/32	86	ps	1,2
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Lo-band content (10kHz to 1.5MHz)		1.2/1.5	3	ps rms	1,2
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Hi-band content (1.5MHz to Nyquist)		2.6/2.7	3.1	ps rms	1,2
		QPI_133MHz (4.8Gb, 12 UI)		0.27/0.28	0.5	ps rms	2, 3
		QPI_133MHz (6.4Gb, 12 UI)		0.2/0.21	0.5	ps rms	2, 3

Notes on Phase Jitter: (Guaranteed by design and characterization, not tested in production)

[1] See http://www.pcisig.com for complete specs. First number is Spread Spectrum Off, second is Spread Spectrum On.

[2] Device driven by IDT CK410B+ (932S421CGLF) or CK509B (932S509EKLF) or equivalent

[3] Calculated from Intel Supplied Clock Jitter Tool 1.5.1. First number is Spread Spectrum Off, second is Spread Spectrum On

General SMBus serial interface information for the ICS9EX21801A

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D4_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D5_{(h)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

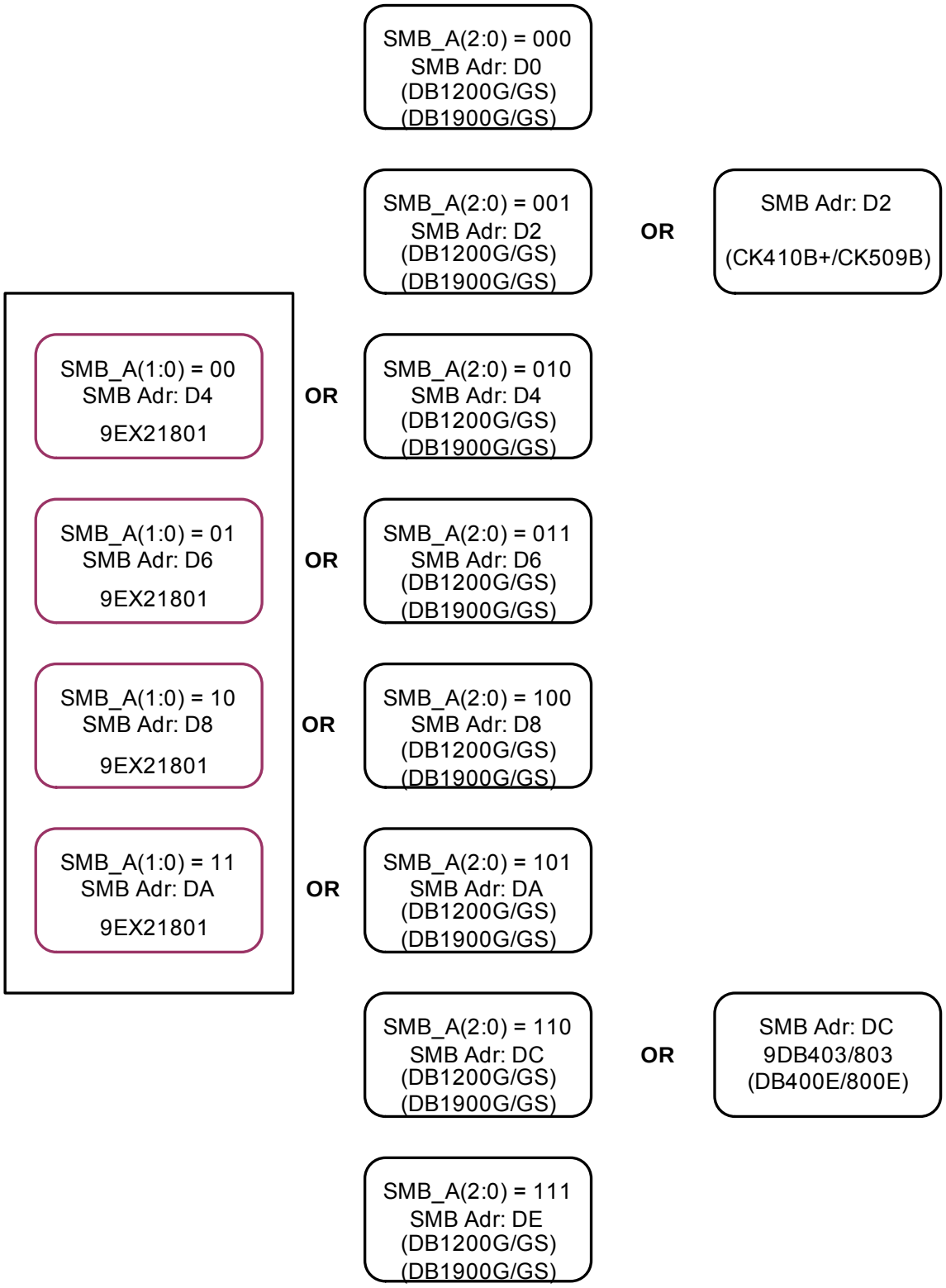
Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D4_{(h)}$*			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D4_{(h)}$*			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D5_{(h)}$*			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Note: The address is selectable among 4 values (page 2).

9EX21801 SMBus Addressing



SMBusTable: Output, and PLL BW Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	4	PLL_BW# adjust		RW	00 = Low BW (1MHz) 10 = Bypass 11 = High BW (3MHz)		Latch
Bit 6		BYPASS# test mode / PLL		RW			Latch
Bit 5		DIF_17	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_16	Output Control	RW	Hi-Z	Enable	1
Bit 3		RESERVED					0
Bit 2	-	100M_133M#	Frequency Select Bit C	RW	133MHz	100MHz	Latch
Bit 1	-	FSB	Frequency Select Bit B	RW	See Frequency Select Table		0
Bit 0	-	FSA	Frequency Select bit A	RW			1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		DIF_15	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_14	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_13	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_12	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_8	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	5	OE11# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 6	2	OE10# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 5	72	OE9# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 4	59	OE8# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 3	56	OE7# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 2	52	OE6# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 1	49	OE5# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 0	36	OE_01234# Input	Pin Readback	R	Pin Low	Pin Hi	X

SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5	62	100M_133M# Input	Pin Readback	R	133M	100M	X
Bit 4	68	SEL_A_B# Input	Pin Readback	R	Input B	Input A	X
Bit 3	22	OE15_17# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 2	18	OE14# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 1	15	OE13# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 0	8	OE12# Input	Pin Readback	R	Pin Low	Pin Hi	X

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBusTable: Vendor & Revision ID Register

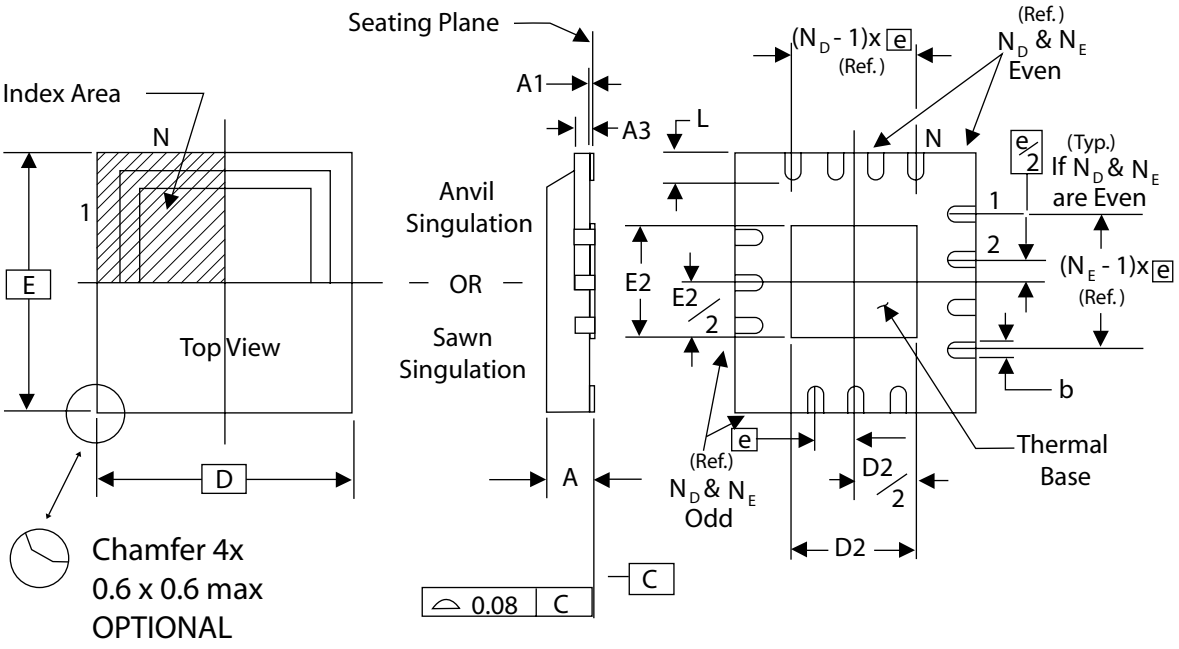
Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		R	Device ID is 18 hex		0
Bit 6	-	Device ID 6		R			0
Bit 5	-	Device ID 5		R			0
Bit 4	-	Device ID 4		R			1
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			0
Bit 0	-	Device ID 0		R			0

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	72L
N	72
N_D	18
N_E	18

DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75	6.15
E2 MIN. / MAX.	5.75	6.15
L MIN. / MAX.	0.3	0.5

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9EX21801AKLF	Tubes	72-pin MLF	0 to +70°C
9EX21801AKLFT	Tape and Reel	72-pin MLF	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate to the datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	4/29/2008	Initial Release	-
0.2	5/1/2008	1. SMBus Bytes 11-16 are now reserved 2. SMBus References to 1:1 operating set point register are removed. 3. Updated readback registers to match new control pins 3. Added QPI phase noise spec 4. Significant changes to pinout to improve performance	Various
0.3	5/30/2008	1. Updated/Corrected SMBus, filled in empty bytes 2. Updated Frequency/Functionality Table 3. Added SMBus Address decoding table and graph 4. Corrected Power hook up table.	Various
0.4	6/3/2008	Added revision designator to orderng information	12
0.5	12/8/2008	1. Updated front page text 2. Updated Functionality foot notes on Page 2. 3. Deleted duplicate table on page 6. 4. Corrected DIF 0.7V Current Mode electrical characterisitcs - removed skew spec. 5. Updated skew and Differential Parameters Table to reflect char data, added PLL BW and jitterpeaking data to this table. 6. Updated Phase Jitter Table - removed FBD specs and added HiBW and Low BW sections 7. Added SMBus Addressing Table after page 9	1,2,6,7,8, 10
A	12/17/2008	1. Updated PLL mode input frequency range 2. Noted that Modulation frequency is the Allowable Spread Modulation Frequency. Added foonote 3. 3. Corrected PCIe Gen1 Max phase jitter spec to be 86 ps instead of 108ps. 86ps is the derated limit when using ~160K cycles to calculate the value. Released to final - Rev A.	5,8
B	1/20/2010	1. Corrected Pin Description for Pin 62. 0 = 133M, 1 = 100M.	4