PROGRAMMABLE FLEXPC CLOCK FOR P4 PROCESSOR

IDTCV126

FEATURES:

- One high precision PLL for CPU, SSC, and N programming
- One high precision PLL for SRC/PCI, SSC, and N programming
- One high precision PLL for 48MHz
- Band-gap circuit for differential outputs
- Support spread spectrum modulation, down spread 0.5% and others
- Support SMBus block read/write, index read/write
- Selectable output strength for REF, 48MHz, PCI
- Allows for CPU frequency to change to a higher frequency for maximum system computing power
- Available in SSOP and TSSOP packages

OUTPUTS:

- 4*0.7V current –mode differential CPU CLK pair
- 5*0.7V current –mode differential SRC CLK pair
- 7*PCI, 3 free running, 33.3MHz
- 1*48MHz
- 2*REF

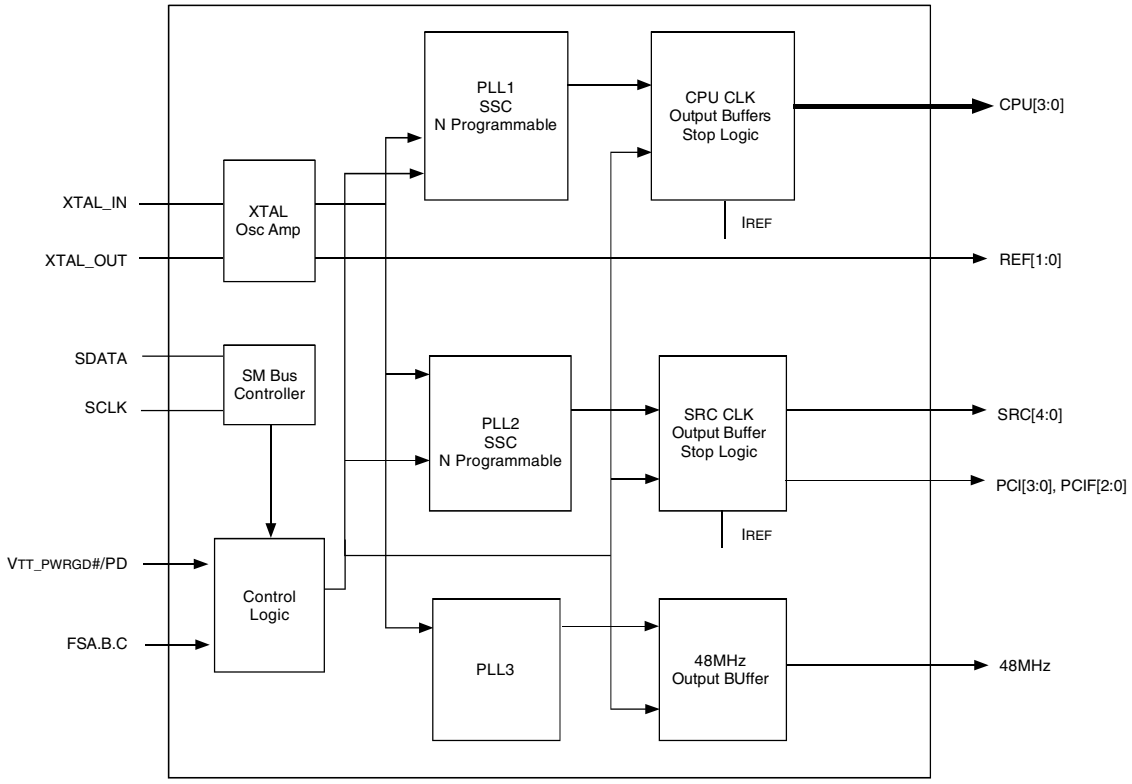
DESCRIPTION:

IDTCV126 is a 56 pin clock device. The CPU output buffer is designed to support up to 400MHz processor. This chip has three PLLs inside for CPU, SRC/PCI, and 48MHz IO clocks. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance. Each CPU and SRC/PCI has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

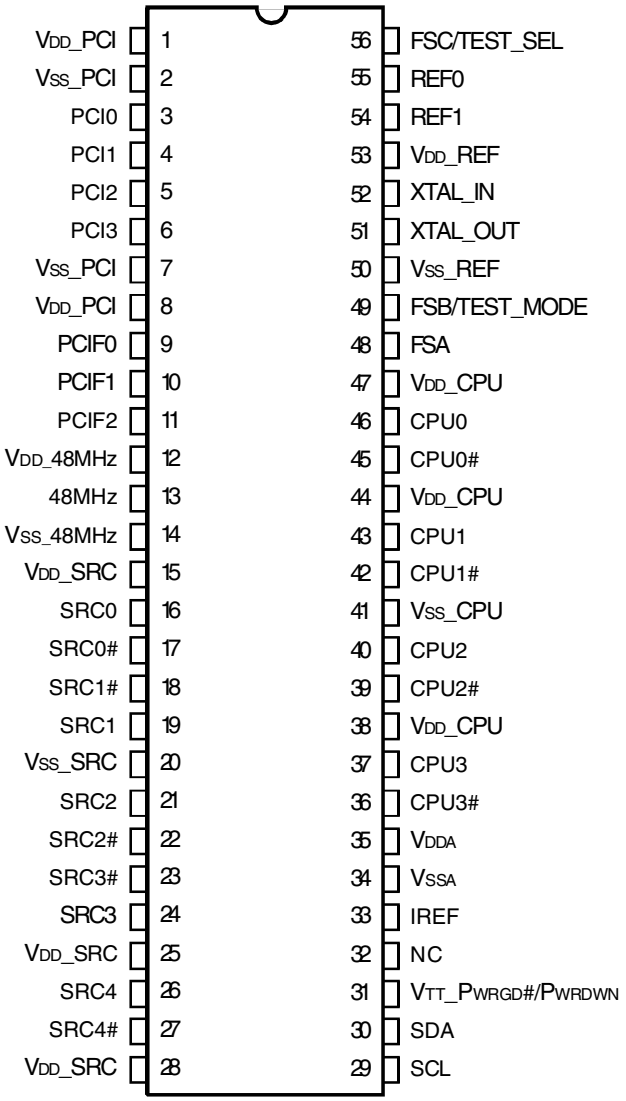
KEY SPECIFICATIONS:

- CPU/SRC CLK cycle to cycle jitter < 50ps
- PCI CLK cycle to cycle jitter < 500ps

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

CPU AND SRC SPREAD SPECTRUM MAGNITUDE CONTROL

SMC[2:0]	%
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDDIN	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	–65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin#	Pin Name	Type	Description
52	XTAL_IN	I	14.318 XTAL input
51	XTAL_OUT	O	14.318 XTAL output
54, 55	REF[1:0]	O	14.318 MHz
3-6	PCI[3:0]	O	33.33MHz PCI clock
9-11	PCIF[2:0]	O	33.33MHz PCI free running clock
13	USB48	O	48MHz
36,37,39 40,42,43 45, 46	CPU[3:0] CPU#[3:0]	O	CPU differential clock
16-19, 21-24, 26, 27	SRC[4:0] SRC#[4:0]	O	SRC differential clock
49	FSB/TEST_MODE	I	Frequency select. When in test mode, 0 = clock Hi-Z, 1 = clk REF/N
56	FSC/TEST_SEL	I	Frequency select. Select test mode if pulled to 2V and above when VTT_PWRGD# assertion.
48	FSA	I	Frequency select, sampled on VTT_PWRGD# assertion.
33	IREF	I	Reference current for differential outputs
31	VTT_PWRGD#/PD	I	3.3V LVTTL input, a level-sensitive strobe used to latch the FS_A, FS_B, FS_C/TEST_SEL inputs. After VTT_PWRGD# assertion, becomes a real-time input for asserting power down (active HIGH).
30	SDA	I/O	SMBus data
29	SCL	I	SMBus clock

FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC[7:1]	PCI	USB	REF
101	100	100	33.3	48	14.318
001	133	100	33.3	48	14.318
011	166	100	33.3	48	14.318
010	200	100	33.3	48	14.318
000	266	100	33.3	48	14.318
100	333	100	33.3	48	14.318
110	400	100	33.3	48	14.318
111	Reserved	100	33.3	48	14.318

RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

SE SIGNAL STRENGTH SELECTION

Str[1:0]	Strength
00	0.6x
01	0.8x
10	1x
11	1.2x

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 0Eh
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	SRCT0, SRCC0	Output Enable	Tristate	Enable	RW	1
1	SRCT1, SRCC1	Output Enable	Tristate	Enable	RW	1
2	SRCT2, SRCC2	Output Enable	Tristate	Enable	RW	1
3	SRCT3, SRCC3	Output Enable	Tristate	Enable	RW	1
4	SRCT4, SRCC4	Output Enable	Tristate	Enable	RW	1
5	Reserved				RW	1
6	Reserved				RW	1
7	Reserved				RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	Spread Spectrum Enable	Spread Spectrum mode enable	Spread off	Spread on	RW	0
1	CPUT0, CPUC0	Output Enable	Tristate	Enable	RW	1
2	CPUT1, CPUC1	Output Enable	Tristate	Enable	RW	1
3	Reserved				RW	1
4	CPUT2, CPUC2	Output Enable	Tristate	Enable	RW	1
5	CPUT3, CPUC3	Output Enable	Tristate	Enable	RW	1
6	REF0	Output Enable	Tristate	Enable	RW	1
7	REF1	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	USB_48	Output Enable	Disable	Enable	RW	1
1	PCIF0	Output Enable	Disable	Enable	RW	1
2	PCIF1	Output Enable	Disable	Enable	RW	1
3	PCIF2	Output Enable	Disable	Enable	RW	1
4	PCI0	Output Enable	Disable	Enable	RW	1
5	PCI1	Output Enable	Disable	Enable	RW	1
6	PCI2	Output Enable	Disable	Enable	RW	1
7	PCI3	Output Enable	Disable	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRCT0, SRCC0	Allow controlled by software PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0
1	SRCT1, SRCC1				RW	0
2	SRCT2, SRCC2				RW	0
3	SRCT3, SRCC3				RW	0
4	SRCT4, SRCC4				RW	0
5	PCIF0				RW	0
6	PCIF1				RW	0
7	PCIF2				RW	0

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPUT0, CPUC0	Allow control of CPU_0 with assertion of CPU_STOP#	Free running, not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
1	CPUT1, CPUC1	Allow control of CPU_1 with assertion of CPU_STOP#			RW	1
2	CPUT2, CPUC2	Allow control of CPU_2 with assertion of CPU_STOP#			RW	1
3	CPUT3, CPUC3	Allow control of CPU_3 with assertion of CPU_STOP#			RW	1
4	CPUT0, CPUC0	CPU PWRDWN Mode	Driven in power down	Tristate in power down	RW	0
5	CPUT1, CPUC1				RW	0
6	CPUT2, CPUC2				RW	0
7	CPUT3, CPUC3				RW	0

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPUT0	CPU0 CPU_Stop drive mode	Driven in CPU_Stop	Tristate in CPU_Stop	RW	0
1	CPUT1	CPU1 CPU_Stop drive mode	Driven in CPU_Stop	Tristate in CPU_Stop	RW	0
2	CPUT2	CPU2 CPU_Stop drive mode	Driven in CPU_Stop	Tristate in CPU_Stop	RW	0
3	CPUT3	CPU3 CPU_Stop drive mode	Driven in CPU_Stop	Tristate in CPU_Stop	RW	0
4	Reserved				RW	0
5	SRC	SRC Pwrdwn drive mode	Driven in power down	Tristate in power down	RW	0
6	SRC	PCI_STOP drive mode	Driven in PCI_Stop	Tristate in power down	RW	0
7	Reserved				RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		FSA latched value on power up			R	FSA
1		FSB latched value on power up			R	FSB
2		FSC latched value on power up			R	FSC
3	Software PCI_STOP		Stop all PCI/F and SRC except PCIF[2:0], and SRC clocks set to free running	No stop	RW	1
4	REFstr1	REF drive strength, works with Byte 12, Bit 2 (see Str table)			RW	1
5	Reserved				RW	1
6		Test mode entry control	Normal operation	Test mode, controlled by Byte 6, Bit 7	RW	0
7		Only valid when Byte 6, Bit 6 is HIGH	Hi-Z	REF/N	RW	0

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		Vendor ID			R	1
1		Vendor ID			R	0
2		Vendor ID			R	1
3		Vendor ID			R	0
4		Revision ID			R	0
5		Revision ID			R	0
6		Revision ID			R	0
7		Revision ID			R	0

BYTE 8 (BLOCK READ BYTE COUNT)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0						0
1						1
2						1
3						1
4						0
5						0
6						0
7						0

BYTE 9

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_SMC0	SSC control (see SMC table)			RW	1
1	SRC_SMC1				RW	0
2	SRC_SMC2				RW	0
3	Reserved				RW	0
4	CPU_SMC0	SSC control (see SMC table)			RW	1
5	CPU_SMC1				RW	0
6	CPU_SMC2				RW	0
7	Reserved				RW	0

BYTE 10

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On[1]
0	CPU_N0, LSB	CPU CLK = N* Resolution			RW	0
1	CPU_N1				RW	1
2	CPU_N2				RW	1
3	CPU_N3				RW	0
4	CPU_N4				RW	1
5	CPU_N5				RW	0
6	CPU_N6				RW	0
7	CPU_N7, MSB				RW	1

NOTE:
1. The default value depends on the value of frequency select signals FSA, FSB, and FSC at power-on.

BYTE 11

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_N0, LSB	CPU CLK = N* Resolution			RW	0
1	SRC_N1				RW	1
2	SRC_N2				RW	1
3	SRC_N3				RW	0
4	SRC_N4				RW	1
5	SRC_N5				RW	0
6	SRC_N6				RW	0
7	SRC_N7, MSB				RW	1

BYTE 12

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	48MHzStr0				RW	1
1	48MHStr1	USB48MHz strength selection			RW	1
2	REFStr0	Work with Byte 6 Bit 4 REFstr1 (see strength table)			RW	1
3	Reserved				RW	0
4	PCIStrC0				RW	0
5	PCIStrC1	PCI strength selection			RW	1
6	PCIFStr0				RW	0
7	PCIFStr1	PCIF strength selection			RW	1

BYTE 13

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Test_scl	On chip test mode enable	Normal	SCLK=1, CLK outputs=1 SCLK=0, CLK outputs=0	RW	0
1		N Programming enable	Disable	enable	RW	0
2	Reserved				RW	0
3	Reserved				RW	0
4		USB PLL power down	Normal	Power down	RW	0
5		SRC PLL power down	Normal	Power down	RW	0
6		CPU PLL power down	Normal	Power down	RW	0
7	Reserved				RW	0

BYTE 62 = 61h

BYTE 63 = 12h

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V_{SS} - 0.3	—	0.35	V
I_{IL}	Input LeakageCurrent	0< V_{IN} < V_{DD}, no internal pull-up or pull-down	–5	—	+5	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		XTAL_IN and XTAL_OUT pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE_PD}(2)	CPU output enable after PD de-assertion	—	—	300	us
	T_{FALL_PD}(2)	Fall time of PD	—	—	5	ns
	T_{RISE_PD}(2)	Rise time of PD	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	1150	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–300	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(2,3)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period(2,3)	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SK3}	Skew, CPU[1:0](2)	V_T = 50%	—	—	100	ps
	Skew, CPU2(2)		—	—	250	
	Skew, SRC(2)		—	—	250	
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[3:0](2)		—	—	50	ps
	Jitter, Cycle to Cycle, SRC(2)	Measurement from differential waveform	—	—	125	

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

PCI STOP FUNCTIONALITY

If PCIF (2:0) and SRC clocks are set to be free-running through SMBus programming, they will ignore the PCI_STOP register bit.

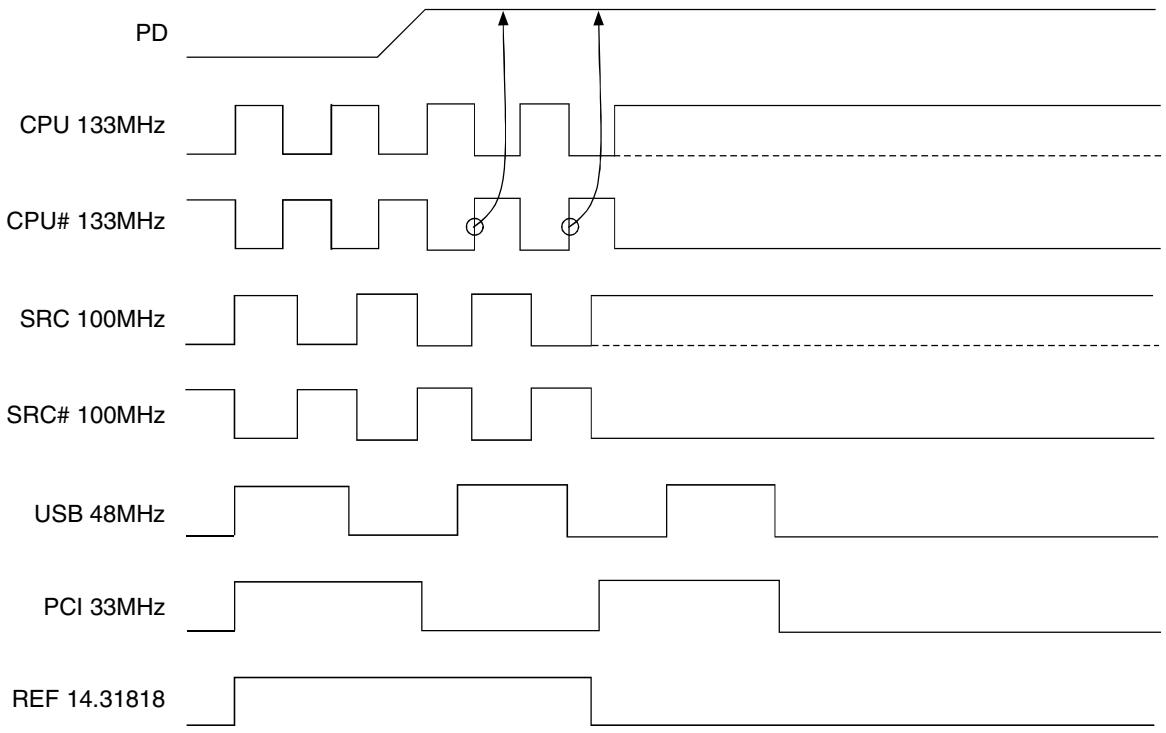
PCI_STOP (Byte 6 bit 3)	CPU	CPU#	SRC	SRC#	PCIF/PCI	48MHz	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	14.318MHz
0	Normal	Normal	I_{REF} * 6 or float	Low	Low	48MHz	14.318MHz

PD, POWER DOWN

PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

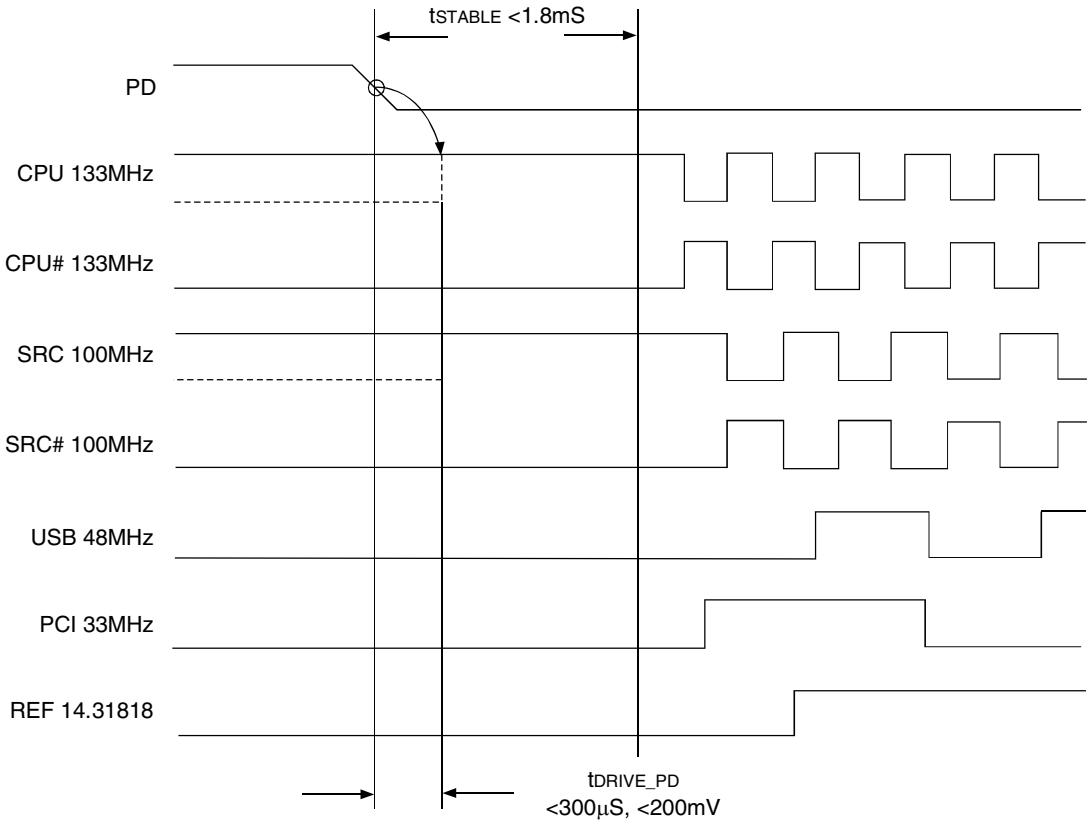
PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	I_{REF} * 2 or float	Float	I_{REF} * 2 or float	Float	Low	Low	I_{REF} * 2 or float	Float	Low

PD ASSERTION



PD DE-ASSERTION

The time from the de-assertion of PD or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD deassertion.



ORDERING INFORMATION

IDTCV XXX XX X

Device Type		
Package	PV	Small Shrink Outline Package
	PVG	SSOP - Green
	PA	Thin Shrink Small Outline Package
	PAG	TSSOP - Green
Grade	Blank	Commercial Temperature Range (0°C to +70°C)
126		Programmable FlexPC Clock for P4 Processor

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com

REVISION HISTORY

September 08, 2006	Updated CPU/SRC CLK cycle to cycle jitter specs to 50ps.
June 22, 2007	Updated PCI CLK cycle to cycle jitter specs to 500ps.