PROGRAMMABLE FLEXPC CLOCK FOR P4 PROCESSOR

IDTCV110N

FEATURES:

- **One high precision PLL for CPU, SSC, and N programming**
- **One high precision PLL for SRC/PCI/SATA, SSC, and N programming**
- **One high precision PLL for 96MHz/48MHz**
- **Band-gap circuit for differential outputs**
- **Support spread spectrum modulation, down spread 0.5%**
- **Support SMBus block read/write, index read/write**
- **Selectable output strength for REF**
- **Allows for CPU frequency to change to a higher frequency for maximum system computing power**
- **Available in SSOP package**

OUTPUTS:

- **2*0.7V current –mode differential CPU CLK pair**
- **6*0.7V current –mode differential SRC CLK pair, one dedicated for SATA**
- **One CPU_ITP/SRC selectable CLK pair**
- **9*PCI, 3 free running, 33.3MHz**
- **1*96MHz, 1*48MHz**
- **1*REF**

DESCRIPTION:

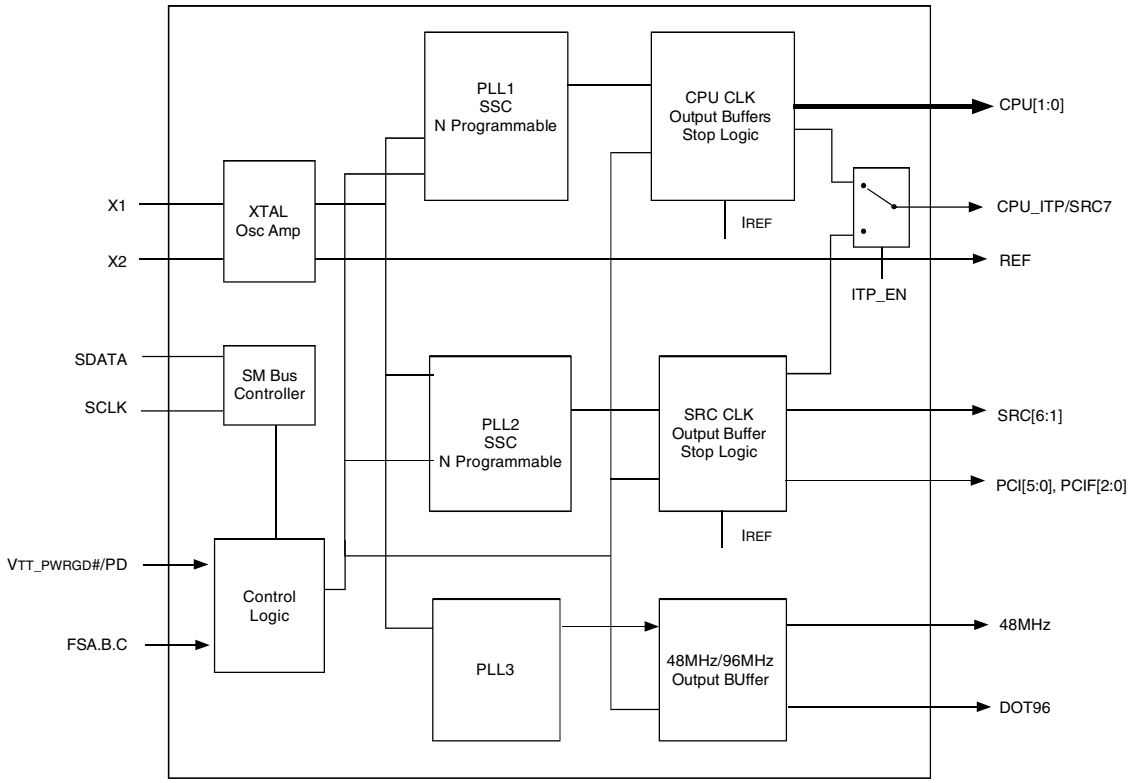
IDTCV110N is a 56 pin clock device, compliant with Intel CK410 specifications. The CPU output buffer is designed to support up to 400MHz processor. This chip has three PLLs inside for CPU/SRC/PCI, SATA, and 48MHz/DOT96 IO clocks. One dedicated PLL for Serial ATA clock provides high accuracy frequency. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

Each CPU/SRC/PCI, SATA clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

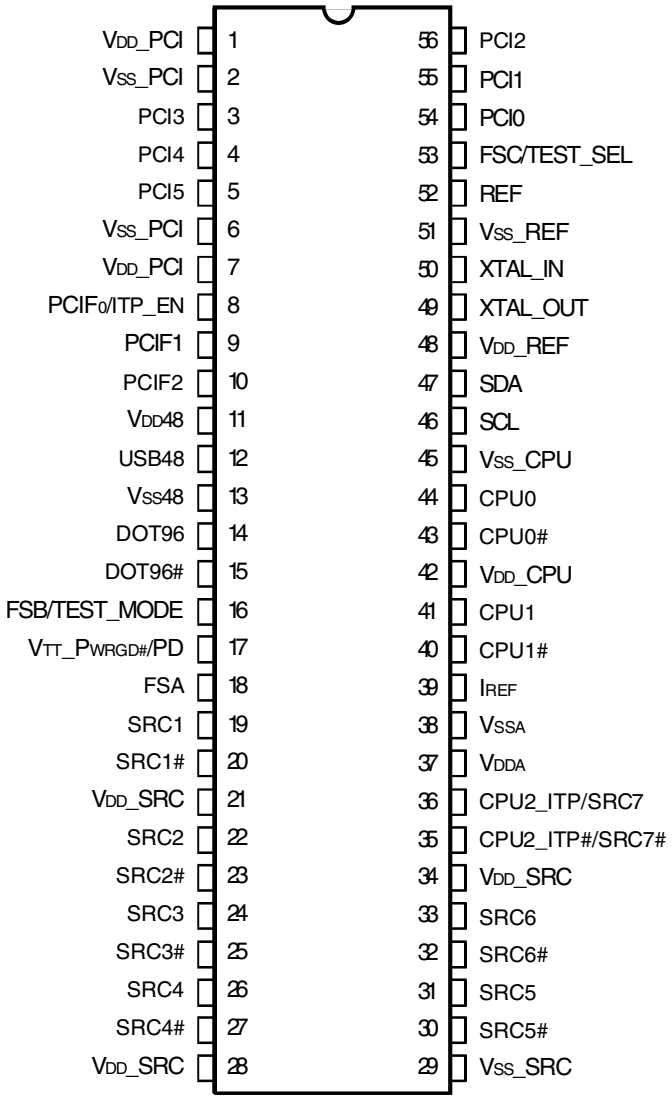
KEY SPECIFICATIONS:

- **CPU/SRC CLK cycle to cycle jitter < 85ps**
- **SATA CLK cycle to cycle jitter < 85ps**
- **PCI CLK cycle to cycle jitter < 250ps**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
V_{DDA}	3.3V Core Supply Voltage		4.6	V
V_{DD}	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
T_{STG}	Storage Temperature	–65	+150	° C
$T_{AMBIENT}$	Ambient Operating Temperature	0	+70	° C
T_{CASE}	Case Temperature		+115	° C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC[7:1]	PCI	USB	DOT	REF
101	100	100	33.3	48	96	14.318
001	133	100	33.3	48	96	14.318
011	166	100	33.3	48	96	14.318
010	200	100	33.3	48	96	14.318
000	266	100	33.3	48	96	14.318
100	333	100	33.3	48	96	14.318
110	400	100	33.3	48	96	14.318
111	Reserve	100	33.3	48	96	14.318

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	V_{DD}_PCI	PWR	3.3V
2	V_{SS}_PCI	GND	GND
3	PCI3	OUT	PCI clock
4	PCI4	OUT	PCI clock
5	PCI5	OUT	PCI clock
6	V_{SS}_PCI	GND	GND
7	V_{DD}_PCI	PWR	3.3V
8	PCIF0/ITP_EN	I/O	PCI clock, free running. CPU2 select (sampled on V_{TT}_P_{WRGD}# assertion) HIGH = CPU2.
9	PCIF1	OUT	PCI clock, free running
10	PCIF2	OUT	PCI clock, free running
11	V_{DD}48	PWR	3.3V
12	USB48	OUT	48MHz clock
13	V_{SS}48	GND	GND
14	DOT96	OUT	96MHz 0.7 current mode differential clock output
15	DOT96#	OUT	96MHz 0.7 current mode differential clock output
16	FSB/TEST_MODE	IN	CPU frequency selection. Selects R_{EF}/N or Hi-Z when in test mode, Hi-Z = 1, R_{EF}/N = 0.
17	V_{TT}_P_{WRGD}#/PD	IN	Level-sensitive strobe used to latch the FSA, FSB, FSC/TEST_SEL, and PCIF0/ITP_EN inputs. After V_{TT}_P_{WRGD}# assertion, becomes a real-time input for asserting power down. (Active HIGH)
18	FSA	IN	CPU frequency selection
19	SRC1	OUT	Differential serial reference clock
20	SRC1#	OUT	Differential serial reference clock
21	V_{DD}_SRC	PWR	3.3V
22	SRC2	OUT	Differential serial reference clock
23	SRC2#	OUT	Differential serial reference clock
24	SRC3	OUT	Differential serial reference clock
25	SRC3#	OUT	Differential serial reference clock
26	SRC4	OUT	Differential serial reference clock
27	SRC4#	OUT	Differential serial reference clock
28	V_{DD}_SRC	PWR	3.3V
29	V_{SS}_SRC	GND	GND
30	SRC5#	OUT	Differential serial reference clock
31	SRC5	OUT	Differential serial reference clock
32	SRC6#	OUT	Differential serial reference clock
33	SRC6	OUT	Differential serial reference clock
34	V_{DD}_SRC	PWR	3.3V
35	CPU2_ITP#/SRC7#	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at V_{TT}_P_{WRGD}# assertion = SRC7#.
36	CPU2_ITP/SRC7	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at V_{TT}_P_{WRGD}# assertion = SRC7.
37	V_{DDA}	PWR	3.3V
38	V_{SSA}	GND	GND
39	I_{REF}	OUT	Reference current for differential output buffer
40	CPU1#	OUT	Host 0.7 current mode differential clock output
41	CPU1	OUT	Host 0.7 current mode differential clock output
42	V_{DD}_CPU	PWR	3.3V

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
43	CPU0#	OUT	Host 0.7 current mode differential clock output
44	CPU0	OUT	Host 0.7 current mode differential clock output
45	V_{SS}_CPU	GND	GND
46	SCL	IN	SMBus clock
47	SDA	I/O	SMBus data
48	V_{DD}_REF	PWR	3.3V
49	XTAL_OUT	OUT	XTAL output
50	XTAL_IN	IN	XTAL input
51	V_{SS}_REF	GND	GND
52	REF	OUT	14.318 MHz reference clock output
53	FSC/TEST_SEL	IN	CPU frequency selection. Selects test mode if pulled to above 2V when V_{TT}_PWRGD# is asserted LOW.
54	PCI0	OUT	PCI clock
55	PCI1	OUT	PCI clock
56	PCI2	OUT	PCI clock

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

CONTROL REGISTERS

N PROGRAMMING PROCEDURE

- Use Index byte write.
- For N programming, the user only needs to access Byte17, Byte 25, and Byte8.

1. Write Byte17 for CPU PLL N, CPU f = N* Resolution, see resolution table below Byte17.
2. Write Byte25 for SRC PLL N, SRC f = N*0.666667, PCI = SRC f /3.
3. Enable N Programming bit, Byte8 bit1. Once this bit is enabled, any N value will be changed on the fly.

- Center spread only works when the N Programming bit is enabled. Down spread is OK even N Programming bit is disabled
- It is OK to change N value to any value on the bench test board. In the system, IDT recommends the stepping change. It is unknown how much the system can sustain for each stepping change; the estimate is about 5. If the N changes too much in one step, the system will likely hang.
- Note that SATA is with SRC PLL. This SATA Hard Drive might not operate during SRC N programming.

Most of the Bytes, from Byte8-Byte31, are used to adjust output waveforms and SSC modulation profiles. The power on setting will be changed according to each power on frequency selection. To avoid mistakes, don't write on those byte (be careful about Block Write). It is suggested to use the Index Byte write to access bytes.

SSC MAGNITUDE CONTROL, SMC

SMC[2:0]	
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

FREQUENCY SELECTION TABLE

FS_C, B, A	CPU
101	100
001	133
011	166
010	200
000	266
100	333
110	400
111	RESERVE

RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	Reserve					
1	SRC1, SRC1#	Output enable	Tristate	Enable	RW	1
2	SRC2, SRC2#	Output enable	Tristate	Enable	RW	1
3	SRC3, SRC3#	Output enable	Tristate	Enable	RW	1
4	SRC4, SRC4#	Output enable	Tristate	Enable	RW	1
5	SRC5, SRC5#	Output enable	Tristate	Enable	RW	1
6	SRC6, SRC6#	Output enable	Tristate	Enable	RW	1
7	CPU2, CPU2#/ SRC7, SRC7#	Output enable	Tristate	Enable	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	CPU[2:0], SRC[7:1], PCI[5:0], PCIF[2:0]	Spread Spectrum mode enable	Spread off	Spread on	RW	0
1	CPU0, CPU0#	Output enable	Tristate	Enable	RW	1
2	CPU1, CPU1#	Output enable	Tristate	Enable	RW	1
3	Reserve					0
4	REF	Output enable	Tristate	Enable	RW	1
5	USB48	Output enable	Tristate	Enable	RW	1
6	DOT96	Output enable	Tristate	Enable	RW	1
7	PCIF0	Output enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	PCIF1	Output enable	Tristate	Enable	RW	1
1	PCIF2	Output enable	Tristate	Enable	RW	1
2	PCI0	Output enable	Tristate	Enable	RW	1
3	PCI1	Output enable	Tristate	Enable	RW	1
4	PCI2	Output enable	Tristate	Enable	RW	1
5	PCI3	Output enable	Tristate	Enable	RW	1
6	PCI4	Output enable	Tristate	Enable	RW	1
7	PCI5	Output enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Reserve					
1	SRC1	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
2	SRC2	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
3	SRC3	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
4	SRC4	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
5	SRC5	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
6	SRC6	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0
7	SRC7	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Free running, not affected by PCI_STOP	Stopped with PCI_STOP	RW	0

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Reserve				RW	1
1	Reserve				RW	1
2	Reserve				RW	1
3	PCIF0	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Not stopped by PCI_STOP	Stopped with PCI_STOP	RW	0
4	PCIF1	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Not stopped by PCI_STOP	Stopped with PCI_STOP	RW	0
5	PCIF2	Allow controlled by software PCI_STOP, byte 6, bit 3, assertion	Not stopped by PCI_STOP	Stopped with PCI_STOP	RW	0
6	DOT96	DOT96 power down drive mode	Driven in power down	Tristate	RW	0
7	Reserve					0

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU0, CPU0#	CPU0 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
1	CPU1, CPU1#	CPU1 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
2	CPU2, CPU2#	CPU2 PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
3	SRC[7:1], SRC[7:1]#	SRC PWRDWN drive mode	Driven in power down	Tristate in power down	RW	0
4	Reserve					0
5	Reserve					0
6	Reserve					0
7	SRC[7:1], SRC[7:1]#	SRC PCI_STOP drive mode	Driven in PCI_STOP	Tristate when stopped	RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU[2:0]	FSA latched value on power up			R	
1	CPU[2:0]	FSB latched value on power up			R	
2	CPU[2:0]	FSC latched value on power up			R	
3	PCI, SRC	Software PCI_STOP control for PCI and SRC CLK	Stop all PCI, PCIF, and SRC which can be stopped by PCI_STOP#	Software STOP Disabled	RW	1
4	REF	REF drive strength	1x drive	2x drive		1
5	Reserve					0
6		Test clock mode entry control	Normal operation	Test mode, controlled by Byte 6, Bit 7	RW	0
7	CPU, SRC, PCI PCIF, REF, USB48, DOT96	Only valid when Byte 6, Bit 7 is HIGH	Hi-Z	REF/N		0

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		Vendor ID			R	1
1		Vendor ID			R	0
2		Vendor ID			R	1
3		Vendor ID			R	0
4		Revision ID			R	0
5		Revision ID			R	1
6		Revision ID			R	1
7		Revision ID			R	0

BYTE 8

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	One cycle read		disable	enable	RW	0
1		N Programming enable	Disable	enable	RW	0
2	Reserve				RW	0
3	USB48	USB 48 Strength control	1x	2x	RW	0
4		USB PLL power down	normal	Power down	RW	0
5		SRC PLL power down	normal	Power down	RW	0
6		CPU PLL power down	normal	Power down	RW	0
7	SRC, PLL2, SSC enable	Only valid when Byte1 bit0 is 1	disable	enable	RW	1

BYTE 9

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC SMC0	SRC/PCI SSC control see SMC table			RW	1
1	SRC SMC1				RW	0
2	SRC SMC2				RW	0
3	Reserve				RW	0
4	CPU SMC0	CPU PLL SSC control see SMC table			RW	1
5	CPU SMC1				RW	0
6	CPU SMC2				RW	0
7		Must be 0	Must be 0		RW	0 (Must be 0)

BYTES 10-16: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

BYTE 17

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU_N0, LSB	CPU CLK = N* Resolution			RW	
1	CPU_N1	see Resolution table			RW	
2	CPU_N2				RW	
3	CPU_N3				RW	
4	CPU_N4				RW	
5	CPU_N5				RW	
6	CPU_N6				RW	
7	CPU_N7, MSB				RW	

BYTES 18-24: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

BYTE 25

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_N0, LSB	SRC f = N*SRC Resolution			RW	
1	SRC_N1	Resolution = 0.666667			RW	
2	SRC_N2	100MHz N= 150			RW	
3	SRC_N3				RW	
4	SRC_N4				RW	
5	SRC_N5				RW	
6	SRC_N6				RW	
7	SRC_N7, MSB				RW	

BYTES 26-31: OUTPUT WAVEFORM ADJUSTMENT. DON'T WRITE OVER.

APPLICATION NOTE

Bits	Strength
111	0.6x
011	0.8x
001	1x
000	1.2x

Byte 18, bit[2:0] controls PCIF[2:0] strength.
Byte 26, bit[2:0] controls PCI[5:0] strength.
Byte 27, Byte 28 controls the magnitude of the SRC spread. (1)
Byte 30, Byte 31 sets the center of the frequency of the SRC. (1)
Byte 23, bit[3:0] controls the CPU PLL spread.

NOTE:
1. Write byte 9 prior to Bytes 27, 28, 30, and 31.

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V_{SS} - 0.3	—	0.35	V
I_{IL}	Input LeakageCurrent	0< V_{IN} < V_{DD}, no internal pull-up or pull-down	–5	—	+5	mA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		X1 and X2 pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE_PD}(2)	CPU output enable after PD de-assertion	—	—	300	us
	T_{FALL_PD}(2)	Fall time of PD	—	—	5	ns
	T_{RISE_PD}(3)	Rise time of PD	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	1150	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–300	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(2,3)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period(2,3)	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SK3}	Skew, CPU[1:0](2)	V_T = 50%	—	—	100	ps
	Skew, CPU2(2)		—	—	250	
	Skew, SRC(2)		—	—	250	
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[1:0](2)	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, CPU2(2)		—	—	100	
	Jitter, Cycle to Cycle, SRC(2)		—	—	125	
	Jitter, Cycle to Cycle, DOT96(2)		—	—	250	

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

PCI STOP FUNCTIONALITY

If PCIF (2:0) and SRC clocks are set to be free-running through SMBus programming, they will ignore the PCI_STOP register bit.

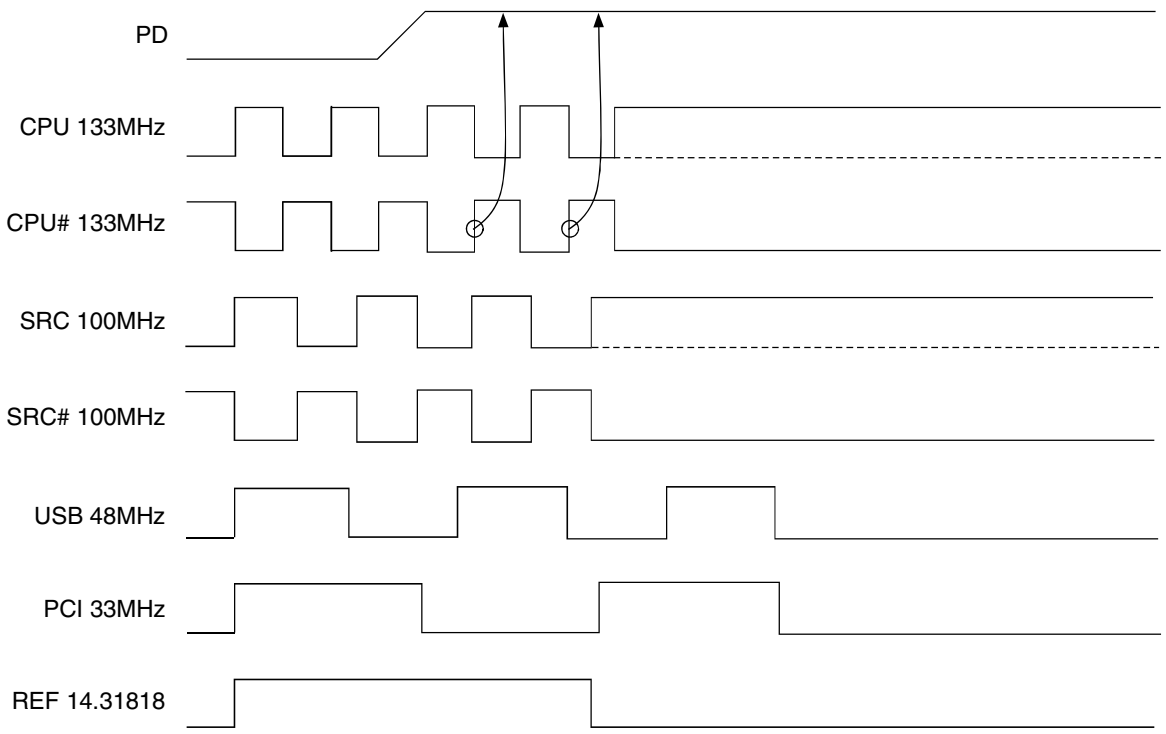
PCI_STOP (Byte 6 bit 3)	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	Normal	Normal	I_{REF} * 6 or float	Low	Low	48MHz	Normal	Normal	14.318MHz

PD, POWER DOWN

PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

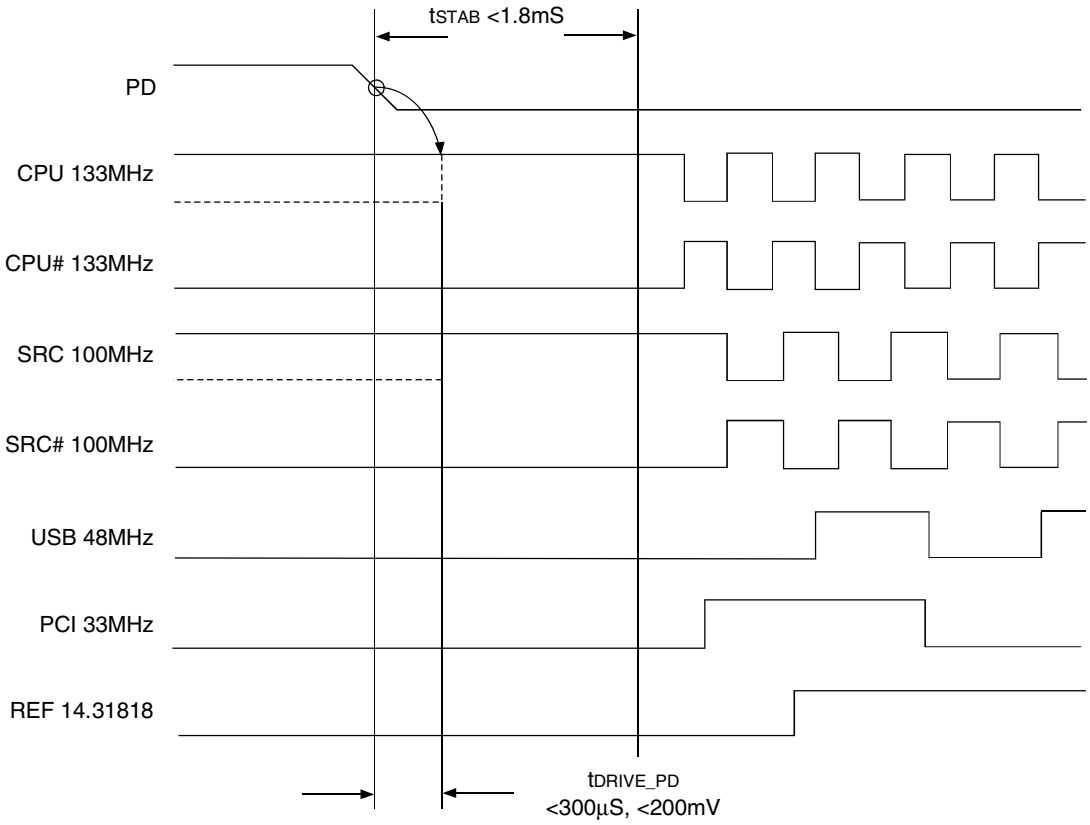
PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	I_{REF} * 2 or float	Float	I_{REF} * 2 or float	Float	Low	Low	I_{REF} * 2 or float	Float	Low

PD ASSERTION

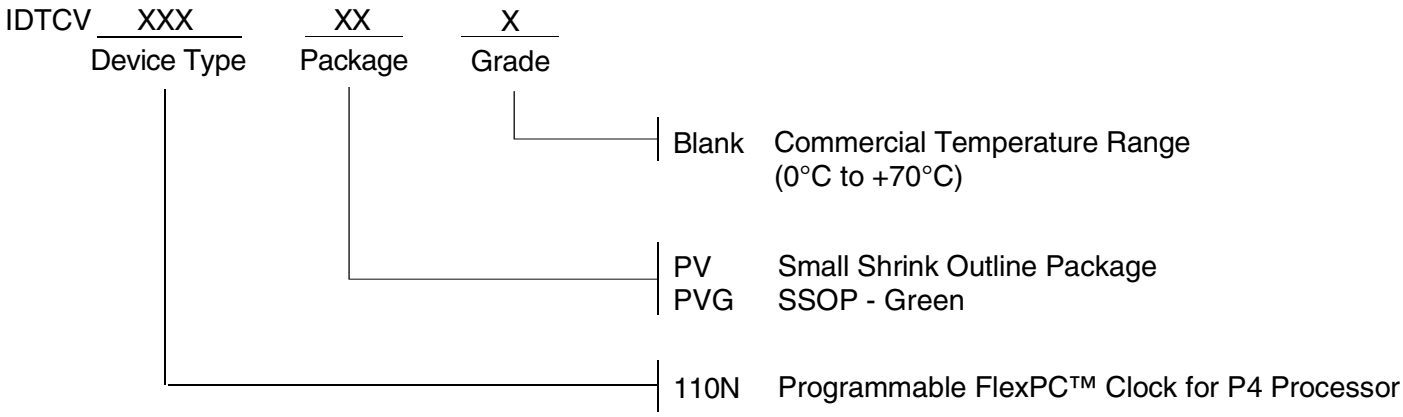


PD DE-ASSERTION

The time from the de-assertion of PD or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD deassertion.



ORDERING INFORMATION



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