

## 3.3V SDRAM Buffer for Mobile PCs with 4 SO-DIMMs

### Features

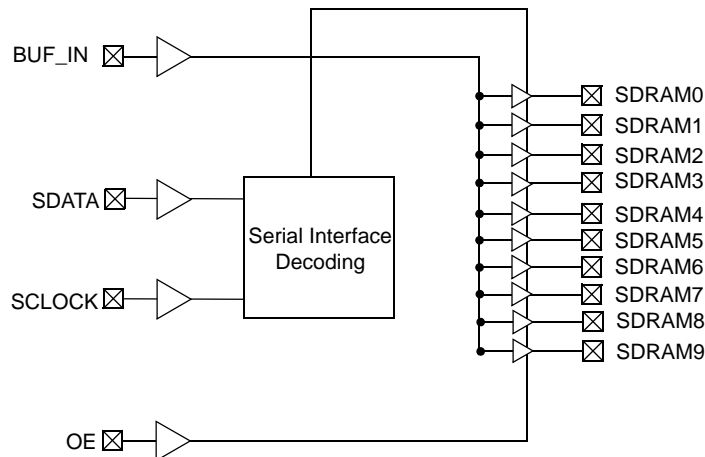
- One input to 10 output buffer and driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 100 MHz operation
- Multiple  $V_{DD}$  and  $V_{SS}$  pins for noise reduction
- Dedicated OE pin for testing
- Space saving 28-pin SSOP package
- 3.3V operation

### Functional Description

The CY2310ANZ is a 3.3V buffer designed to distribute high speed clocks in mobile PC applications. The part has 10 outputs, eight of which are used to drive up to four SDRAM SO-DIMMs. The remaining are used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium II® processors. The CY2310ANZ can be used in conjunction with the CY2281 or similar clock synthesizer for a full Pentium II motherboard solution.

The CY2310ANZ also includes a serial interface which can enable or disable each output clock. During power up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

### Logic Block Diagram



## Pin Configuration

Figure 1. Pin Diagram: 28-Pin SSOP

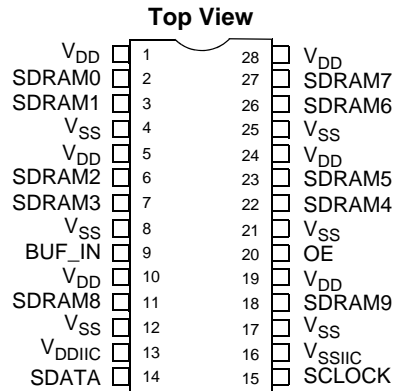


Table 1. Pin Summary

Name	Pins	Description
V <sub>DD</sub>	1, 5, 10, 19, 24, 28	3.3V Digital voltage supply
V <sub>SS</sub>	4, 8, 12, 17, 21, 25	Ground
V <sub>DDIIC</sub>	13	Serial interface voltage supply
V <sub>SSIIC</sub>	16	Ground for serial interface
BUF_IN	9	Input clock
OE	20	Output Enable, three-states outputs when LOW. Internal pull up to V <sub>DD</sub>
SDATA	14	Serial data input, internal pull-up to V <sub>DD</sub>
SCLK	15	Serial clock input, internal pull-up to V <sub>DD</sub>
SDRAM [0–3]	2, 3, 6, 7	SDRAM byte 0 clock outputs
SDRAM [4–7]	22, 23, 26, 27	SDRAM byte 1 clock outputs
SDRAM [8–9]	11, 18	SDRAM byte 2 clock outputs

### Device Functionality

OE	SDRAM [0–17]
0	High-Z
1	1 x BUF_IN

### Serial Configuration Map

- The serial bits are read by the clock driver in the following order:
  - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to “0”.
- Serial interface address for the CY2310ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

### Byte 0:SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enabled

Bit	Pin No.	Description
Bit 7	--	Initialize to 0
Bit 6	--	Initialize to 0
Bit 5	--	Initialize to 0
Bit 4	--	Initialize to 0
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

### Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin No.	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	--	Initialize to 0
Bit 2	--	Initialize to 0
Bit 1	--	Initialize to 0
Bit 0	--	Initialize to 0

### Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin No.	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	--	Reserved, drive to 0
Bit 0	--	Reserved, drive to 0

## Maximum Ratings

Supply Voltage to Ground Potential.....	-0.5V to +7.0V	Storage Temperature .....	-65°C to +150°C
DC Input Voltage (Except BUF_IN) .....	-0.5V to $V_{DD} + 0.5V$	Junction Temperature .....	150°C
DC Input Voltage (BUF_IN) .....	-0.5V to +7.0V	Static Discharge Voltage (per MIL-STD-883, Method 3015) .....	>2000V

## Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	3.135	3.465	V
$T_A$	Operating Temperature (Ambient Temperature)	0	70	°C
$C_L$	Load Capacitance	20	30	pF
$C_{IN}$	Input Capacitance		7	pF
$t_{PU}$	Power up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

## Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>	Except serial interface pins		0.8	V
$V_{ILiic}$	Input LOW Voltage	For serial interface pins only		0.7	V
$V_{IH}$	Input HIGH Voltage <sup>[1]</sup>		2.0		V
$I_{IL}$	Input LOW Current (BUF_IN input)	$V_{IN} = 0V$	-10	10	μA
$I_{IL}$	Input LOW Current (Except BUF_IN Pin)	$V_{IN} = 0V$		100	μA
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$	-10	10	μA
$V_{OL}$	Output LOW Voltage <sup>[2]</sup>	$I_{OL} = 25\text{ mA}$		0.4	V
$V_{OH}$	Output HIGH Voltage <sup>[2]</sup>	$I_{OH} = -36\text{ mA}$	2.4		V
$I_{DD}$	Supply Current <sup>[2]</sup>	Unloaded outputs, 100-MHz		200	mA
$I_{DD}$	Supply Current	Loaded outputs, 100-MHz		360	mA
$I_{DD}$	Supply Current <sup>[2]</sup>	Unloaded outputs, 66.67-MHz		150	mA
$I_{DD}$	Supply Current	Loaded outputs, 66.67-MHz		230	mA
$I_{DDs}$	Supply Current	BUF_IN= $V_{DD}$ or $V_{SS}$ All other inputs at $V_{DD}$		500	μA

### Notes

1. BUF\_IN input has a threshold voltage of  $V_{DD}/2$ .
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Characteristics<sup>[3]</sup>

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
	Maximum Operating Frequency				100	MHz
	Duty Cycle <sup>[2, 4]</sup> = $t_2 \div t_1$	Measured at 1.5V	45.0	50.0	55.0	%
t <sub>3</sub>	Rising Edge Rate <sup>[2]</sup>	Measured between 0.4V and 2.4V	0.9	1.5	4.0	V/ns
t <sub>4</sub>	Falling Edge Rate <sup>[2]</sup>	Measured between 2.4V and 0.4V	0.9	1.5	4.0	V/ns
t <sub>5</sub>	Output to Output Skew <sup>[2]</sup>	All outputs equally loaded		150	250	ps
t <sub>6</sub>	SDRAM Buffer LH Prop. Delay <sup>[2]</sup>	Input edge greater than 1 V/ns	1.0	3.5	5.0	ns
t <sub>7</sub>	SDRAM Buffer HL Prop. Delay <sup>[2]</sup>	Input edge greater than 1 V/ns	1.0	3.5	5.0	ns
t <sub>8</sub>	SDRAM Buffer Enable Delay <sup>[2]</sup>	Input edge greater than 1 V/ns	1.0	5	12	ns
t <sub>9</sub>	SDRAM Buffer Disable Delay <sup>[2]</sup>	Input edge greater than 1 V/ns	1.0	20	30	ns

Switching Waveforms

Figure 2. Duty Cycle Timing

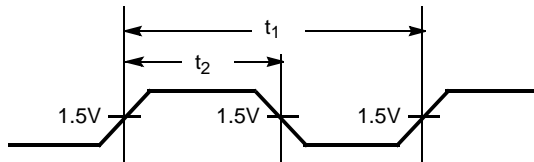


Figure 3. All Outputs Rise/Fall Time

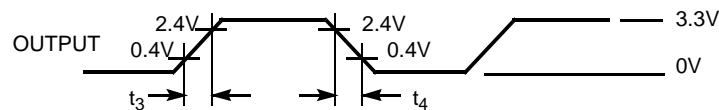
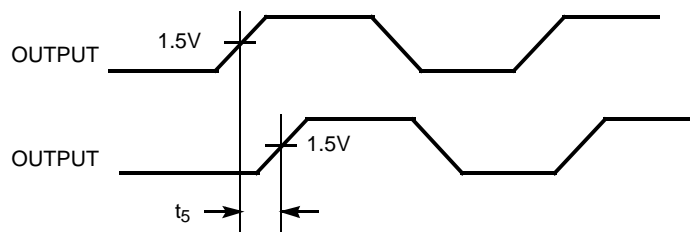


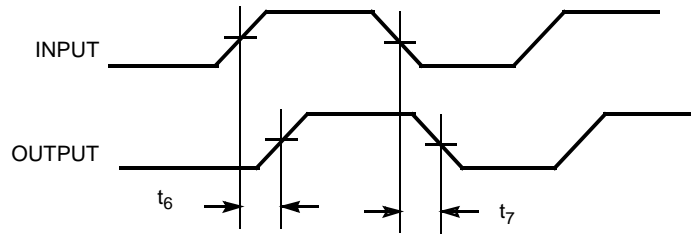
Figure 4. Output-Output Skew



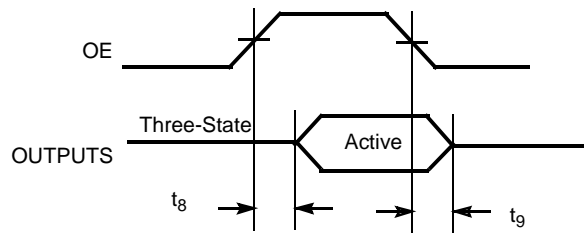
Notes

- 3. All parameters specified with loaded outputs.
- 4. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/n

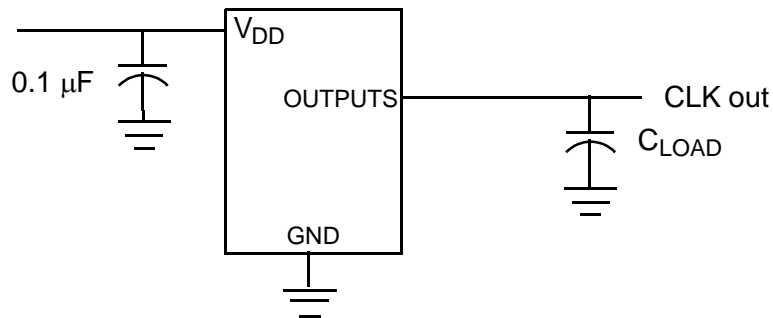
**Figure 5. SDRAM Buffer LH and HL Propagation Delay**



**Figure 6. SDRAM Buffer Enable and Disable Times**

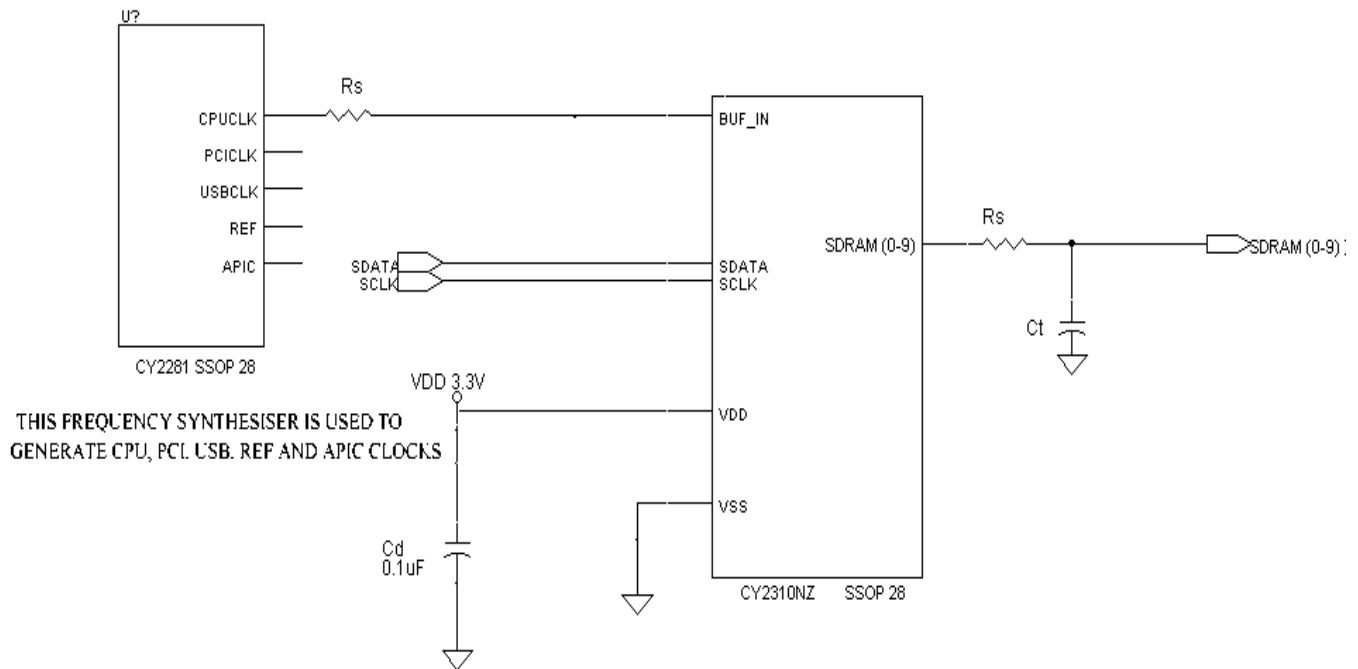


**Figure 7. Test Circuit**



## Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.



Cd = DECOUPLING CAPACITOR

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Rs = SERIES TERMINATING RESISTORS

## Summary

- Surface mount, low ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the buffer (typically 25Ω), and  $R_{series}$  is the series terminating resistor.  

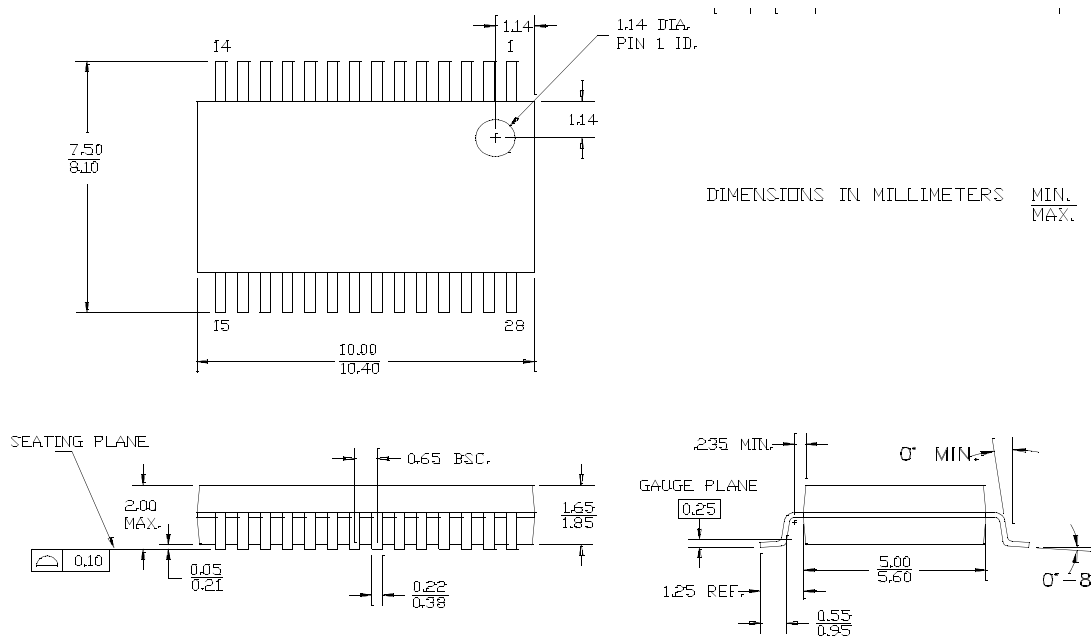
$$R_{series} > R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 μF to 22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

### Ordering Information

Ordering Code	Package Type	Operating Range
CY2310ANZPVC-1T	28-Pin SSOP - Tape and Reel	Commercial
<b>Pb-Free</b>		
CY2310ANZPVXC-1	28-Pin SSOP	Commercial
CY2310ANZPVXC-1T	28-Pin SSOP - Tape and Reel	Commercial

### Package Diagram

Figure 8. 28-Pin (5.3 mm) Shrunk Small Outline Package O28



51-85079-C



## Document History Page

Document Title: CY2310ANZ 3.3V SDRAM Buffer for Mobile PCs with 4 SO-DIMMs Document Number: 38-07142				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110251	DSG	11/18/01	Change from Spec number: 38-00659 to 38-07142
*A	121829	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	310555	RGL	See ECN	Added Lead-free Devices
*C	2635282	KVM/PYRS	01/13/09	Remove CY2310ANZPVC-1 from Ordering Information table Replace "Lead-Free" with "Pb-Free"

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