

# Programmable Timing Control Hub™ for P4™

## ICS950201

**Recommended Application:**

CK-408 clock for Intel® 845 chipset with P4 processor.

**Output Features:**

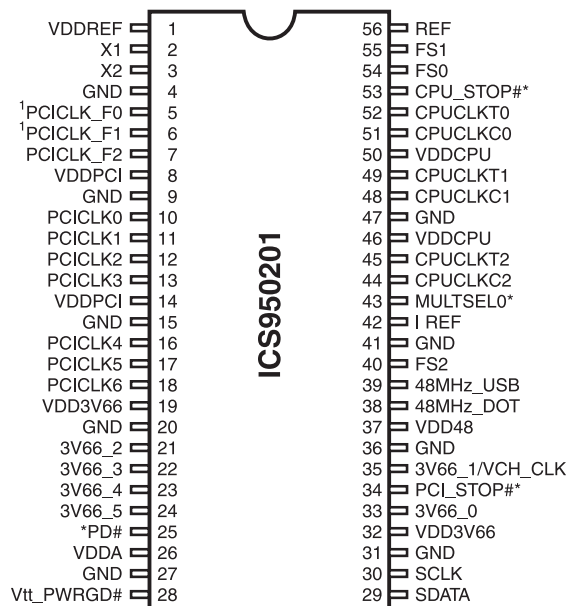
- 3 Differential CPU Clock Pairs @ 3.3V
- 7 PCI (3.3V) @ 33.3MHz
- 3 PCI\_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz
- 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

**Features:**

- Supports spread spectrum modulation, down spread 0 to -0.5%.
- Efficient power management scheme through PD#, CPU\_STOP# and PCI\_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through I<sup>2</sup>C interface.

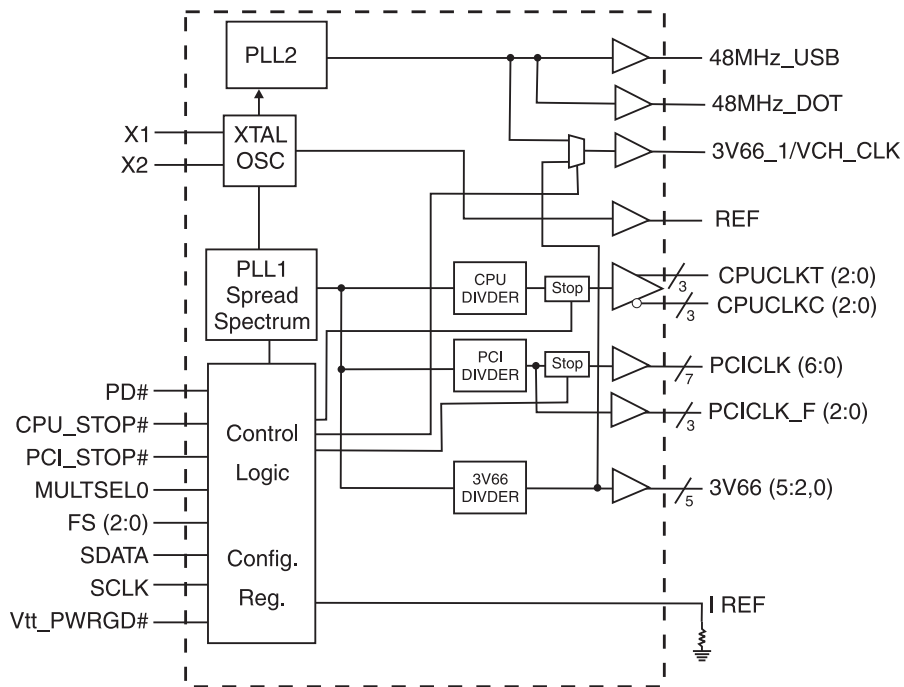
**Key Specifications:**

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps, programmable over 800 ps with groups CPU0,1 and CPU2.

**Pin Configuration**

**56-Pin SSOP & TSSOP**

\* These inputs have 150K internal pull-up resistor to VDD.

Block Diagram



## Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 19, 26, 32, 37, 46, 50	VDD	PWR	3.3V power supply
2	X1	X2 Crystal Input	14.318MHz Crystal input
3	X2	X1 Crystal Output	14.318MHz Crystal output
7, 6, 5	PCICLK_F (2:0)	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
4, 9, 15, 20, 27, 31, 36, 41, 47	GND	PWR	Ground pins for 3.3V supply
18, 17, 16, 13, 12, 11, 10	PCICLK (6:0)	OUT	PCI clock outputs
24, 23, 22, 21	3V66 (5:2)	OUT	66MHz reference clocks, from internal VCO
24	3V66_5	OUT	66MHz reference clock, from internal VCO
25	PD#	IN	Invokes power-down mode. Active Low.
28	Vtt_PWRGD#	IN	This 3.3V LVTTTL input is a level sensitive strobe used to determine when FS(2:0) and MULTISEL0 inputs are valid and are ready to be sampled (active low)
29	SDATA	I/O	Data pin for I <sup>2</sup> C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I <sup>2</sup> C circuitry 5V tolerant
33	3V66_0	OUT	66MHz reference clocks, from internal VCO
34	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low except PCICLK_F which are free running
35	3V66_1/VCH_CLK	OUT	3.3V output selectable through I <sup>2</sup> C to be 66MHz from internal VCO or 48MHz (non-SSC)
38	48MHz_DOT	OUT	48MHz output clock for DOT
39	48MHz_USB	OUT	48MHz output clock for USB
40	FS2	IN	Special 3.3V input for Mode selection, cannot be logic 1
, 42	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL0	IN	3.3V LVTTTL input for selecting the current multiplier for CPU outputs
44, 48, 51	CPUCLKC (2:0)	OUT	"Complementary" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 49, 52	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
53	CPU_STOP#	IN	Halts CPUCLK clocks at logic 0 level, when input low
55, 54	FS (1:0)	IN	Frequency select pins
56	REF	OUT	14.318MHz reference clock.

## Power Groups

### (Analog)

VDDA = Analog Core PLL1  
 VDDREF = REF, Xtal  
 VDD48 = 48MHz, PLL

### (Digital)

VDDPCI  
 VDD3V66  
 VDDCPU

**Truth Table**

FS2	FS1	FS0	CPU (MHz)	3V66 (5:0) (MHz)	PCI_F PCI (MHz)	REF0 (MHz)	USB/DOT (MHz)
0	0	0	66.66	66.66	33.33	14.318	48.00
0	0	1	100.00	66.66	33.33	14.318	48.00
0	1	0	200.00	66.66	33.33	14.318	48.00
0	1	1	133.33	66.66	33.33	14.318	48.00
Mid	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/8	TCLK	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved	Reserved	Reserved

**Maximum Allowed Current**

<b>Condition</b>	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
<b>Full Active</b>	360mA

**Host Swing Select Functions**

MULTISELO	Board Target Trace/Term Z	Reference R, Iref = $V_{DD}/(3 \cdot R_r)$	Output Current	Voh @ Z
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6 * I REF	0.7V @ 50

## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
 For more information, contact IDT for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 6**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Byte 6	
	<b>ACK</b>
Stop Bit	

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
	<b>Byte 6</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only **"Block-Writes"** from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

**Byte 0: Control Register**

Bit	Pin#	Name	PWD <sup>2</sup>	Type <sup>1</sup>	Description
Bit 0	54	FS0	X	R	Reflects the value of FS0 pin sampled on power up
Bit 1	55	FS1	X	R	Reflects the value of FS1 pin sampled on power up
Bit 2	40	FS2	X	R	Reflects the value of FS2 pin sampled on power up
Bit 3	34	PCI_STOP# <sup>3</sup>	X	R	Hardware mode: Reflects the value of PCI_STOP# pin sampled on PWD
			1	RW	Software mode: 0=PCICLK stopped 1=PCICLK not stopped
Bit 4	53	CPU_STOP#	X	R	Reflects the current value of the external CPU_STOP# pin
Bit 5	35	3V66_1/VCH	0	RW	VCH Select 66MHz/48MHz 0=66MHz, 1=48MHz
Bit 6	-		0		(Reserved)
Bit 7	-	Spread Enabled	0	RW	0=Spread Off, 1=Spread On

**Byte 1: Control Register**

Bit	Pin#	Name	PWD <sup>2</sup>	Type <sup>1</sup>	Description
Bit 0	52, 51	CPUCLKT0 CPUCLKC0	1	RW	0=Disabled 1=Enabled <sup>4</sup>
Bit 1	49, 48	CPUCLKT1 CPUCLKC1	1	RW	0=Disabled 1=Enabled <sup>4</sup>
Bit 2	45, 44	CPUCLKT2 CPUCLKC2	1	RW	0=Disabled 1=Enabled <sup>4</sup>
Bit 3	52, 51	CPUCLKT0 CPUCLKC0	0	RW	Allow control of CPUCLKT0/C0 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 4	49, 48	CPUCLKT1 CPUCLKC1	0	RW	Allow control of CPUCLKT1/C1 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 5	45, 44	CPUCLKT2 CPUCLKC2	0	RW	Allow control of CPUCLKT2/C2 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 6	-	-	0	-	(Reserved)
Bit 7	43	MULTSELO	X	R	Reflects the current value of MULTSELO

**Notes:**

1. R= Read only RW= Read and Write
2. PWD = Power on Default
3. The purpose of this bit is to allow a system designer to implement PCI\_STOP functionality in one of two ways. With the system designer can choose to use the externally provided PCI\_STOP# pin to assert and de-assert PCI\_STOP functionality via I<sup>2</sup>C Byte 0 Bit 3.

In Hardware mode it is not allowed to write to the I<sup>2</sup>C Byte 0 Bit3. In Software mode it is not allowed to pull the external PCI\_STOP pin low. This avoids the issues related with Hardware started and software stopped PCI\_STOP conditions. The clock chip is to be operated in the Hardware or Software PCI\_STOP mode ONLY, it is not allowed to mix these modes.

In Hardware mode the I<sup>2</sup>C byte 0 Bit 3 is R/W and should reflect the status of the part. Whether or not the chip is in PCI\_STOP mode.

Functionality PCI\_STOP mode should be entered when [(PCI\_STOP#=0) or (I<sup>2</sup>C Byte 0 Bit 3 = 0)].

4. For disabled clocks, they stop low for single ended clocks. Differential CPU clocks stop with CPUCLKT at high, CPUCLKC off, and external resistor termination will bring CPUCLKC low.

**Byte 2: Control Register**

Bit	Pin#	Name	PWD	Type	Description
Bit 0	10	PCICLK0	1	RW	0=Disabled 1=Enabled
Bit 1	11	PCICLK1	1	RW	0=Disabled 1=Enabled
Bit 2	12	PCICLK2	1	RW	0=Disabled 1=Enabled
Bit 3	13	PCICLK3	1	RW	0=Disabled 1=Enabled
Bit 4	16	PCICLK4	1	RW	0=Disabled 1=Enabled
Bit 5	17	PCICLK5	1	RW	0=Disabled 1=Enabled
Bit 6	18	PCICLK6	1	RW	0=Disabled 1=Enabled
Bit 7	-	-	0	-	(Reserved)

**Byte 3: Control Register**

Bit	Pin#	Name	PWD	Type	Description
Bit 0	5	PCICLK_F0	1	RW	0=Disabled 1=Enabled
Bit 1	6	PCICLK_F1	1	RW	0=Disabled 1=Enabled
Bit 2	7	PCICLK_F2	1	RW	0=Disabled 1=Enabled
Bit 3	5	PCICLK_F0	0	RW	Allow control of PCICLK_F0 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 4	6	PCICLK_F1	0	RW	Allow control of PCICLK_F1 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 5	7	PCICLK_F2	0	RW	Allow control of PCICLK_F2 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 6	39	48MHz_USB	1	RW	0=Disabled 1=Enabled
Bit 7	38	48MHz_DOT	1	RW	0=Disabled 1=Enabled

**Byte 4: Control Register**

Bit	Pin#	Name	PWD	Type	Description
Bit 0	21	3V66-2	1	RW	0=Disabled 1=Enabled
Bit 1	22	3V66-3	1	RW	0=Disabled 1=Enabled
Bit 2	23	3V66-4	1	RW	0=Disabled 1=Enabled
Bit 3	24	3V66_5	1	RW	0=Disabled 1=Enabled
Bit 4	35	3V66_1/VCH_CLK	1	RW	0=Disabled 1=Enabled
Bit 5	33	3V66_0	1	RW	0=Disabled 1=Enabled
Bit 6	-	-	0	R	(Reserved)
Bit 7	-	-	0	R	(Reserved)

**Notes:**

1. R= Read only RW= Read and Write
2. PWD = Power on Default

## Absolute Maximum Ratings

Supply Voltage	5.5 V
Logic Inputs	GND -0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	$V_{IH}$		2		$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$	-5		5	$\mu\text{A}$
Input Low Current	$I_{IL1}$	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5			$\mu\text{A}$
	$I_{IL2}$	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	$C_L =$ Full load; Select @ 100 MHz	229	240	360	mA
	$I_{DD3.3OP}$	$C_L =$ Full load; Select @ 133 MHz	220	236	360	mA
	$I_{DD3.3OP}$	$C_L =$ Full load; Select @ 200 MHz	234	245	360	mA
Powerdown Current	$I_{DD3.3PD}$				45	mA
Input Frequency	$F_i$	$V_{DD} = 3.3$ V		14.318		MHz
Pin Inductance	$L_{pin}$				7	nH
Input Capacitance <sup>1</sup>	$C_{IN}$	Logic Inputs			5	pF
	$C_{OUT}$	Output pin capacitance			6	pF
	$C_{INX}$	X1 & X2 pins	27		45	pF
Transition time <sup>1</sup>	$T_{trans}$	To 1st crossing of target frequency			3	ms
Settling time <sup>1</sup>	$T_s$	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization <sup>1</sup>	$T_{STAB}$	From $V_{DD} = 3.3$ V to 1% target frequency			3	ms
Delay <sup>1</sup>	$t_{PZH}, t_{PZL}$	Output enable delay (all outputs)	1		10	ns
	$t_{PHZ}, t_{PLZ}$	Output disable delay (all outputs)	1		10	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	$Z_o^1$	$V_O = V_x$	3000			$\Omega$	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	770	850	mV	1
Voltage Low	VLow		-150	5	150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		756	1150	mV	1
Min Voltage	Vuds		-300	-7			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	$T_{absmin}$	200MHz nominal	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	$t_r$	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175	332	700	ps	1
Fall Time	$t_f$	$V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$	175	344	700	ps	1
Rise Time Variation	d- $t_r$			30	125	ps	1
Fall Time Variation	d- $t_f$			30	125	ps	1
Duty Cycle	$d_{t3}$	Measurement from differential waveform	45	49	55	%	1
Skew	$t_{sk3}$	$V_T = 50\%$		8	100	ps	1
Jitter, Cycle to cycle	$t_{j\text{cyc-cyc}}$	Measurement from differential waveform		60	150	ps	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

**Electrical Characteristics - PCICLK**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	$F_{O1}$			33.33		MHz
Output Impedance	$R_{DSP1}^1$	$V_O = V_{DD} * (0.5)$	12	33	55	$\Omega$
Output High Voltage	$V_{OH}^1$	$I_{OH} = -1\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}^1$	$I_{OL} = 1\text{ mA}$			0.55	V
Output High Current	$I_{OH}^1$	$V_{OH@MIN} = 1.0\text{ V}, V_{OH@MAX} = 3.135\text{ V}$	-33		-33	mA
Output Low Current	$I_{OL}^1$	$V_{OL@MIN} = 1.95\text{ V}, V_{OL@MAX} = 0.4\text{ V}$	30		38	mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$	0.5	1.29	2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$	0.5	1.45	2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.5\text{ V}$	45	51	55	%
Skew	$t_{sk1}^1$	$V_T = 1.5\text{ V}$		190	500	ps
Jitter, cycle to cyc	$t_{jyc-cyc}^1$	$V_T = 1.5\text{ V}$		124	250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - 3V66**

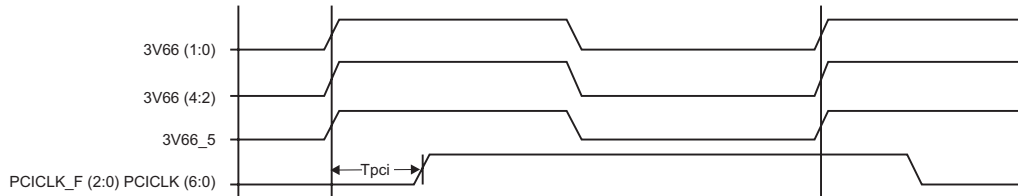
$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	$F_{O1}$			66.67		MHz
Output Impedance	$R_{DSP1}^1$	$V_O = V_{DD} * (0.5)$	12	33	55	$\Omega$
Output High Voltage	$V_{OH}^1$	$I_{OH} = -1\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}^1$	$I_{OL} = 1\text{ mA}$			0.55	V
Output High Current	$I_{OH}^1$	$V_{OH@MIN} = 1.0\text{ V}, V_{OH@MAX} = 3.135\text{ V}$	-33		-33	mA
Output Low Current	$I_{OL}^1$	$V_{OL@MIN} = 1.95\text{ V}, V_{OL@MAX} = 0.4\text{ V}$	30		38	mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$	0.5	1.28	2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$	0.5	1.36	2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.5\text{ V}$	45	53.1	55	%
Skew	$t_{sk1}^1$	$V_T = 1.5\text{ V}$		90	250	ps
Jitter	$t_{jyc-cyc}^1$	$V_T = 1.5\text{ V}$ 3V66		128	250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66\_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66\_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as T<sub>pci</sub>.



### Group Skews at Common Transition Edges: (Un-Buffered Mode)

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 pin to pin skew	0		500	ps
PCI	PCI	PCI_F and PCI pin to pin skew	0		500	ps
3V66 to PCI	S <sub>3V66-PCI</sub>	3V66 leads 33MHz PCI	1.5		3.5	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.

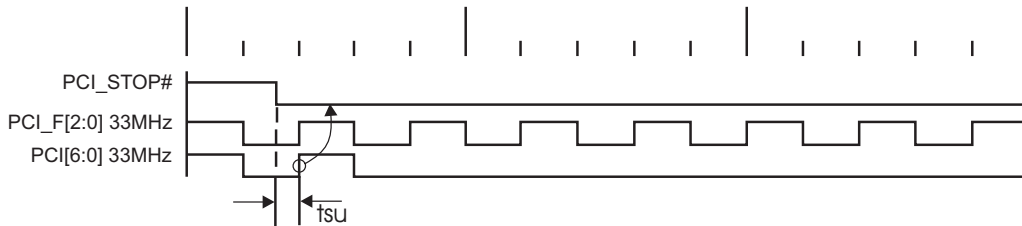
### PD# Functionality

CPU_STOP#	CPUT	CPUC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN	66MHz_IN	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low

**PCI\_STOP# - Assertion (transition from logic "1" to logic "0")**

The impact of asserting the PCI\_STOP# signal will be the following. All PCI[6:0] and stoppable PCI\_F[2,0] clocks will latch low in their next high to low transition. The PCI\_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

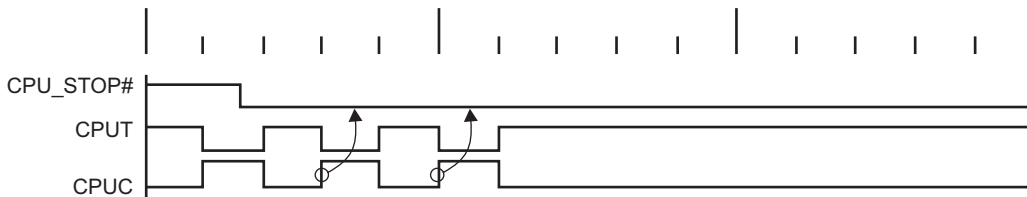
**Assertion of PCI\_STOP# Waveforms**



**CPU\_STOP# - Assertion (transition from logic "1" to logic "0")**

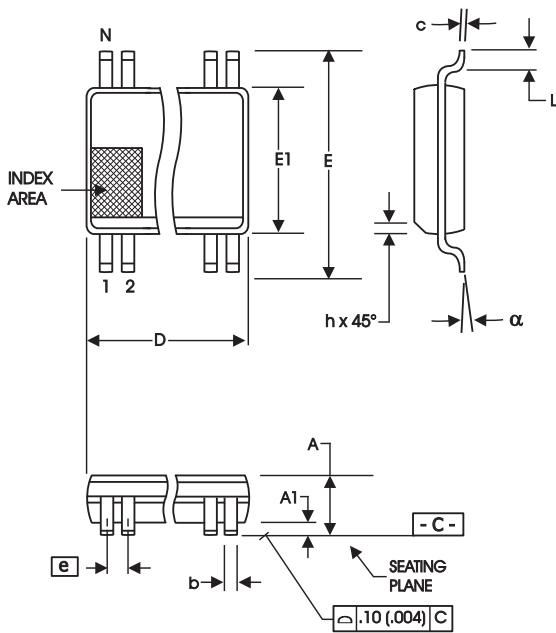
The impact of asserting the CPU\_STOP# pin is all CPU outputs that are set in the I<sup>2</sup>C configuration to be stoppable via assertion of CPU\_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

**Assertion of CPU\_STOP# Waveforms**



**CPU\_STOP# Functionality**

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS				
N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

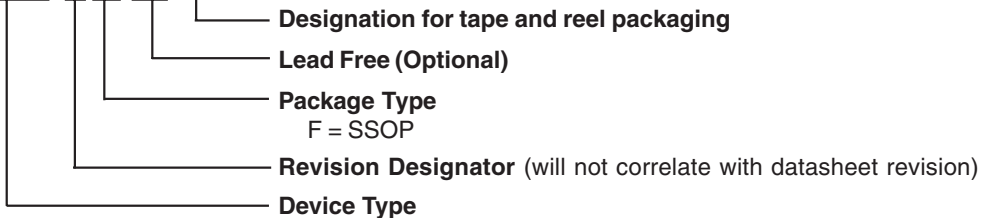
10-0034

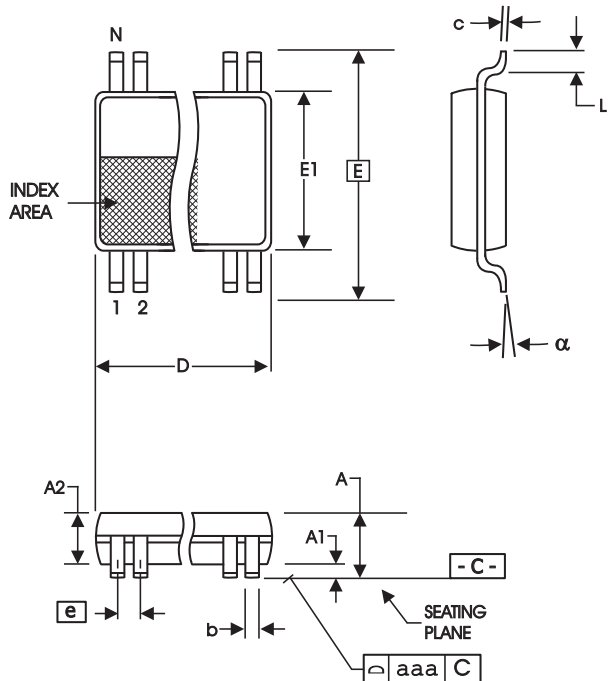
## Ordering Information

950201yFLF-T

Example:

XXXX y F LF-T





6.10 mm. Body, 0.50 mm. pitch TSSOP  
 (240 mil) (0.020 mil)

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
alpha	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

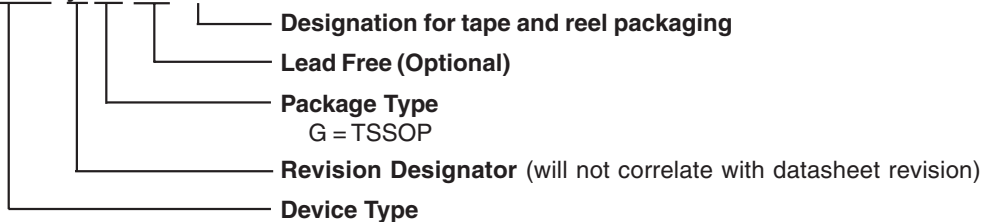
Reference Doc.: JEDEC Publication 95, MO-153  
 10-0039

## Ordering Information

950201yGLF-T

Example:

XXXX y G LF-T



## Revision History

Rev.	Issue Date	Description	Page #
J	1/25/2010	Updated document template	

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