

NUF3101FC

Three Line EMI Filter

This device is a three-line EMI filter array for SIM Card wireless applications. Greater than -25 dB attenuation is obtained at frequencies from 800 MHz to 2.2 GHz. ESD protection is provided across all capacitors.

Features

- EMI Filtering and ESD Protection
- Integration of 10 Discretes
- Provides Protection for IEC61000-4-2 (Level 4)
 - ◆ 8.0 kV (Contact)
 - ◆ 15 kV (Air)
- Flip-Chip Package
- Moisture Sensitivity Level 1
- ESD Rating: Machine Model = C; Human Body Model = 3B
- Pb-Free Package is Available*

Benefits

- Reduces EMI/RFI Emissions on a Data Line
- Integrated Solution Offers Cost and Space Savings
- Reduces Parasitic Inductances Which Offer a More “Ideal” Low Pass Filter Response
- Integrated Solution Improves System Reliability

Applications

- SIM Card
- EMI Filtering and ESD Protection for Data Lines
- Cell Phones
- Handheld Products

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
ESD Discharge IEC61000-4-2	Air Discharge	V _{PP}	15	kV
	Contact Discharge		8.0	
Steady-State Power per Resistor		P _R	100	mW
Steady-State Power per Package		P _T	300	mW
Operating Temperature Range		T _{OP}	-40 to +85	°C
Storage Temperature Range		T _{STG}	-55 to +150	°C
Junction Temperature		T _J	+125	°C

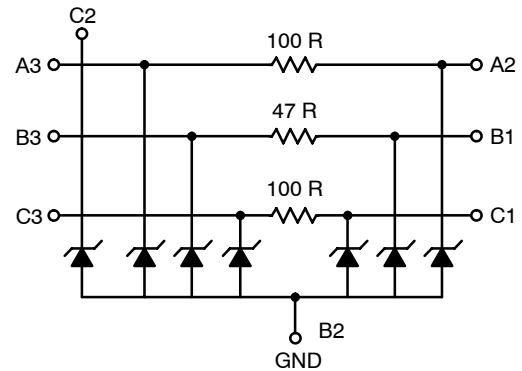
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



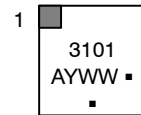
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8-Pin Flip-Chip
FC SUFFIX
CASE 499AG

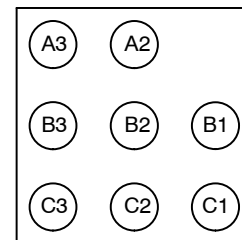
MARKING DIAGRAM



3101 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

Device	Package	Shipping†
NUF3101FCT1	Flip-Chip	3000 Tape & Reel
NUF3101FCT1G	Flip-Chip (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Reverse Working Voltage	V_{RWM}	-	-	-	5.6	V
Breakdown Voltage	V_{BR}	$I_R = 1.0 \text{ mA}$	6.0	-	8.0	V
Leakage Current	I_R	$V_{RM} = 3.0 \text{ V}$	-	-	0.1	μA
Series Resistance	R_1	-	80	100	120	Ω
Series Resistance	R_2	-	38	47	56	Ω
Series Resistance	R_3	-	80	100	120	Ω
Capacitance	$C_{LINE 1}$	$f = 1.0 \text{ MHz}, 0 \text{ Vdc}$	-	-	40	pF
Cut-Off Frequency	f_{3dB}	50 Ω Source and 50 Ω Load Termination	100	-	300	MHz

TYPICAL PERFORMANCE CURVES

($T_A = 25^\circ\text{C}$ unless otherwise specified)

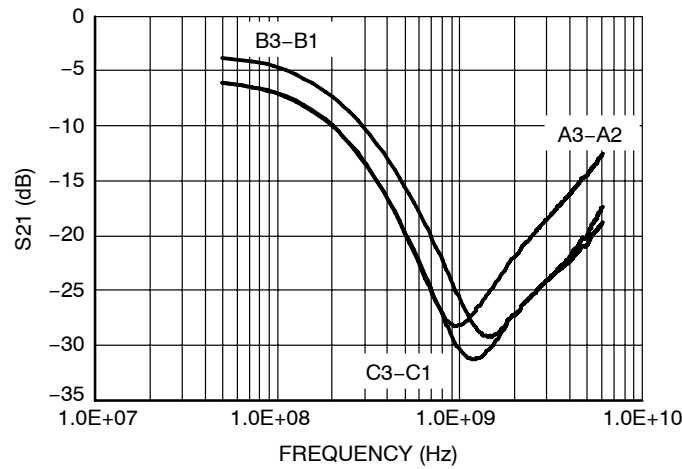


Figure 1. Insertion Loss Characteristics

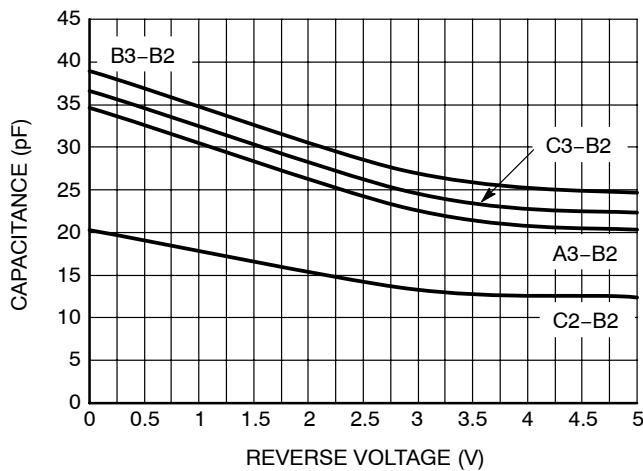


Figure 2. Typical Line Capacitance vs. Reverse Bias Voltage

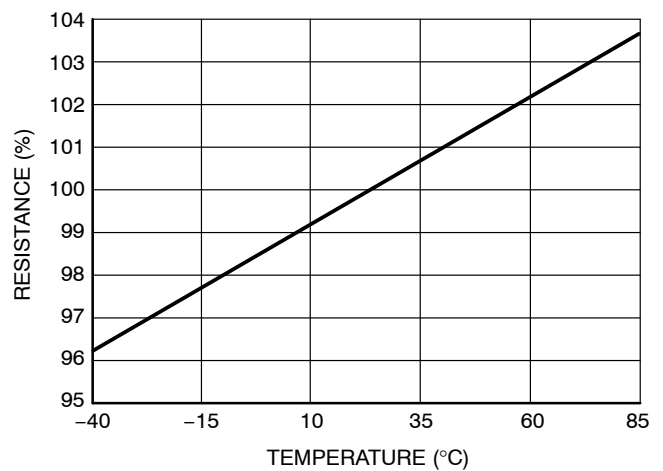


Figure 3. Typical Normalized Resistance Over Temperature

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PRINTED CIRCUIT BOARD RECOMMENDATIONS

Parameter	500 μm Pitch 300 or 350 μm Solder Ball
PCB Pad Size	250 μm +25 -0
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm \pm 25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

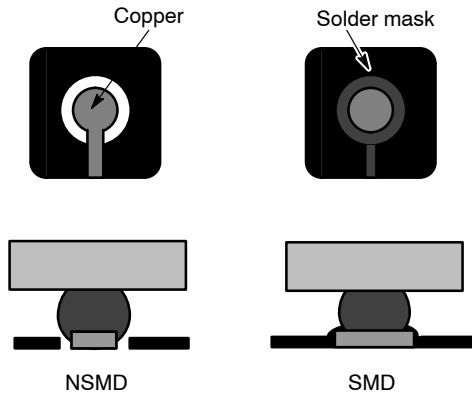


Figure 4. NSMD vs. SMD

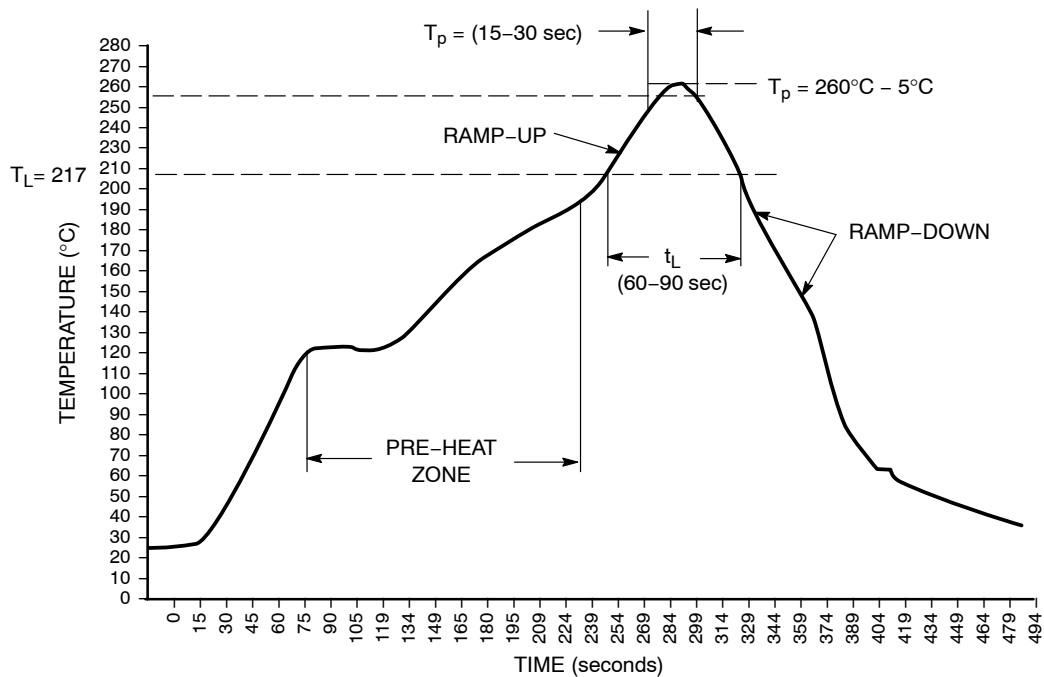
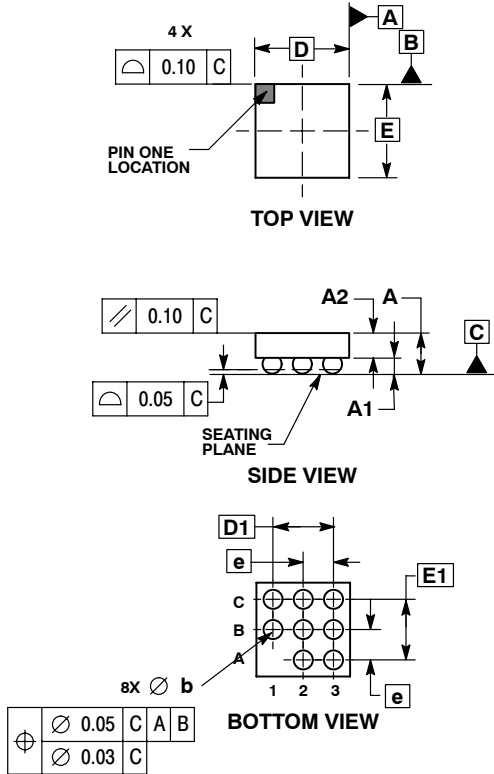


Figure 5. Typical Pb-Free Solder Heating Profile

NUF3101FC

PACKAGE DIMENSIONS

**8 PIN FLIP-CHIP
FC SUFFIX
CASE 499AG-01
ISSUE A**



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.550 BSC	
E	1.550 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

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