

# DTC144TT1

Preferred Devices

## Bias Resistor Transistor

### NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-59 package which is designed for low power surface mount applications.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- ESD Rating: Human Body Model: Class 1  
Machine Model: Class B
- The SC-59 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Pb-Free Package is Available

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mA <sub>dc</sub>

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW  $^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	264 (Note 1) 287 (Note 2)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

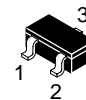
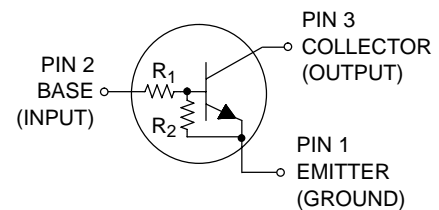
1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



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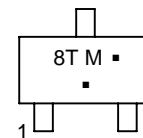
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### NPN SILICON BIAS RESISTOR TRANSISTOR



SC-59  
CASE 318D  
STYLE 1

#### MARKING DIAGRAM



8T = Specific Device Code  
M = Date Code\*  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

# DTC144TT1

## DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
DTC144TT1	8T	47	∞	SC-59	3000/Tape & Reel
DTC144TT1G	8T	47	∞	SC-59 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.2	mAdc
Collector-Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

### ON CHARACTERISTICS (Note 3)

DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)	h <sub>FE</sub>	160	350	–	
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 1 mA)	V <sub>CE(sat)</sub>	–	–	0.25	Vdc
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 3.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OL</sub>	–	–	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.25 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor	R <sub>1</sub>	32.9	47	61.1	kΩ

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

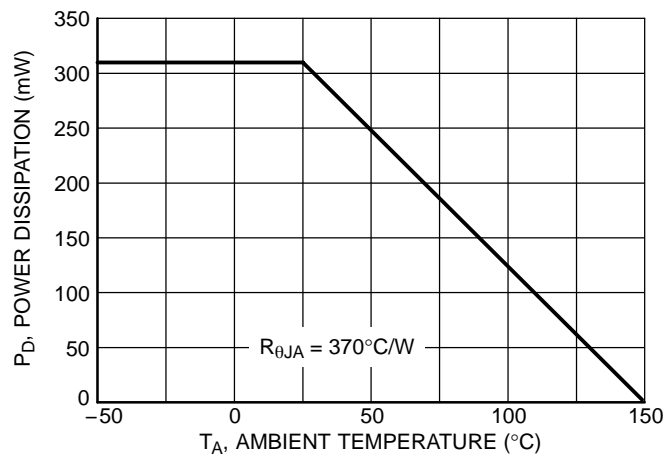


Figure 1. Derating Curve

# DTC144TT1

## TYPICAL APPLICATIONS FOR NPN BRTs

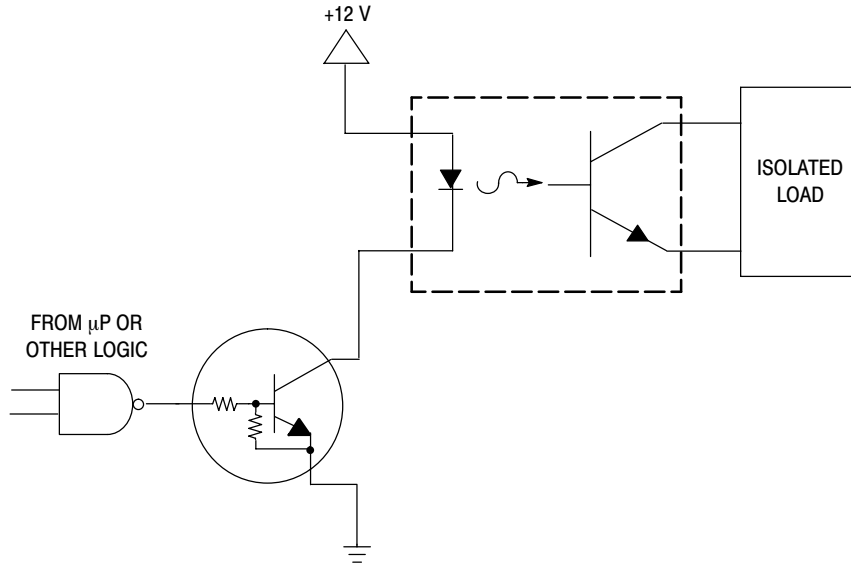


Figure 2. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

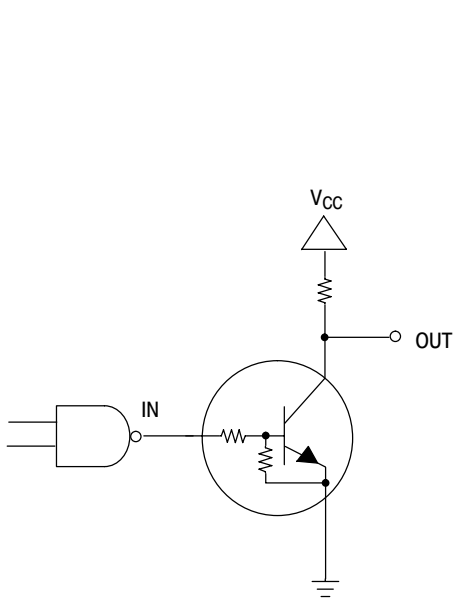


Figure 3. Open Collector Inverter: Inverts the Input Signal

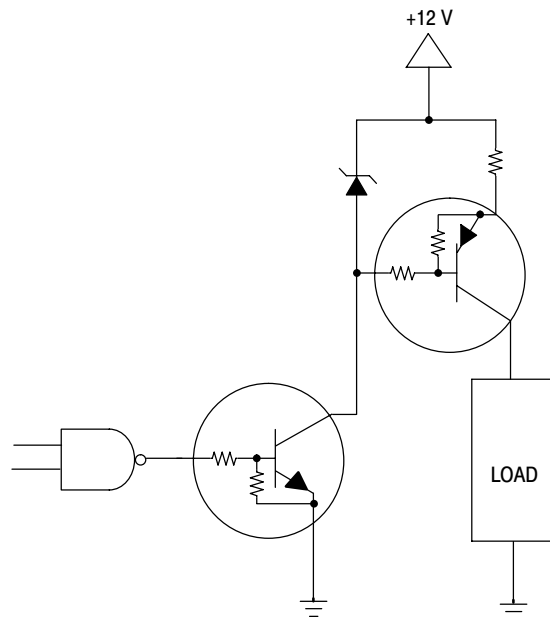
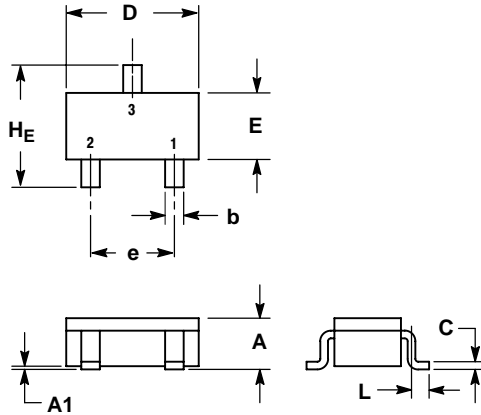


Figure 4. Inexpensive, Unregulated Current Source

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## PACKAGE DIMENSIONS

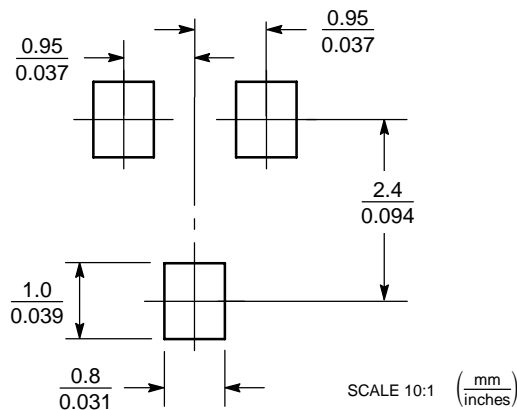
SC-59  
CASE 318D-04  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.15	1.30	0.039	0.045	0.051
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.35	0.43	0.50	0.014	0.017	0.020
c	0.09	0.14	0.18	0.003	0.005	0.007
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	1.70	1.90	2.10	0.067	0.075	0.083
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.80	3.00	0.099	0.110	0.118

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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