

# Switching Power Manager with USB On-The-Go And Overvoltage Protection

## FEATURES

- Bidirectional Switching Regulator Makes Optimal Use of Limited Power Available from USB Port and also Provides a 5V Output for USB On-The-Go
- Overvoltage Protection Guards Against Damage
- 180mΩ Internal Ideal Diode Plus Optional External Ideal Diode Controller Seamlessly Provides Low Loss PowerPath When Input Power is Limited or Unavailable
- Instant-On Operation with Discharged Battery
- Full Featured Li-Ion/Polymer Battery Charger
- Bat-Track™ Adaptive Output Control For Efficient Charging
- 1.2A Max Input Current Limit
- 1.2A Max Charge Current with Thermal Limiting
- Battery Float Voltage: 4.2V (LTC4160), 4.1V (LTC4160-1)
- Low Battery Powered Quiescent Current (8μA)
- 20-pin 3mm × 4mm × 0.75mm QFN Package

## APPLICATIONS

- Media Players and Personal Navigation Devices
- Digital Cameras, PDAs, Smart Phones

## DESCRIPTION

The LTC®4160/LTC4160-1 are high efficiency power management and Li-Ion/Polymer battery charger ICs. They each include a bidirectional switching PowerPath™ controller with automatic load prioritization, a battery charger, and an ideal diode.

The LTC4160/LTC4160-1's bidirectional switching regulator transfers nearly all of the power available from the USB port to the load with minimal loss and heat which eases thermal constraints in small spaces. These devices feature a precision input current limit for USB compatibility and Bat-Track output control for efficient charging. In addition, the ICs can also generate 5V at 500mA for USB On-The-Go applications.

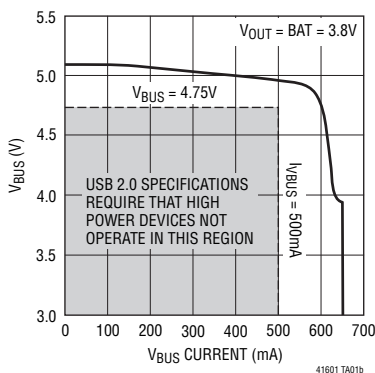
An overvoltage circuit protects the LTC4160/LTC4160-1 from high voltage damage on the USB/wall adapter inputs with an external N-channel MOSFET and a resistor.

The LTC4160/LTC4160-1 are available in a 3mm × 4mm × 0.75mm QFN surface mount package.

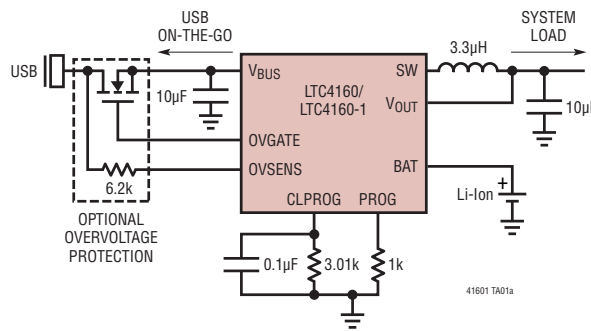
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## TYPICAL APPLICATION

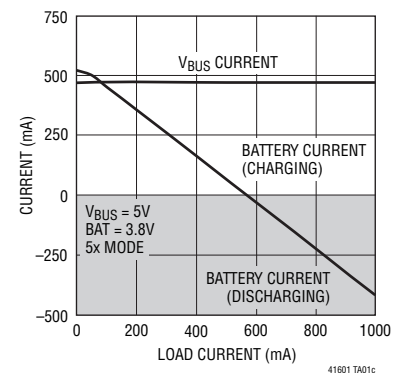
USB OTG V<sub>BUS</sub> Voltage vs V<sub>BUS</sub> Current



High Efficiency Power Manager/Battery Charger with USB On-The-Go and Overvoltage Protection



Battery and V<sub>BUS</sub> Currents vs Load Current



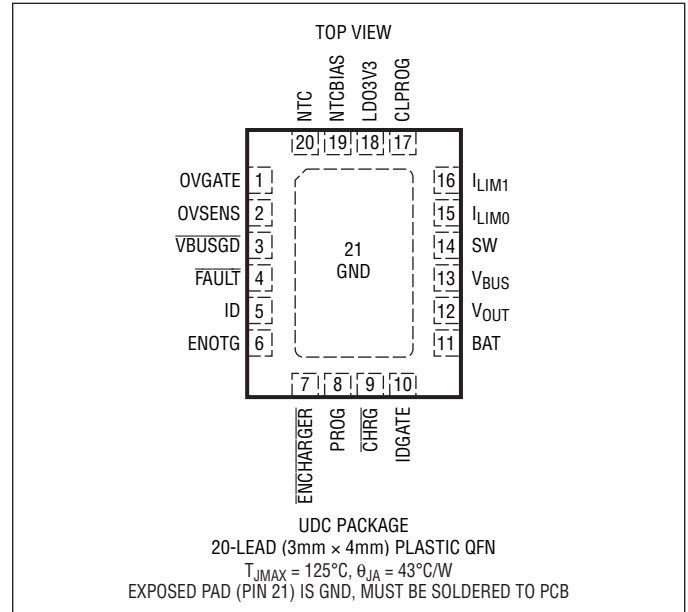
# LTC4160/LTC4160-1

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

$V_{BUS}$ (Transient) $t < 1\text{ms}$ , Duty Cycle $< 1\%$ ..	-0.3V to 7V
$V_{BUS}$ (Static), BAT, $V_{OUT}$ , NTC, ENOTG, ID, ENCHARGER, $V_{BUSGD}$ , FAULT, CHRG.....	-0.3V to 6V
$I_{LIM0}$ , $I_{LIM1}$ .....	-0.3V to $\text{Max}(V_{BUS}, V_{OUT}, \text{BAT}) + 0.3\text{V}$
$I_{OVSENS}$ .....	10mA
$I_{CLPROG}$ .....	3mA
$I_{CHRG}$ , $I_{V_{BUSGD}}$ , $I_{FAULT}$ .....	50mA
$I_{PROG}$ .....	2mA
$I_{LDO3V3}$ .....	30mA
$I_{SW}$ , $I_{BAT}$ , $I_{V_{OUT}}$ , $I_{V_{BUS}}$ .....	2A
Operating Temperature Range.....	-40°C to 85°C
Maximum Junction Temperature.....	125°C
Storage Temperature Range.....	-65°C to 125°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4160EUDC#PBF	LTC4160EUDC#TRPBF	LFX Y	20-Lead (3mm × 4mm) Plastic QFN	-40°C to 85°C
LTC4160EUDC-1#PBF	LTC4160EUDC-1#TRPBF	LFX Z	20-Lead (3mm × 4mm) Plastic QFN	-40°C to 85°C
LTC4160EPDC#PBF	LTC4160EPDC#TRPBF	FDRT	20-Lead (3mm × 4mm) Plastic UTQFN	-40°C to 85°C ( <b>OBSOLETE</b> )
LTC4160EPDC-1#PBF	LTC4160EPDC-1#TRPBF	FDST	20-Lead (3mm × 4mm) Plastic UTQFN	-40°C to 85°C ( <b>OBSOLETE</b> )

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$  (Note 2).  $V_{BUS} = 5\text{V}$ ,  $\text{BAT} = 3.8\text{V}$ ,  $R_{CLPROG} = 3.01\text{k}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PowerPath Switching Regulator – Step-Down Mode</b>						
$V_{BUS}$	Input Supply Voltage		4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current	1x Mode ● 5x Mode ● 10x Mode ● Suspend Mode ●	82 440 900 0.32	90 480 955 0.43	100 500 1000 0.5	mA mA mA mA
$I_{V_{BUSQ}}$ (Note 4)	Input Quiescent Current	1x Mode 5x, 10x Modes Suspend Mode		7 20 0.050		mA mA mA
$h_{CLPROG}$ (Note 4)	Ratio of Measured $V_{BUS}$ Current to $CL_{PROG}$ Program Current	1x Mode 5x Mode 10x Mode Suspend Mode		211 1170 2377 9.6		mA/mA mA/mA mA/mA mA/mA

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{\text{VOUT(PowerPath)}}$	$V_{\text{OUT}}$ Current Available Before Discharging Battery	1x Mode, $\text{BAT} = 3.3\text{V}$ 5x Mode, $\text{BAT} = 3.3\text{V}$ 10x Mode, $\text{BAT} = 3.3\text{V}$ Suspend Mode	0.26	121 667 1217 0.34	0.43	mA mA mA mA
$V_{\text{CLPROG}}$	CLPROG Servo Voltage in Current Limit	Switching Modes Suspend Mode		1.183 100		V mV
$V_{\text{UVLO}}$	$V_{\text{BUS}}$ Undervoltage Lockout	Rising Threshold Falling Threshold	3.95	4.3 4	4.35	V V
$V_{\text{DUVLO}}$	$V_{\text{BUS}}$ To $\text{BAT}$ Differential Undervoltage Lockout	Rising Threshold Falling Threshold		200 50		mV mV
$V_{\text{OUT}}$	$V_{\text{OUT}}$ Voltage	1x, 5x, 10x Modes, $0\text{V} < \text{BAT} \leq 4.2\text{V}$ , $I_{\text{VOUT}} = 0\text{mA}$ , Battery Charger Off USB Suspend Mode, $I_{\text{VOUT}} = 250\mu\text{A}$	3.5 4.5	$\text{BAT} + 0.3$ 4.6	4.7 4.7	V V
$f_{\text{OSC}}$	Switching Frequency		1.8	2.25	2.7	MHz
$R_{\text{PMOS\_POWERPATH}}$	PMOS On-Resistance			0.18		$\Omega$
$R_{\text{NMOS\_POWERPATH}}$	NMOS On-Resistance			0.3		$\Omega$
$I_{\text{PEAK\_POWERPATH}}$	Peak Inductor Current Clamp	1x Mode (Note 5) 5x Mode (Note 5) 10x Mode (Note 5)		1 1.6 3		A A A
$R_{\text{SUSP}}$	Suspend LDO Output Resistance	Closed Loop		10		$\Omega$

### PowerPath Switching Regulator – Step-Up Mode (USB On-The-Go)

$V_{\text{BUS}}$	Output Voltage	$0 \leq I_{\text{VBUS}} \leq 500\text{mA}$ , $V_{\text{OUT}} > 3.2\text{V}$		4.75	5.25	V
$V_{\text{OUT}}$	Input Voltage			2.9	4.2	V
$I_{\text{VBUS}}$	Output Current Limit		● 550	680		mA
$I_{\text{PEAK}}$	Peak Inductor Current Limit	(Note 5)		1.8		A
$I_{\text{OTGQ}}$	$V_{\text{OUT}}$ Quiescent Current	$V_{\text{OUT}} = 3.8\text{V}$ , $I_{\text{VBUS}} = 0\text{mA}$ (Note 6)		1.6		mA
$V_{\text{CLPROG}}$	Output Current Limit Servo Voltage			1.15		V
$V_{\text{OUTUVLO}}$	$V_{\text{OUT}}$ UVLO – $V_{\text{OUT}}$ Falling $V_{\text{OUT}}$ UVLO – $V_{\text{OUT}}$ Rising		2.5	2.6 2.8	2.9	V V
$t_{\text{SCFAULT}}$	Short Circuit Fault Delay	PMOS Switch Off		7.2		ms

### Overvoltage Protection

$V_{\text{OVCTOFF}}$	Overvoltage Protection Threshold	With 6.2k Series Resistor		6.1	6.42	6.7	V
$V_{\text{OVGATE}}$	OVGATE Output Voltage	$V_{\text{OVSENS}} < V_{\text{OVCTOFF}}$ $V_{\text{OVSENS}} > V_{\text{OVCTOFF}}$		$1.88 \cdot V_{\text{OVSENS}}$ 0	12		V V
$t_{\text{RISE}}$	OVGATE Time To Reach Regulation	OVGATE $C_{\text{LOAD}} = 1\text{nF}$		1.25			ms

### Battery Charger

$V_{\text{FLOAT}}$	BAT Regulated Output Voltage	LTC4160	● 4.179 4.165	4.2 4.2	4.221 4.235	V V
		LTC4160-1	● 4.079 4.065	4.1 4.1	4.121 4.135	V V
$I_{\text{CHG}}$	Constant Current Mode Charger Current	$R_{\text{PROG}} = 845\Omega$ , 10x Mode $R_{\text{CLPROG}} \leq 2.49\text{k}$ $R_{\text{PROG}} = 5\text{k}$ , 5x or 10x Mode	1120 185	1219 206	1320 223	mA mA
$I_{\text{BAT}}$	Battery Drain Current	$V_{\text{BUS}} > V_{\text{UVLO}}$ , Suspend Mode, $I_{\text{VOUT}} = 0\mu\text{A}$		3.8	6	$\mu\text{A}$
		$V_{\text{BUS}} = 0\text{V}$ , $I_{\text{VOUT}} = 0\mu\text{A}$ (Ideal Diode Mode)		8	12	$\mu\text{A}$

# LTC4160/LTC4160-1

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2).  $V_{\text{BUS}} = 5\text{V}$ ,  $\text{BAT} = 3.8\text{V}$ ,  $R_{\text{CLPROG}} = 3.01\text{k}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{PROG}}$	PROG Pin Servo Voltage			1		V
$V_{\text{PROG\_TRKL}}$	PROG Pin Servo Voltage in Trickle Charge	$\text{BAT} < V_{\text{TRKL}}$		0.1		V
$V_{\text{C/10}}$	C/10 Threshold Voltage at PROG			100		mV
$h_{\text{PROG}}$	Ratio of $I_{\text{BAT}}$ to PROG Pin Current			1030		mA/mA
$I_{\text{TRKL}}$	Trickle Charge Current	$\text{BAT} < V_{\text{TRKL}}$		100		mA
$V_{\text{TRKL}}$	Trickle Charge Threshold Voltage	BAT Rising	2.7	2.85	3	V
$\Delta V_{\text{TRKL}}$	Trickle Charge Hysteresis Voltage			135		mV
$\Delta V_{\text{RECHRG}}$	Recharge Battery Threshold Voltage	Threshold Voltage Relative to $V_{\text{FLOAT}}$	-75	-100	-125	mV
$t_{\text{TERM}}$	Safety Timer Termination Period	Timer Starts when $V_{\text{BAT}} = V_{\text{FLOAT}}$	3.9	4.3	5.4	Hour
$t_{\text{BADBAT}}$	Bad Battery Termination Time	$\text{BAT} < V_{\text{TRKL}}$	0.4	0.5	0.6	Hour
$h_{\text{C/10}}$	End of Charge Current Ratio	(Note 7)	0.085	0.1	0.115	mA/mA
$R_{\text{ON\_CHG}}$	Battery Charger Power FET On-Resistance (Between $V_{\text{OUT}}$ and BAT)			0.18		$\Omega$
$T_{\text{LIM}}$	Junction Temperature in Constant Temperature Mode			110		$^\circ\text{C}$

## NTC

$V_{\text{COLD}}$	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis	75	76.5 1.5	78	%NTCBIAS %NTCBIAS
$V_{\text{HOT}}$	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis	33.4	34.9 1.8	36.4	%NTCBIAS %NTCBIAS
$V_{\text{DIS}}$	NTC Disable Threshold Voltage	Falling Threshold Hysteresis	0.7	1.7 50	2.7	%NTCBIAS mV
$I_{\text{NTC}}$	NTC Leakage Current	$\text{NTC} = \text{NTCBIAS} = 5\text{V}$	-50		50	nA

## Ideal Diode

$V_{\text{FWD}}$	Forward Voltage Detection	$V_{\text{BUS}} = 0\text{V}$ , $I_{\text{VOUT}} = 10\text{mA}$ $I_{\text{VOUT}} = 10\text{mA}$		2 15		mV mV
$R_{\text{DROPOUT}}$	Internal Diode On-Resistance, Dropout	$I_{\text{VOUT}} = 200\text{mA}$		0.18		$\Omega$
$I_{\text{MAX\_DIODE}}$	Diode Current Limit		2			A

## Always On 3.3V LDO Supply

$V_{\text{LD03V3}}$	Regulated Output Voltage	$0\text{mA} < I_{\text{LD03V3}} < 20\text{mA}$	3.1	3.3	3.5	V
$R_{\text{CL\_LD03V3}}$	Closed-Loop Output Resistance			2.7		$\Omega$
$R_{\text{OL\_LD03V3}}$	Dropout Output Resistance			23		$\Omega$

## Logic ( $I_{\text{LIM0}}$ , $I_{\text{LIM1}}$ , ID, ENOTG, ENCHARGER)

$V_{\text{IL}}$	Logic Low Input Voltage				0.4	V
$V_{\text{IH}}$	Logic High Input Voltage		1.2			V
$I_{\text{PD1}}$	$I_{\text{LIM0}}$ , $I_{\text{LIM1}}$ , ENOTG, ENCHARGER Pull-Down Current			1.8		$\mu\text{A}$
$I_{\text{PU1}}$	ID Pull-Up Current			2.5		$\mu\text{A}$

## Status Outputs (CHRG, VBUSGD, FAULT)

$V_{\text{VBUSGD}}$	Output Low Voltage	$I_{\text{VBUSGD}} = 5\text{mA}$ , $V_{\text{BUS}} = 5\text{V}$		65	100	mV
$V_{\text{CHRG}}$ , $V_{\text{FAULT}}$	Output Low Voltage	$I_{\text{CHRG}} = I_{\text{FAULT}} = 5\text{mA}$ , $V_{\text{OUT}} = 3.8\text{V}$		100	150	mV
$I_{\text{CHRG}}$ , $I_{\text{VBUSGD}}$ , $I_{\text{FAULT}}$	Leakage Current	$V_{\text{CHRG}} = V_{\text{VBUSGD}} = V_{\text{FAULT}} = 5\text{V}$			1	$\mu\text{A}$

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## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4160E/LTC4160E-1 are guaranteed to meet specifications from 0°C to 85°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** The LTC4160E/LTC4160E-1 include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 4:** Total input current is the sum of quiescent current,  $I_{VBUSQ}$ , and measured current given by  $V_{CLPROG}/R_{CLPROG} \cdot (I_{CLPROG} + 1)$ .

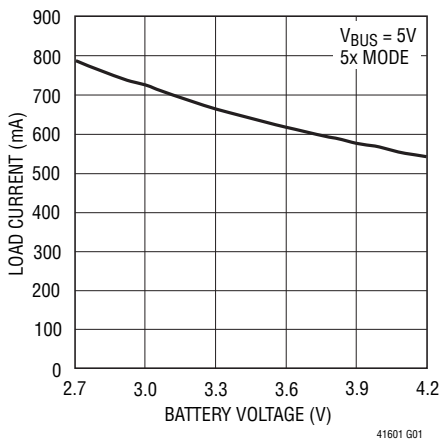
**Note 5:** The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

**Note 6:** The bidirectional switcher's supply current is bootstrapped to  $V_{BUS}$  and in the application will reflect back to  $V_{OUT}$  by  $(V_{BUS}/V_{OUT}) \cdot 1/\text{efficiency}$ . Total quiescent current is the sum of the current into the  $V_{OUT}$  pin plus the reflected current.

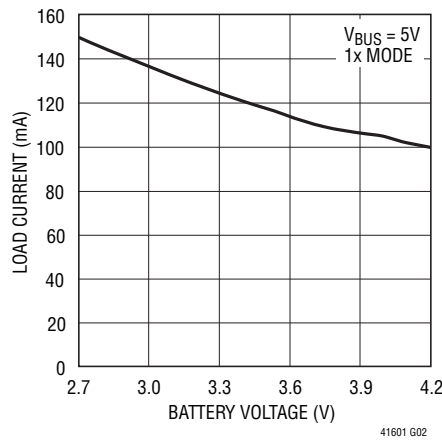
**Note 7:**  $h_{C/10}$  is expressed as a fraction of the measured full charge current with indicated PROG resistor.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

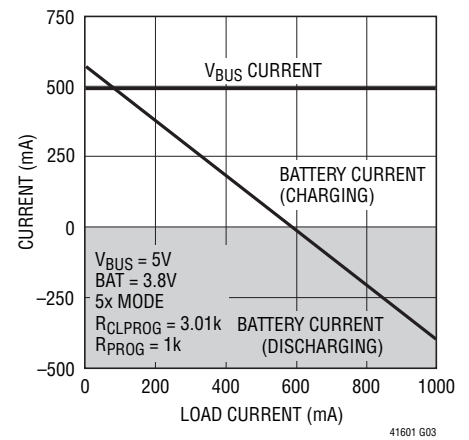
USB Limited Load Current vs Battery Voltage (Battery Charger Disabled)



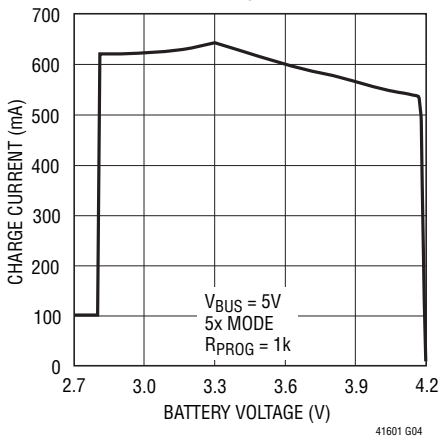
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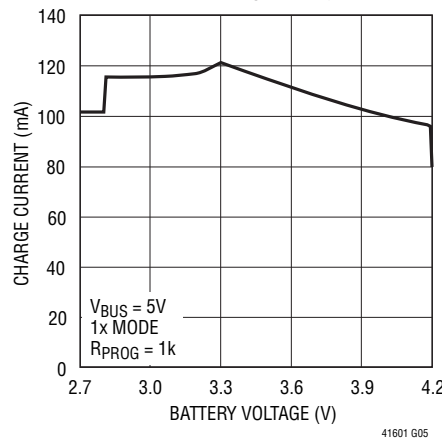
Battery and  $V_{BUS}$  Currents vs Load Current



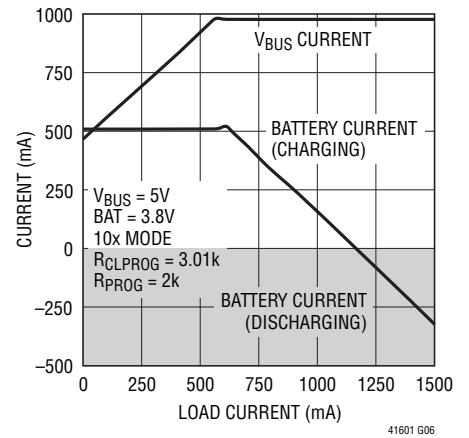
USB Limited Battery Charge Current vs Battery Voltage



USB Limited Battery Charge Current vs Battery Voltage

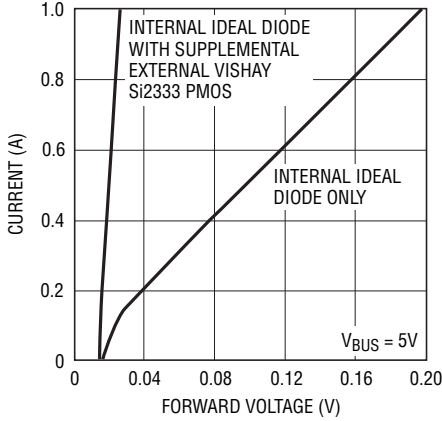


Battery and  $V_{BUS}$  Currents vs Load Current

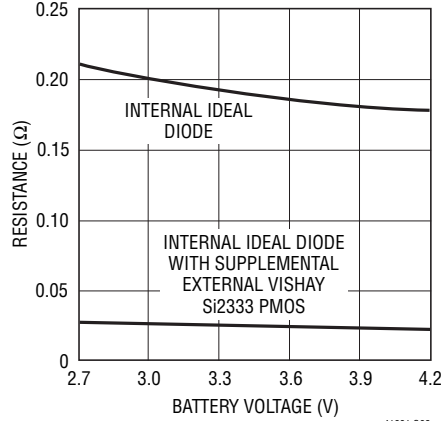


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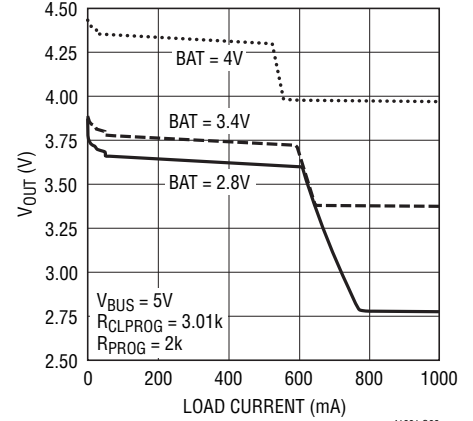
### Ideal Diode V-I Characteristics



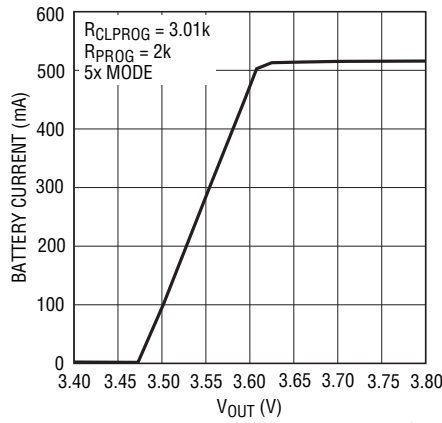
### Ideal Diode Resistance vs Battery Voltage



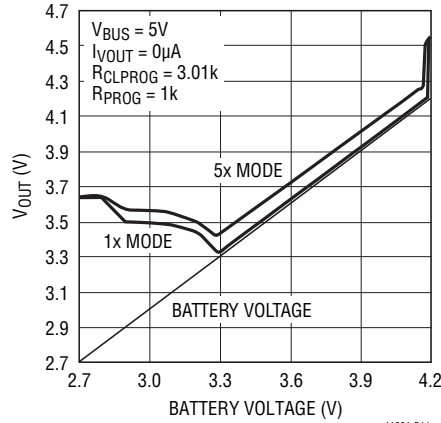
### V<sub>OUT</sub> Voltage vs Load Current (Battery Charger Disabled)



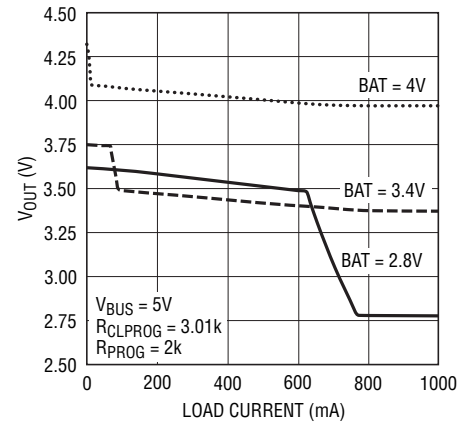
### Battery Charge Current vs V<sub>OUT</sub> Voltage



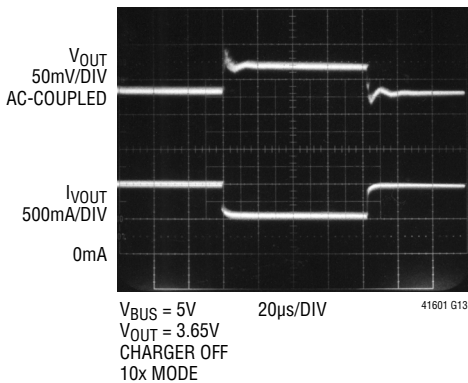
### V<sub>OUT</sub> Voltage vs Battery Voltage (Charger Overprogrammed)



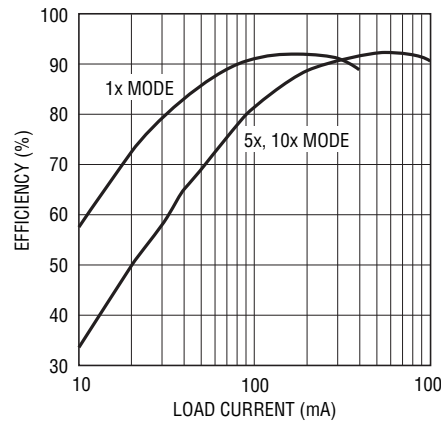
### V<sub>OUT</sub> Voltage vs Load Current (Battery Charger Enabled)



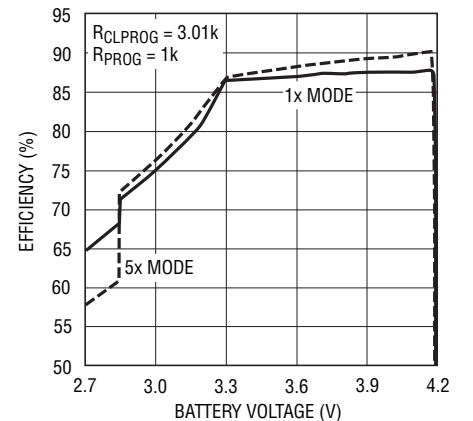
### PowerPath Switching Regulator Transient Response



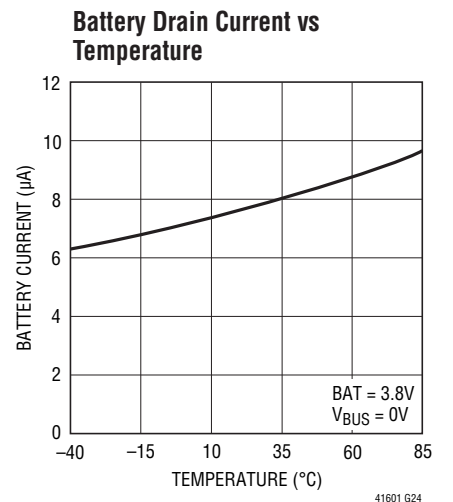
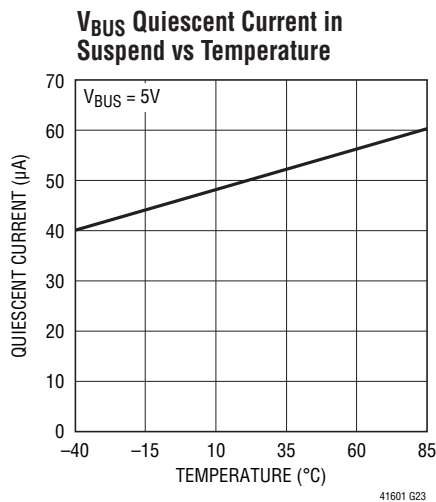
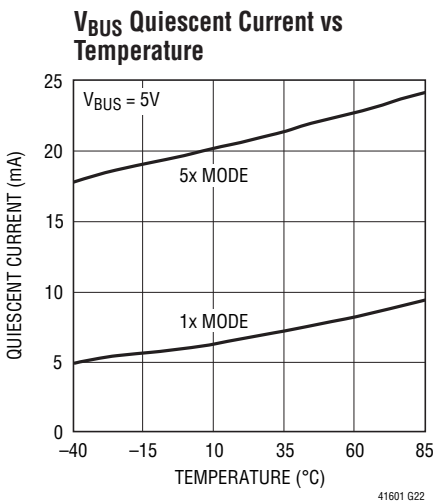
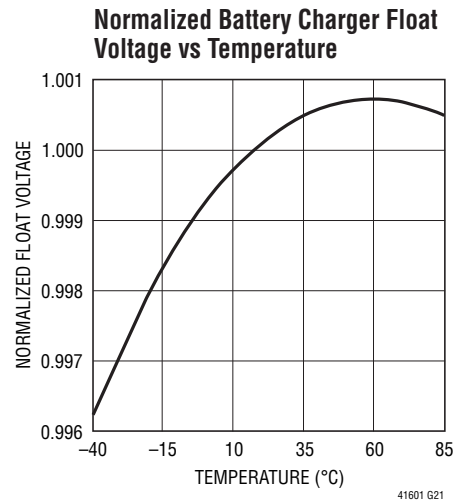
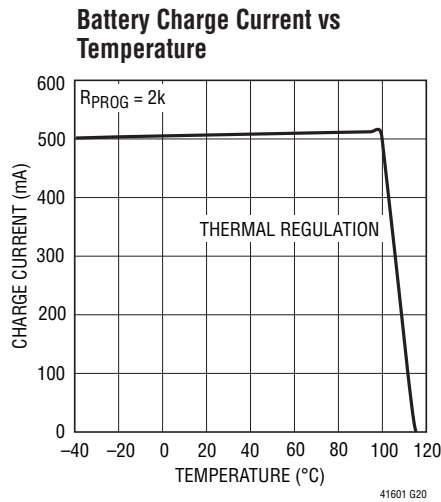
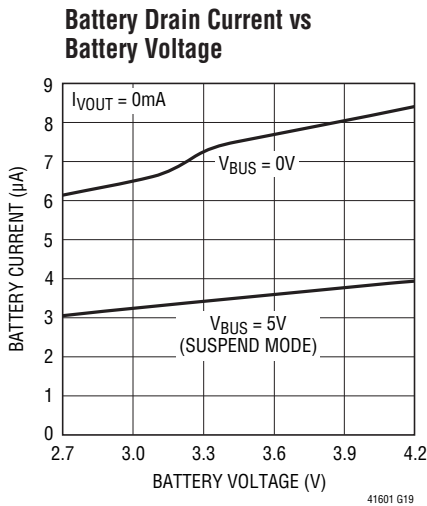
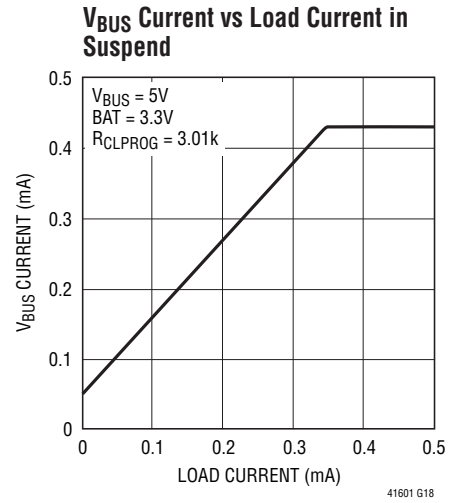
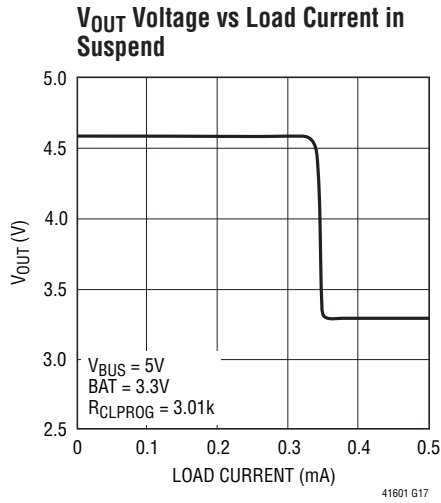
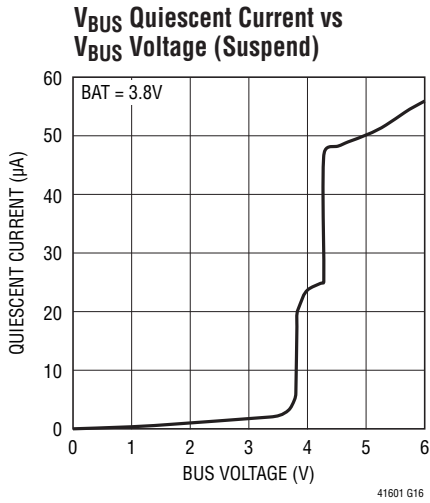
### PowerPath Switching Regulator Efficiency vs Load Current



### Battery Charging Efficiency vs Battery Voltage with No External Load ( $P_{BAT}/P_{V_{BUS}}$ )

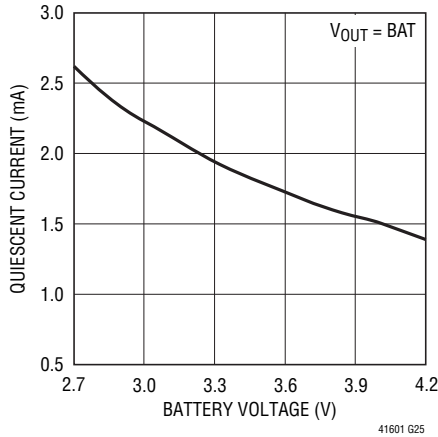


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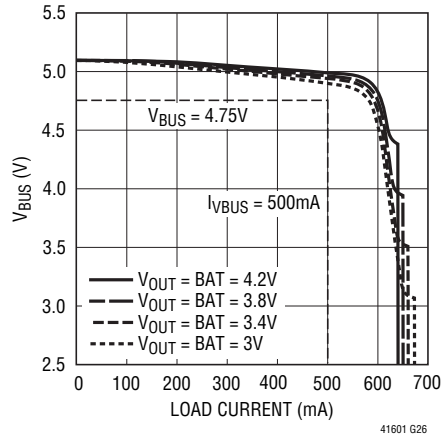


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

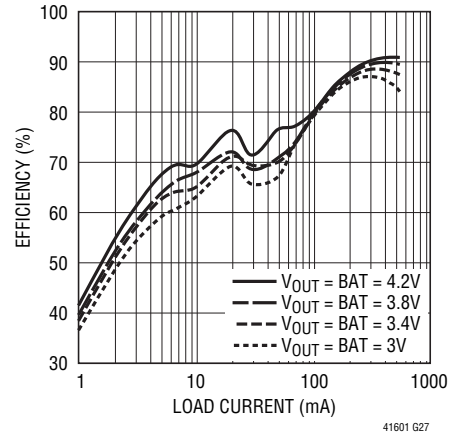
**OTG Boost Quiescent Current vs Battery Voltage**



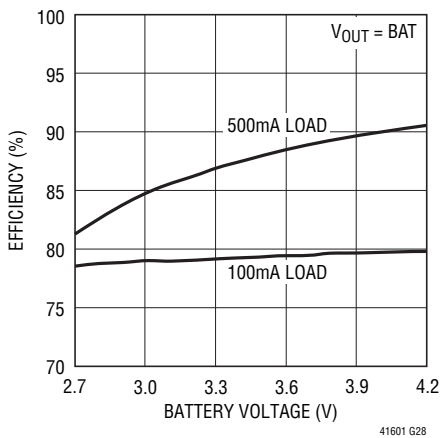
**OTG Boost  $V_{BUS}$  Voltage vs Load Current**



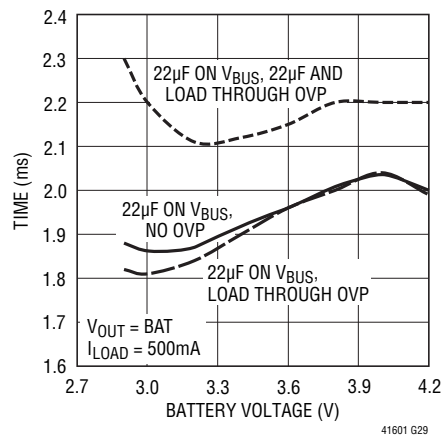
**OTG Boost Efficiency vs Load Current**



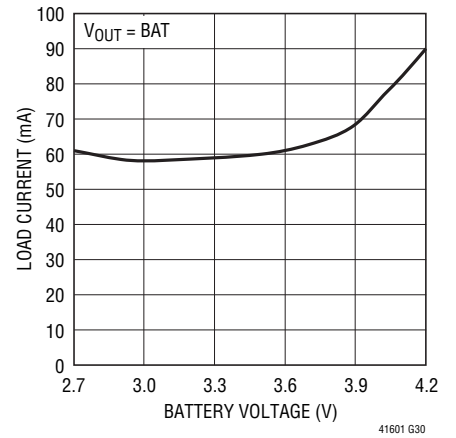
**OTG Boost Efficiency vs Battery Voltage**



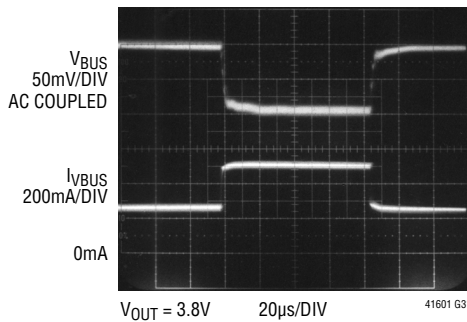
**OTG Boost Start-Up Time into Current Source Load vs Battery Voltage**



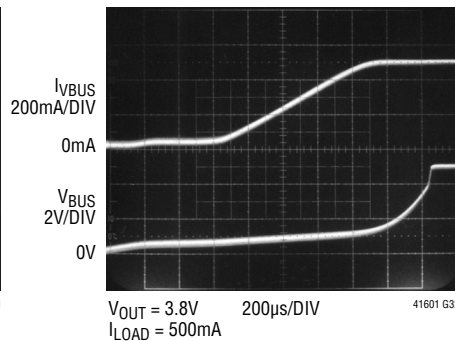
**OTG Boost Burst Mode Current Threshold vs Battery Voltage**



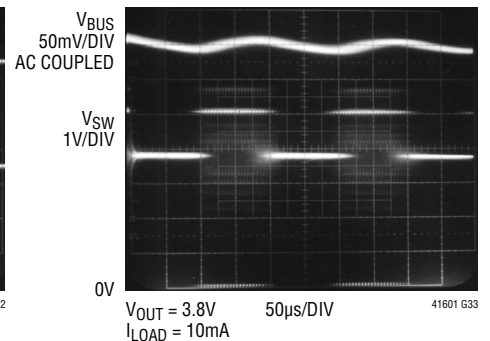
**OTG Boost Transient Response**



**OTG Boost Start-Up into Current Source Load**



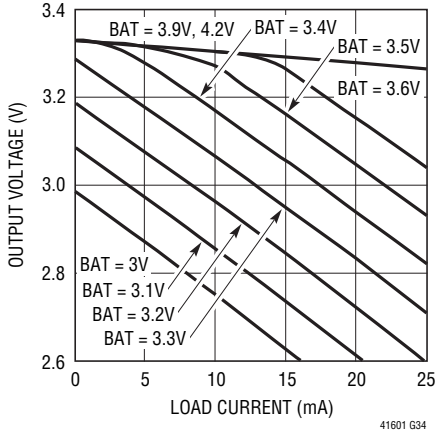
**OTG Boost Burst Mode Operation**



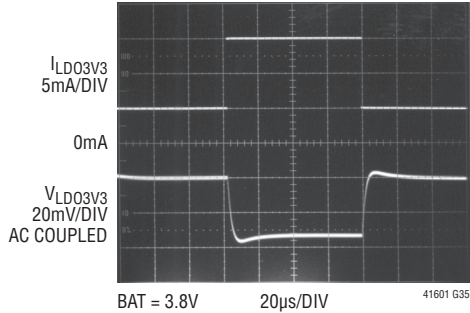


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

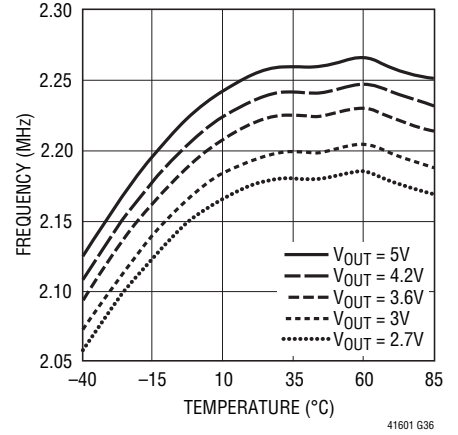
**3.3V LDO Output Voltage vs Load Current,  $V_{BUS} = 0\text{V}$**



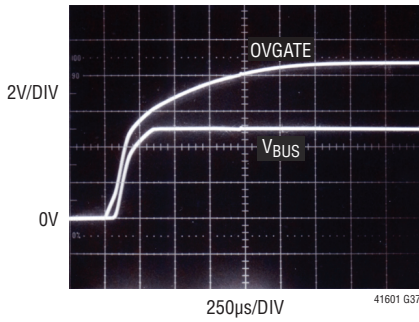
**3.3V LDO Step Response (5mA to 15mA)**



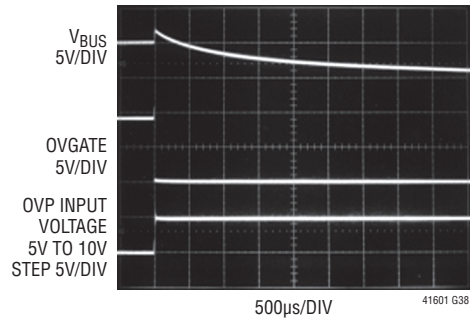
**Oscillator Frequency vs Temperature**



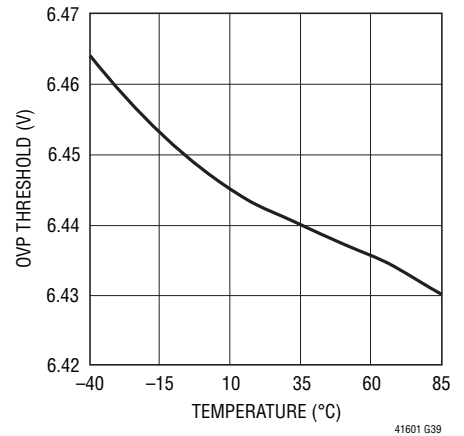
**OVP Connect Waveform**



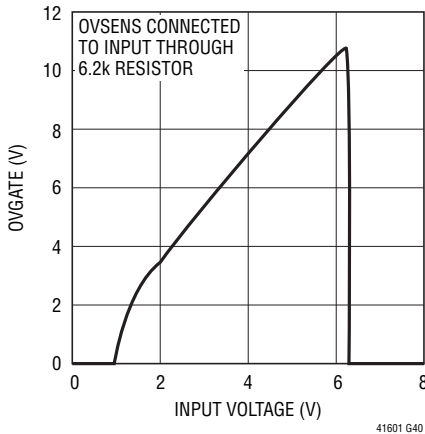
**OVP Disconnect Waveform**



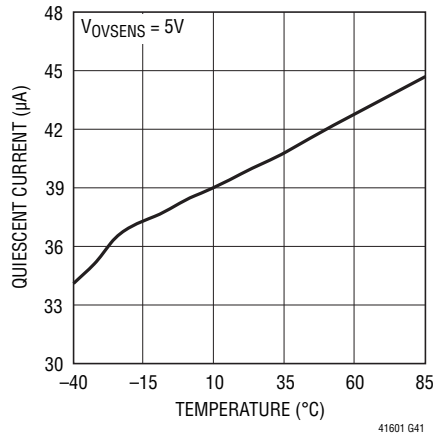
**Rising OVP Threshold vs Temperature**



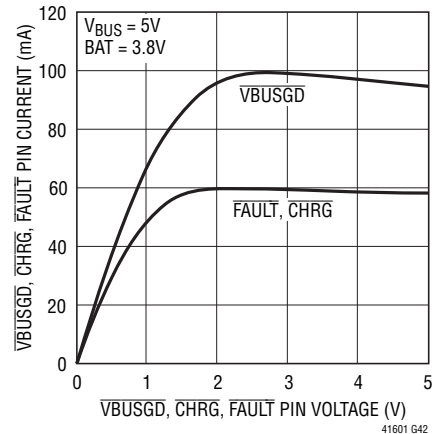
**OVGATE vs OVSENS**



**OVSENS Quiescent Current vs Temperature**



**$\overline{VBUSGD}$ ,  $\overline{CHRG}$ ,  $\overline{FAULT}$  Pin Current vs Voltage (Pull-Down State)**



## PIN FUNCTIONS

**OVGATE (Pin 1):** Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOSFET. The source of the transistor should be connected to  $V_{BUS}$  and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance the MOSFET. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage to the LTC4160/LTC4160-1. OVGATE works in conjunction with OVSENS to provide this protection.

**OVSENS (Pin 2):** Overvoltage Protection Sense Input. OVSENS should be connected through a 6.2k resistor to the input power connector and the drain of an external N-channel MOSFET. When the voltage on this pin exceeds  $V_{OVCTOFF}$ , the OVGATE pin will be pulled to GND to disable the MOSFET and protect the LTC4160/LTC4160-1. The OVSENS pin shunts current during an overvoltage transient in order to keep the pin voltage at 6V.

**VBUSGD (Pin 3):** Logic Output. This is an open-drain output which indicates that  $V_{BUS}$  is above  $V_{UVLO}$  and  $V_{DUVLO}$ . VBUSGD requires a pull-up resistor and/or LED to provide indication.

**FAULT (Pin 4):** Logic Output. This is an open-drain output which indicates a bad battery fault when the charger is enabled or a short circuit condition on  $V_{BUS}$  when the bidirectional PowerPath switching regulator is in step-up mode (On-The-Go). FAULT requires a pull-up resistor and/or LED to provide indication.

**ID (Pin 5):** Logic Input. This pin independently enables the bidirectional switching regulator to step-up the voltage on  $V_{OUT}$  and provide a 5V output on the  $V_{BUS}$  pin for USB On-The-Go applications. If the host does not power down  $V_{BUS}$  then connect this pin directly to the ID pin of a USB micro-AB receptacle. Active low. Has an internal 2.5 $\mu$ A pull-up current source.

**ENOTG (Pin 6):** Logic Input. This pin independently enables the bidirectional switching regulator to step-up the voltage on  $V_{OUT}$  and provide a 5V output on the  $V_{BUS}$  pin for USB On-The-Go applications. Active high. Has an internal 1.8 $\mu$ A pull-down current source.

**ENCHARGER (Pin 7):** Logic Input. This pin enables the battery charger. Active low. Has an internal 1.8 $\mu$ A pull-down current source.

**PROG (Pin 8):** Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor from PROG to ground, programs the charge current. If sufficient input power is available in constant-current mode, this pin serves to 1V. The voltage on this pin always represents the actual charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \cdot 1030$$

**CHRG (Pin 9):** Logic Output. This is an open-drain output that indicates whether the battery is charging or not charging. CHRG requires a pull-up resistor and/or LED to provide indication.

**IDGATE (Pin 10):** Ideal Diode Amplifier Output. This pin controls the gate of an optional external P-channel MOSFET used as an ideal diode between  $V_{OUT}$  and BAT. The external ideal diode operates in parallel with the internal ideal diode. The source of the P-channel MOSFET should be connected to  $V_{OUT}$  and the drain should be connected to BAT. If the external ideal diode MOSFET is not used, IDGATE should be left floating.

**BAT (Pin 11):** Single Cell Li-Ion Battery Pin. Depending on available  $V_{BUS}$  power, a Li-Ion battery on BAT will either deliver power to  $V_{OUT}$  through the ideal diode or be charged from  $V_{OUT}$  via the battery charger.

**$V_{OUT}$  (Pin 12):** Output Voltage of the Bidirectional Power-Path Switching Regulator in Step-Down Mode and Input Voltage of the Battery Charger. The majority of the portable product should be powered from  $V_{OUT}$ . The LTC4160/LTC4160-1 will partition the available power between the external load on  $V_{OUT}$  and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to  $V_{OUT}$  ensures that  $V_{OUT}$  is powered even if the load exceeds the allotted power from  $V_{BUS}$  or if the  $V_{BUS}$  power source is removed. In On-The-Go mode, this pin delivers power to  $V_{BUS}$  via the SW pin.  $V_{OUT}$  should be bypassed with a low impedance multilayer ceramic capacitor.

## PIN FUNCTIONS

**V<sub>BUS</sub> (Pin 13):** Power Pin. This pin delivers power to V<sub>OUT</sub> via the SW pin by drawing controlled current from a DC source such as a USB port or DC output wall adapter. In On-The-Go mode this pin provides power to external loads. Bypass V<sub>BUS</sub> with a low impedance multilayer ceramic capacitor.

**SW (Pin 14):** The SW pin transfers power between V<sub>BUS</sub> to V<sub>OUT</sub> via the bidirectional switching regulator. See the Applications Information section for a discussion of inductance value and current rating.

**I<sub>LIM0</sub>, I<sub>LIM1</sub> (Pins 15, 16):** I<sub>LIM0</sub> and I<sub>LIM1</sub> control the V<sub>BUS</sub> input current limit of the bidirectional PowerPath switching regulator in step-down mode. See Table 1. Each has an internal 1.8μA pull-down current source.

**CLPROG (Pin 17):** USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn or sourced from the V<sub>BUS</sub> pin. A precise fraction, h<sub>CLPROG</sub>, of the V<sub>BUS</sub> current is sent to the CLPROG pin when the PMOS switch of the bidirectional PowerPath switching regulator is on. The switching regulator delivers power until the CLPROG pin reaches 1.18V in step-down mode and 1.15V in step-up mode. When the switching regulator is in step-down mode, CLPROG is used to regulate the average input current. Several V<sub>BUS</sub> current limit settings are available via user input which will typically correspond to the 500mA and 100mA USB specifications. When the switching regulator is in step-up mode (USB On-The-Go), CLPROG is used to limit the average output current to 680mA. A multilayer ceramic averaging capacitor or R-C network is required at CLPROG for filtering.

**LDO3V3 (Pin 18):** 3.3V LDO Output Pin. This pin provides a regulated always-on 3.3V supply voltage. LDO3V3 gets its power from V<sub>OUT</sub>. It may be used for light loads such as a watch dog microprocessor or real time clock. A 1μF capacitor is required from LDO3V3 to ground. If the LDO3V3 output is not used it should be disabled by connecting it to V<sub>OUT</sub>.

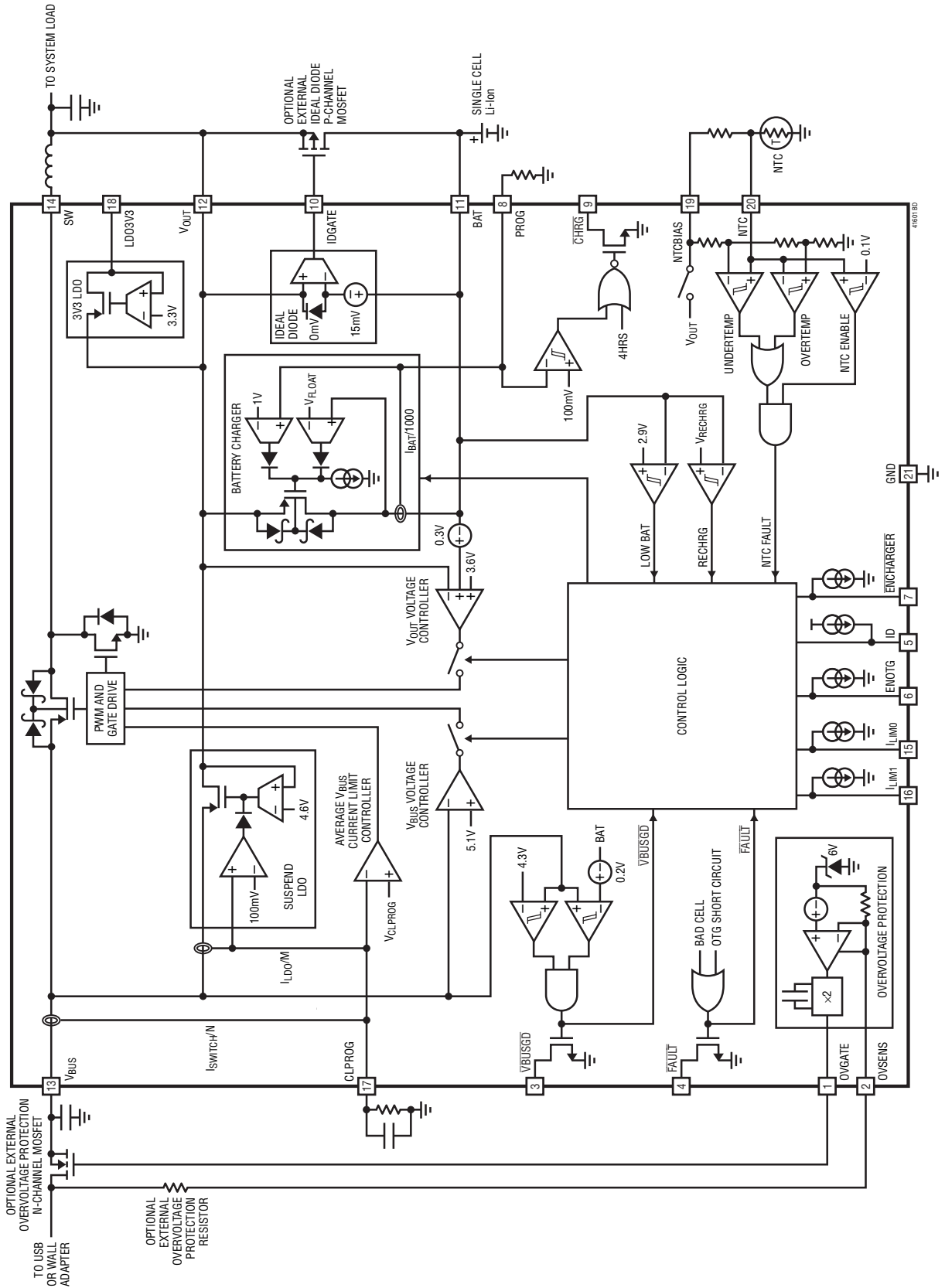
**NTCBIAS (Pin 19):** NTC Thermistor Bias Output. If NTC operation is desired, connect a bias resistor between NTCBIAS and NTC, and an NTC thermistor between NTC and GND. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

**NTC (Pin 20):** Input to the Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor, which is typically co-packaged with the battery, to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

**GND (Exposed Pad Pin 21):** Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC4160/LTC4160-1.

# LTC4160/LTC4160-1

## BLOCK DIAGRAM



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## OPERATION

### Introduction

The LTC4160/LTC4160-1 are high efficiency bidirectional switching power managers and Li-Ion/Polymer battery chargers designed to make optimal use of the power available while minimizing power dissipation and easing thermal budgeting constraints. The innovative PowerPath architecture ensures that the end product application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the end product.

When acting as a step-down converter, the LTC4160/LTC4160-1's bidirectional switching regulator takes power from USB, wall adapters, or other 5V sources and provides power to the end product application and efficiently charges the battery using Bat-Track. Because power is conserved, the LTC4160/LTC4160-1 allow the load current on  $V_{OUT}$  to exceed the current drawn by the USB port, making maximum use of the allowable USB power for battery charging. For USB compatibility, the switching regulator includes a precision average input current limit. The bidirectional switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

In addition, the bidirectional switching regulator can also operate as a 5V synchronous step-up converter, taking power from  $V_{OUT}$  and delivering up to 500mA to  $V_{BUS}$  without the need for any additional external components. This enables systems with USB dual-role transceivers to function as USB On-The-Go dual-role devices. True output disconnect and average output current limit features are included for short circuit protection.

The LTC4160/LTC4160-1 contain both an internal 180m $\Omega$  ideal diode as well as an ideal diode controller for use with an external P-channel MOSFET. The ideal diodes from BAT to  $V_{OUT}$  guarantee that ample power is always available to  $V_{OUT}$  even if there is insufficient or absent power at  $V_{BUS}$ .

An always-on LDO provides a regulated 3.3V from available power at  $V_{OUT}$ . Drawing very little quiescent current, this LDO will be on at all times and can be used to supply up to 20mA.

The LTC4160/LTC4160-1 also feature an overvoltage protection circuit which is designed to work with an external N-channel MOSFET to prevent damage to their inputs caused by accidental application of high voltage.

Finally, to prevent battery drain when a device is connected to a suspended USB port, an LDO from  $V_{BUS}$  to  $V_{OUT}$  provides low power USB suspend current to the end product application.

### Bidirectional PowerPath Switching Regulator – Step-Down Mode

The power delivered from  $V_{BUS}$  to  $V_{OUT}$  is controlled by a 2.25MHz constant frequency bidirectional switching regulator in step-down mode.  $V_{OUT}$  drives the combination of the external load and the battery charger. To meet the maximum USB load specification, the switching regulator contains a measurement and control system that ensures that the average input current remains below the level programmed at CLPROG.

If the combined load does not cause the switching regulator to reach the programmed input current limit,  $V_{OUT}$  will track approximately 0.3V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power flow in step-down mode.

If the combined external load plus battery charge current is large enough to cause the switching regulator to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB current, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at  $V_{OUT}$  exceeds the programmed power from  $V_{BUS}$ , load current will be drawn from the battery via the ideal diode(s) even when the battery charger is enabled.

The current out of CLPROG is a precise fraction of the  $V_{BUS}$  current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches

## OPERATION

the programmed limit, CLPROG reaches 1.18V and power delivered by the switching regulator is held constant.

The input current limit is programmed by the  $I_{LIM0}$  and  $I_{LIM1}$  pins. The input current limit has four possible settings ranging from the USB suspend limit of 500 $\mu$ A up to 1A for wall adapter applications. Two of these settings are specifically intended for use in the 100mA and 500mA USB application. Refer to Table 1 for current limit settings using  $I_{LIM0}$  and  $I_{LIM1}$ .

**Table 1. USB Current Limit Settings Using  $I_{LIM0}$  and  $I_{LIM1}$**

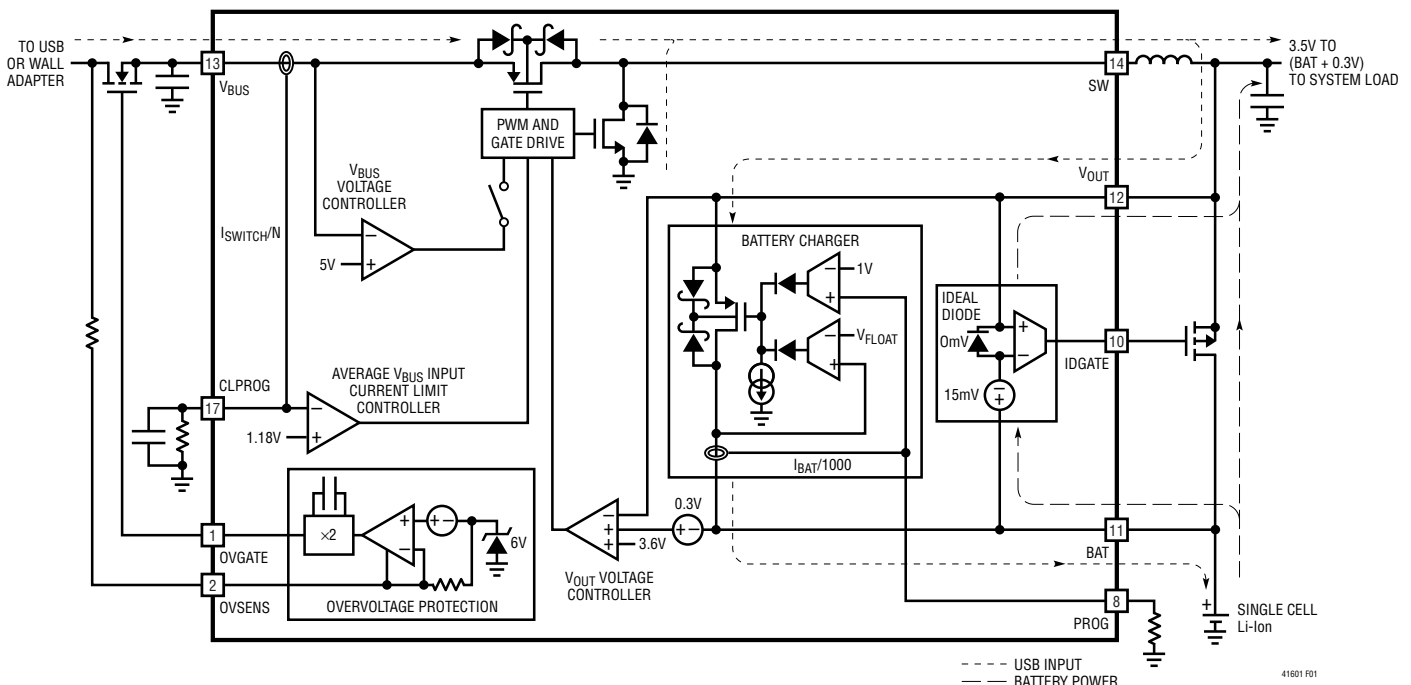
$I_{LIM1}$	$I_{LIM0}$	USB SETTING
0	0	1x Mode (USB 100mA Limit)
0	1	10x Mode (Wall 1A Limit)
1	0	Low Power Suspend (USB 500 $\mu$ A Limit)
1	1	5x Mode (USB 500mA Limit)

When the switching regulator is activated, the average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \cdot (h_{CLPROG} + 1)$$

where  $I_{VBUSQ}$  is the quiescent current of the LTC4160/LTC4160-1,  $V_{CLPROG}$  is the CLPROG servo voltage in current limit,  $R_{CLPROG}$  is the value of the programming resistor and  $h_{CLPROG}$  is the ratio of the measured current at  $V_{BUS}$  to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of  $h_{CLPROG}$ ,  $V_{CLPROG}$  and  $I_{VBUSQ}$ . Given worst-case circuit tolerances, the USB specification for the average input current in 100mA or 500mA mode will not be violated, provided that  $R_{CLPROG}$  is 3.01k or greater.

While not in current limit, the switching regulator's Bat-Track feature will set  $V_{OUT}$  to approximately 300mV above the voltage at BAT. However, if the voltage at BAT is below 3.3V, and the load requirement does not cause the switching regulator to exceed its current limit,  $V_{OUT}$  will regulate at a fixed 3.6V, as shown in Figure 2. This instant-on operation will allow a portable product to run immediately when power is applied without waiting for the battery to charge. If the load does exceed the current limit at  $V_{BUS}$ ,  $V_{OUT}$  will range between the no-load voltage and slightly below the battery voltage, indicated by the shaded region of Figure 2.



**Figure 1. Power Path Block Diagram – Power Available from USB/Wall Adapter**

## OPERATION

For very low-battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull  $V_{OUT}$  below the 3.6V instant-on voltage. To prevent  $V_{OUT}$  from falling below this level, an undervoltage circuit automatically detects that  $V_{OUT}$  is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized while allowing as much battery charge current as possible. See Over Programming the Battery Charger in the Applications Information section.

The voltage regulation loop compensation is controlled by the capacitance on  $V_{OUT}$ . A multilayer ceramic capacitor of 10 $\mu$ F is required for loop stability. Additional capacitance beyond this value will improve transient response.

An internal undervoltage lockout circuit monitors  $V_{BUS}$  and keeps the switching regulator off until  $V_{BUS}$  rises above 4.30V and is about 200mV above the battery voltage. When both conditions are met,  $\overline{VBUSGD}$  goes low and the switching regulator turns on. Hysteresis on the UVLO forces  $\overline{VBUSGD}$  high and turns off the switching regulator if  $V_{BUS}$  falls below 4.00V or to within 50mV of the battery voltage. When this happens, system power at  $V_{OUT}$  will be drawn from the battery via the ideal diode(s).

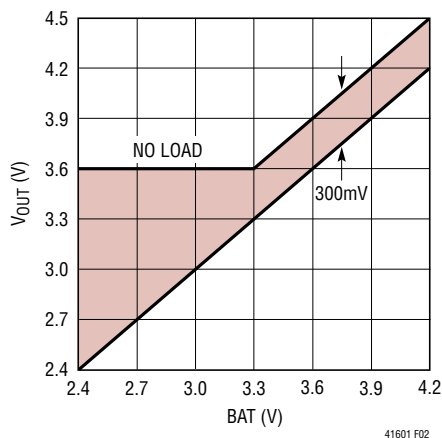


Figure 2.  $V_{OUT}$  vs BAT

### Bidirectional PowerPath Switching Regulator – Step-Up Mode

For USB On-The-Go applications, the bidirectional PowerPath switching regulator acts as a step-up converter to deliver power from  $V_{OUT}$  to  $V_{BUS}$ . The power from  $V_{OUT}$

comes from the battery via the ideal diode(s). As a step-up converter, the bidirectional switching regulator produces 5V on  $V_{BUS}$  and is capable of delivering at least 500mA. USB On-The-Go can be enabled by either of the external control pins, ENOTG or ID. Figure 3 shows the power flow in step-up mode.

An undervoltage lockout circuit monitors  $V_{OUT}$  and prevents step-up conversion until  $V_{OUT}$  rises above 2.8V. To prevent backdriving of  $V_{BUS}$  when input power is available, the  $V_{BUS}$  undervoltage lockout circuit prevents step-up conversion if  $V_{BUS}$  is already greater than 4.3V at the time step-up mode is enabled. The switching regulator is also designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS switch. This allows  $V_{BUS}$  to go to zero volts during a short-circuit condition or while shutdown, drawing zero current from  $V_{OUT}$ .

The voltage regulation loop is compensated by the capacitance on  $V_{BUS}$ . A 4.7 $\mu$ F multilayer ceramic capacitor is required for loop stability. Additional capacitance beyond this value will improve transient response. The  $V_{BUS}$  voltage has approximately 3% load regulation up to an output current of 500mA. At light loads, the switching regulator goes into Burst Mode<sup>®</sup> operation. The regulator will deliver power to  $V_{BUS}$  until it reaches 5.1V after which the NMOS and PMOS switches shut off. The regulator delivers power again to  $V_{BUS}$  once it falls below 5.1V.

The switching regulator features both peak inductor and average output current limit. The peak current-mode architecture limits peak inductor current on a cycle-by-cycle basis. The peak current limit is equal to  $V_{BUS}/2\Omega$  to a maximum of 1.8A so that in the event of a sudden short circuit, the current limit will fold back to a lower value. In step-up mode, the voltage on CLPROG represents the average output current of the switching regulator when a programming resistor and an averaging capacitor are connected from CLPROG to GND. With a 3.01k resistor on CLPROG, the bidirectional switching regulator has an output current limit of 680mA. As the output current approaches this limit, CLPROG servos to 1.15V and  $V_{BUS}$  falls rapidly to  $V_{OUT}$ . When  $V_{BUS}$  is close to  $V_{OUT}$  there may not be sufficient negative slope on the inductor current when the PMOS switch is on to balance the rise in the inductor

## OPERATION

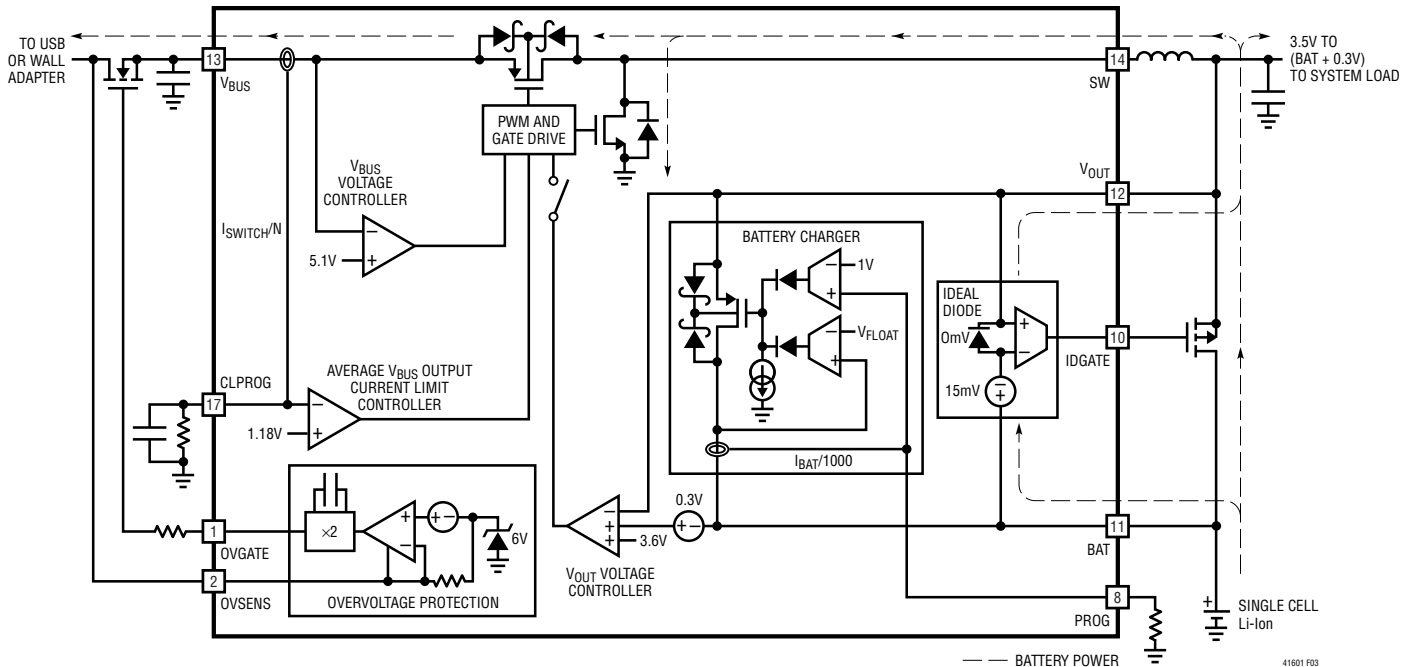


Figure 3. PowerPath Block Diagram – USB On-The-Go

current when the NMOS switch is on. This will cause the inductor current to run away and the voltage on CLPROG to rise. When CLPROG reaches 1.2V the switching of the synchronous PMOS is terminated and  $V_{OUT}$  is applied statically to its gate. This ensures that the inductor current will have sufficient negative slope during the time current is flowing out of the  $V_{BUS}$  pin. The PMOS will resume switching when CLPROG drops down to 1.15V.

The PMOS switch is enabled when  $V_{BUS}$  rises above  $V_{OUT} + 180\text{mV}$  and is disabled when it falls below  $V_{OUT} + 70\text{mV}$  to prevent the inductor current from running away when not in current limit. If the PMOS switch is disabled for more than 7.2ms then the switcher will shut off, the  $\overline{\text{FAULT}}$  pin will go low and a short circuit fault will be declared. To re-enable step-up mode, the  $\overline{\text{ENOTG}}$  pin, with ID high, must be cycled low and then high or the ID pin, with ENOTG grounded, must be cycled high and then low.

### Ideal Diode(s) from BAT to $V_{OUT}$

The LTC4160/LTC4160-1 each have an internal ideal diode as well as a controller for an external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever  $V_{OUT}$  drops below BAT.

If the load current increases beyond the power allowed from the bidirectional switching regulator, additional power will be pulled from the battery via the ideal diode(s). Furthermore, if power to  $V_{BUS}$  (USB or wall adapter) is removed, then all of the application power will be provided by the battery via the ideal diode(s). The ideal diode(s) will prevent  $V_{OUT}$  from drooping with only the storage capacitance required for the bidirectional switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip P-channel MOSFET whenever

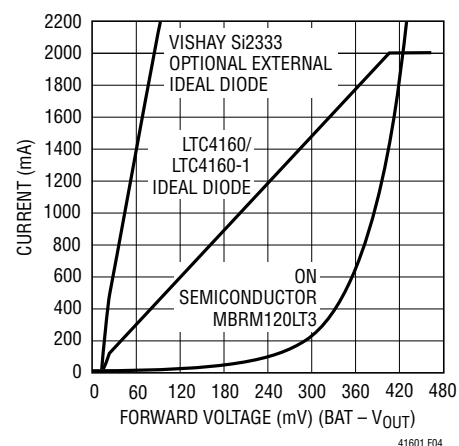


Figure 4. Ideal Diode V-I Characteristics



## OPERATION

the voltage at  $V_{OUT}$  is approximately 15mV ( $V_{FWD}$ ) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction.

To supplement the internal ideal diode, an external P-channel MOSFET may be added from BAT to  $V_{OUT}$ . The IDGATE pin of the LTC4160/LTC4160-1 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to  $V_{OUT}$  and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET having an on-resistance of 30m $\Omega$  or lower.

### Suspend LDO

If the LTC4160/LTC4160-1 is configured for USB suspend mode, the bidirectional switching regulator is disabled and the suspend LDO provides power to the  $V_{OUT}$  pin (presuming there is power available at  $V_{BUS}$ ). This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the bidirectional switching regulator is disabled (suspended). The suspend LDO sends a scaled copy of the  $V_{BUS}$  current to the CLPROG pin, which will servo to approximately 100mV in this mode. In accordance with the USB specification, the input to the LDO is current limited so that it will not exceed the low power suspend specification. If the load on  $V_{OUT}$  exceeds the suspend current limit, the additional current will come from the battery via the ideal diode(s).

### 3.3V Always-On LDO Supply

The LTC4160/LTC4160-1 include a low quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller, standby microcontroller or real time clock. Designed to deliver up to 20mA, the always-on LDO requires at least a 1 $\mu$ F multilayer ceramic bypass capacitor for compensation. The LDO is powered from  $V_{OUT}$ , and therefore will enter dropout at loads less than 20mA as  $V_{OUT}$  falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to  $V_{OUT}$ .

### Battery Charger

The LTC4160/LTC4160-1 include a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection, and thermistor sensor input for out-of-temperature charge pausing. The charger can be disabled using the ENCHARGER pin.

### Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below  $V_{TRKL}$ , typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than a 1/2 hour, the battery charger automatically terminates and indicates via the  $\overline{CHRG}$  and  $\overline{FAULT}$  pins that the battery was unresponsive.

Once the battery voltage is above 2.85V, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach  $1030/R_{PROG}$ . Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. Likewise, the USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

### Charge Termination

The battery charger has a built-in safety timer. When the voltage on the battery reaches the pre-programmed float voltage, the battery charger will regulate the battery voltage and the charge current will decrease naturally. Once the battery charger detects that the battery has reached the float voltage, the four hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

### Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough,

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## OPERATION

the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below the recharge threshold which is typically 100mV less than the charger's float voltage. In the event that the safety timer is running when the battery voltage falls below the recharge threshold, it will reset back to zero. To prevent brief excursions below the recharge threshold from resetting the safety timer, the battery voltage must be below the recharge threshold for more than 1ms. The charge cycle and safety timer will also restart if the  $V_{BUS}$  UVLO cycles low and then high (e.g.,  $V_{BUS}$  is removed and then replaced), or if the battery charger is cycled on and off by the  $\overline{ENCHARGER}$  pin.

### Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1030th of the battery charge current is sent to PROG, which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1030 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equation:

$$I_{CHG} = \frac{V_{PROG}}{R_{PROG}} \cdot 1030$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \cdot 1030$$

In many cases, the actual battery charge current,  $I_{BAT}$ , will be lower than  $I_{CHG}$  due to limited input power available and prioritization with the system load drawn from  $V_{OUT}$ .

The Battery Charger Flow Chart on the next page illustrates the battery charger's algorithm.

### Charge Status Indication

The  $\overline{CHRG}$  and  $\overline{FAULT}$  pins can be used to indicate the status of the battery charger. Two possible states are represented by  $\overline{CHRG}$ : charging and not charging. An open-drain output, the  $\overline{CHRG}$  pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

When charging begins,  $\overline{CHRG}$  is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the BAT pin reaches the float and the charge current has dropped to one tenth of the programmed value, the  $\overline{CHRG}$  pin goes high. The  $\overline{CHRG}$  pin does not respond to the C/10 threshold if the LTC4160/LTC4160-1 is in  $V_{BUS}$  input current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger.

Table 2 illustrates the possible states of the  $\overline{CHRG}$  and  $\overline{FAULT}$  pins when the battery charger is active.

**Table 2. Charge Status Readings Using the  $\overline{CHRG}$  and  $\overline{FAULT}$  Pins**

STATUS	$\overline{CHRG}$	$\overline{FAULT}$
Charging/NTC Fault	Low	High
Not Charging	High	High
Bad Battery	High	Low

An NTC fault pauses charging while the battery temperature is out of range but is not indicated using the  $\overline{CHRG}$  or  $\overline{FAULT}$  pins.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour) the  $\overline{CHRG}$  pin goes high and the  $\overline{FAULT}$  pin goes low to indicate a bad battery fault.

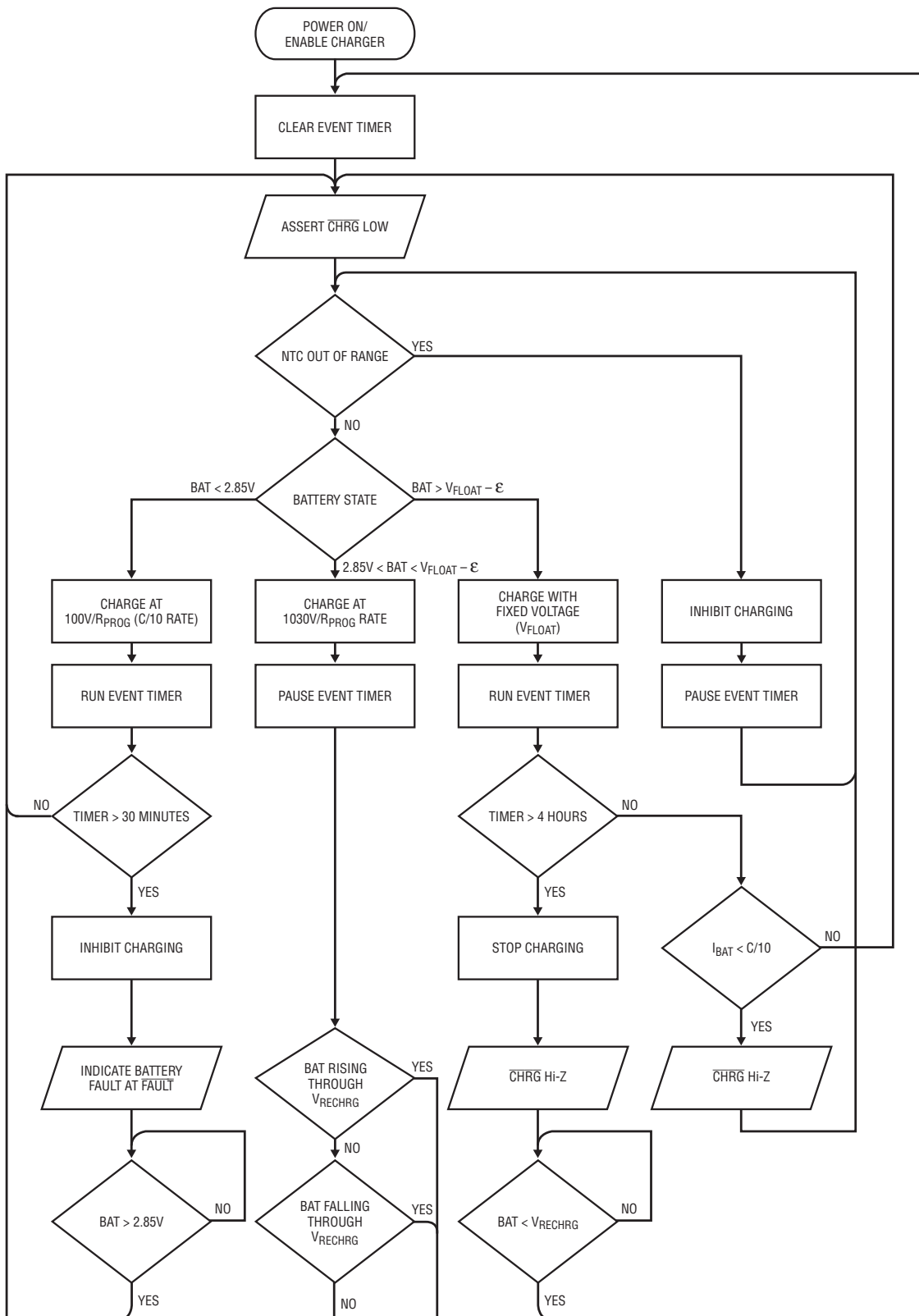
Note that the LTC4160/LTC4160-1 are 3-terminal PowerPath products where system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the trickle charge threshold voltage within the bad battery timeout period. In this case, the battery charger will falsely indicate a bad battery. System software may then reduce the load and reset the battery charger to try again.

The  $\overline{FAULT}$  pin is also used to indicate whether there is a short circuit condition on  $V_{BUS}$  when the bidirectional

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**Battery Charger Flow Chart**



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switching regulator is in On-The-Go mode. When a short circuit condition is detected,  $\overline{\text{FAULT}}$  will go low-Z. The ENOTG or  $\overline{\text{VBUSGD}}$  pins can be used to determine which fault has occurred. If ENOTG or  $\overline{\text{VBUSGD}}$  is low when  $\overline{\text{FAULT}}$  went low, then a bad battery fault has occurred. If either pin is high, then a short circuit on  $V_{\text{BUS}}$  has occurred.

### NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack.

To use this feature connect the NTC thermistor,  $R_{\text{NTC}}$ , between the NTC pin and ground and a bias resistor,  $R_{\text{NOM}}$ , from NTCBIAS to NTC.  $R_{\text{NOM}}$  should be a 1% 200ppm resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25).

The LTC4160/LTC4160-1 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k for a 100k thermistor. For a Vishay Curve 1 thermistor, this corresponds to approximately 40°C. If the battery charger is in constant-voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4160/LTC4160-1 are also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay Curve 1 100k thermistor, this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

### Thermal Regulation

To prevent thermal damage to the LTC4160/LTC4160-1 or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to 105°C. This thermal regulation technique protects the LTC4160/LTC4160-1 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with

a given circuit board design. The benefit of the LTC4160/LTC4160-1 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

### Overvoltage Protection

The LTC4160/LTC4160-1 can protect themselves from the inadvertent application of excessive voltage to  $V_{\text{BUS}}$  with just two external components: an N-channel MOSFET and a 6.2k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external MOSFET and its associated drain breakdown voltage.

The overvoltage protection circuit consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of the external MOSFET. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately  $1.88 \cdot \text{OVSENS}$ . This will enhance the N-channel MOSFET and provide a low impedance connection to  $V_{\text{BUS}}$  which will, in turn, power the LTC4160/LTC4160-1. If OVSENS should rise above 6V due to a fault or the use of an incorrect wall adapter, OVGATE will be pulled to GND. This disables the external MOSFET and protects downstream circuitry. When the voltage drops below 6V again, the external MOSFET will be re-enabled.

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin as it may adversely affect operation.

See the Applications Information section for resistor power dissipation rating calculations, a table of recommended components, and reverse-voltage protection.

### Shutdown Mode

The USB switching regulator is enabled whenever  $V_{\text{BUS}}$  is above  $V_{\text{UVLO}}$  and the LTC4160/LTC4160-1 are not in USB suspend mode.

The ideal diode(s) are enabled at all times and cannot be disabled.

## APPLICATIONS INFORMATION

### Bidirectional PowerPath Switching Regulator CLPROG Resistor and Capacitor Selection

As described in the Bidirectional PowerPath Switching Regulator – Step-Down Mode section, the resistor on the CLPROG pin determines the average  $V_{BUS}$  input current limit. In step-down mode the switching regulator's  $V_{BUS}$  input current limit can be set to either the 1x mode (USB 100mA), the 5x mode (USB 500mA) or the 10x mode. The  $V_{BUS}$  input current will be comprised of two components, the current that is used to drive  $V_{OUT}$  and the quiescent current of the switching regulator. To ensure that the total average input current remains below the USB specification, both components of input current should be considered. The Electrical Characteristics table gives the typical values for quiescent currents in all settings as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a precision resistor should be used. Recall that:

$$I_{V_{BUS}} = I_{V_{BUS}Q} + V_{CLPROG}/R_{CLPPROG} \cdot (h_{CLPROG} + 1).$$

An averaging capacitor is required in parallel with the resistor so that the switching regulator can determine the average input current. This capacitor also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.1 $\mu$ F or larger.

### Bidirectional PowerPath Switching Regulator Inductor Selection

Because the  $V_{BUS}$  voltage range and  $V_{OUT}$  voltage range of the PowerPath switching regulator are both fairly narrow, the LTC4160/LTC4160-1 were designed for a specific inductance value of 3.3 $\mu$ H. Some inductors which may be suitable for this application are listed in Table 3.

**Table 3. Recommended PowerPath Inductors for the LTC4160/LTC4160-1**

INDUCTOR TYPE	L ( $\mu$ H)	MAX IDC (A)	MAX DCR ( $\Omega$ )	SIZE IN mm (L x W x H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 x 3.9 x 1.7	Coilcraft www.coilcraft.com
D53LC	3.3	2.26	0.034	5 x 5 x 3	Toko www.toko.com
DB318C	3.3	1.55	0.070	3.8 x 3.8 x 1.8	
WE-TPC Type M1	3.3	1.95	0.065	4.8 x 4.8 x 1.8	Wurth Elektronik www.we-online.com
CDRH6D12	3.3	2.2	0.063	6.7 x 6.7 x 1.5	Sumida
CDRH6D38	3.3	3.5	0.020	7 x 7 x 4	www.sumida.com

### Bidirectional PowerPath Switching Regulator $V_{BUS}$ and $V_{OUT}$ Bypass Capacitor Selection

The type and value of capacitors used with the LTC4160/LTC4160-1 determine several important parameters such as regulator control-loop stability and input voltage ripple. Because the LTC4160/LTC4160-1 use a bidirectional switching regulator between  $V_{BUS}$  and  $V_{OUT}$ , the  $V_{BUS}$  current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor (MLCC) be used to bypass  $V_{BUS}$ . Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on  $V_{BUS}$  directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple.

The inrush current limit specification for USB devices is calculated in terms of the total number of Coulombs needed to charge the  $V_{BUS}$  bypass capacitor to 5V. The maximum inrush charge for USB On-The-Go devices is 33 $\mu$ C. This places a limit of 6.5 $\mu$ F of capacitance on  $V_{BUS}$  assuming a linear capacitor. However, most ceramic capacitors have a capacitance that varies with bias voltage. The average capacitance needs to be less than 6.5 $\mu$ F over a 0V to 5V bias voltage range to meet the inrush current-limit specification. A 10 $\mu$ F capacitor in a 0805 package, such as the Murata GRM21BR71A106KE51L would be a suitable  $V_{BUS}$  bypass capacitor. If more capacitance is required for better noise performance and stability, it should be connected directly to the  $V_{BUS}$  pin when using the overvoltage protection circuit. This extra capacitance will be soft-connected over a couple of milliseconds to limit inrush current and avoid excessive transient voltage drops on  $V_{BUS}$ .

To prevent large  $V_{OUT}$  voltage steps during transient load conditions, it is also recommended that an MLCC be used to bypass  $V_{OUT}$ . The output capacitor is used in the compensation of the switching regulator. At least 10 $\mu$ F with low ESR are required on  $V_{OUT}$ . Additional capacitance will improve load transient performance and stability.

MLCCs typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

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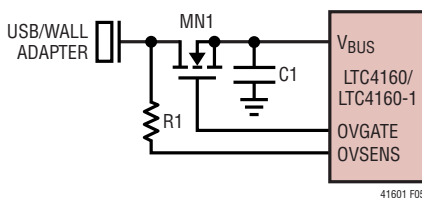
There are MLCCs available with several types of dielectrics each having considerably different characteristics. For example, X7R MLCCs have the best voltage and temperature stability. X5R MLCCs have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V MLCCs have the highest packing density, but must be used with caution, because of their extreme nonlinear characteristic of capacitance versus voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias as is expected in-circuit. Many vendors specify the capacitance versus voltage with a  $1V_{RMS}$  AC test signal and, as a result, over state the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

### Overvoltage Protection

$V_{BUS}$  can be protected from overvoltage damage with two additional components, a resistor R1 and an N-channel MOSFET MN1, as shown in Figure 5. Suitable choices for MN1 are listed in Table 4.

**Table 4. Recommended N-Channel MOSFETs for the Overvoltage Protection Circuit**

PART #	BVDSS	R <sub>ON</sub>	PACKAGE
Si1472DH	30V	57mΩ	SC70-6
Si2302ADS	20V	60mΩ	SOT-23
Si2306BDS	30V	47mΩ	SOT-23
Si2316DS	30V	50mΩ	SOT-23
IRLML2502	20V	50mΩ	SOT-23
FDN372S	30V	50mΩ	SOT-23
NTLJS4114N	30V	35mΩ	WDFN6

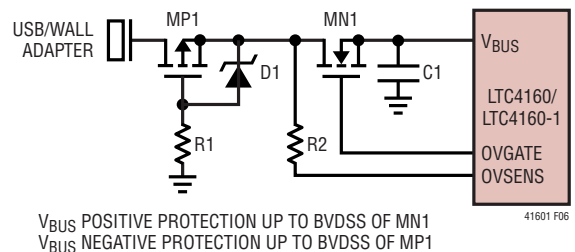


**Figure 5. Overvoltage Protection**

R1 is a 6.2k resistor and must be rated for the power dissipated during maximum overvoltage. In an overvoltage condition the OVSENS pin will be clamped at 6V. R1 must be sized appropriately to dissipate the resultant power. For example, a 1/10W 6.2k resistor can have at most  $\sqrt{(P_{MAX} \cdot 6.2k\Omega)} = 25V$  applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 31V. A 1/4W 6.2k resistor raises this value to 45V. OVSENS's absolute maximum current rating of 10mA imposes an upper limit of 68V protection.

### Reverse Voltage Protection

The LTC4160/LTC4160-1 can also be easily protected against the application of reverse voltages, as shown in Figure 6. D1 and R1 are necessary to limit the maximum  $V_{GS}$  seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BVGS. The circuit shown in Figure 6 offers forward voltage protection up to MN1's BVDSS and reverse voltage protection up to MP1's BVDSS.



**Figure 6. Dual Polarity Voltage Protection**

### Battery Charger Over Programming

The USB high power specification allows for up to 2.5W to be drawn from the USB port. The LTC4160/LTC4160-1's bidirectional switching regulator in step-down mode converts the voltage at  $V_{BUS}$  to a voltage just above BAT on  $V_{OUT}$ , while limiting power to less than the amount programmed at CLPROG. The charger should be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, the charge current will be reduced until the system load on  $V_{OUT}$  is satisfied and the  $V_{BUS}$  current limit is satisfied. Programming the charger for more

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current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal dissipation within the charger.

### Battery Charger Stability Considerations

The LTC4160/LTC4160-1's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1 $\mu$ F from BAT to GND.

High value, low ESR MLCCs reduce the constant-voltage loop phase margin, possibly resulting in instability. Up to 22 $\mu$ F may be used in parallel with a battery, but larger capacitors should be decoupled with 0.2 $\Omega$  to 1 $\Omega$  of series resistance.

Furthermore, a 100 $\mu$ F capacitor in series with a 0.3 $\Omega$  resistor from BAT to GND is required to prevent oscillation when the battery is disconnected.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance,  $C_{PROG}$ , the following equation should be used to calculate the maximum resistance value for  $R_{PROG}$ :

$$R_{PROG} \leq \frac{1}{2\pi \cdot 100\text{kHz} \cdot C_{PROG}}$$

### Alternate NTC Thermistors and Biasing

The LTC4160/LTC4160-1 provide temperature qualified charging if a grounded thermistor and a bias resistor

are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor ( $R_{25}$ ) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C respectively assuming a Vishay Curve 1 thermistor.

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay Curve 1 resistance-temperature characteristic.

In the explanation below, the following notation is used.

$R_{25}$  = Value of the thermistor at 25°C

$R_{NTC|COLD}$  = Value of the thermistor at the cold trip point

$R_{NTC|HOT}$  = Value of the thermistor at the hot trip point

$r_{COLD}$  = Ratio of  $R_{NTC|COLD}$  to  $R_{25}$

$r_{HOT}$  = Ratio of  $R_{NTC|HOT}$  to  $R_{25}$

$R_{NOM}$  – Primary thermistor bias resistor (see Figure 7)

$R_1$  = Optional temperature range adjustment resistor (see Figure 8)

The trip points for the LTC4160/LTC4160-1's temperature qualification are internally programmed at  $0.349 \cdot NTCBIAS$  for the hot threshold and  $0.765 \cdot NTCBIAS$  for the cold threshold.

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Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM} + R_{NTC|HOT}} \cdot NTCBIAS = 0.349 \cdot NTCBIAS$$

And the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \cdot NTCBIAS = 0.765 \cdot NTCBIAS$$

Solving these equations for  $R_{NTC|COLD}$  and  $R_{NTC|HOT}$  results in the following:

$$R_{NTC|HOT} = 0.536 \cdot R_{NOM}$$

and

$$R_{NTC|COLD} = 3.25 \cdot R_{NOM}$$

By setting  $R_{NOM}$  equal to  $R25$ , the above equations result in  $r_{HOT} = 0.536$  and  $r_{COLD} = 3.25$ . Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor,  $R_{NOM}$ , different in value from  $R25$ , the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \cdot R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \cdot R25$$

where  $r_{HOT}$  and  $r_{COLD}$  are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics,  $r_{HOT}$  is 0.2488 at 60°C. Using the above equation,  $R_{NOM}$  should

be set to 46.4k. With this value of  $R_{NOM}$ ,  $r_{COLD}$  is 1.436 and the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in “temperature gain” of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor,  $R1$ , as shown in Figure 8. The following formulas can be used to compute the values of  $R_{NOM}$  and  $R1$ :

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \cdot R25$$

$$R1 = 0.536 \cdot R_{NOM} - r_{HOT} \cdot R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \cdot 100k = 104.2k$$

the nearest 1% value is 105k:

$$R1 = 0.536 \cdot 105k - 0.4368 \cdot 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 8 and results in an upper trip point of 45°C and a lower trip point of 0°C.

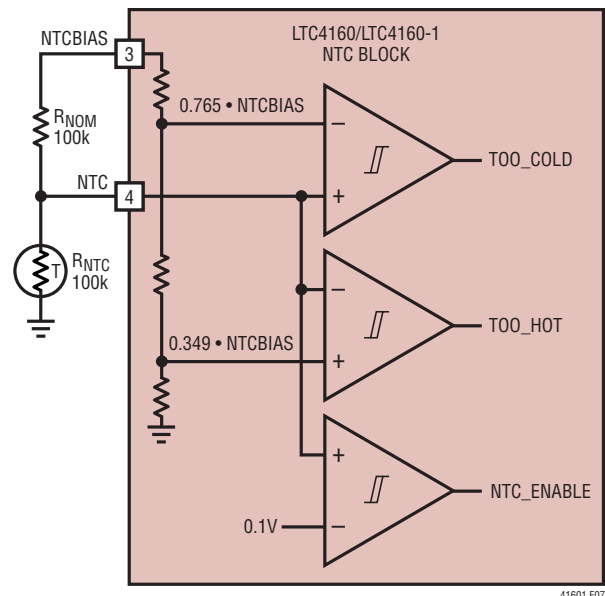


Figure 7. Standard NTC Configuration



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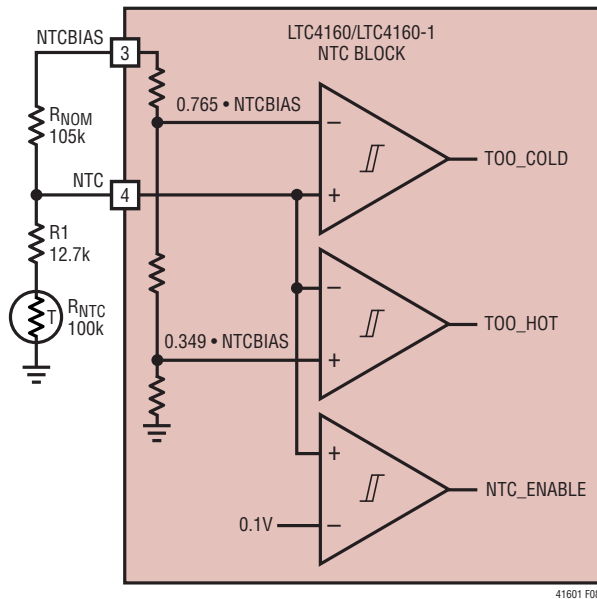


Figure 8. Modified NTC Configuration

## Hot Plugging and USB Inrush Current Limiting

The overvoltage protection circuit provides inrush current limiting due to the long time it takes for OVGATE to fully enhance the N-channel MOSFET. This prevents the current from building up in the cable too quickly and dampens out any resonant overshoot on  $V_{BUS}$ . It is possible to observe voltage overshoot on  $V_{BUS}$  when connecting the LTC4160/LTC4160-1 to a lab supply if the overvoltage protection circuit is not used. This overshoot is caused by the inductance of the long leads from the supply to  $V_{BUS}$ . Twisting the wires together from the supply to  $V_{BUS}$  can greatly reduce the parasitic inductance of these long leads and keep  $V_{BUS}$  at a safe level. USB cables are generally manufactured with the power leads in close proximity and thus have fairly low parasitic inductance.

## Hot Plugging and USB On-The-Go

If there is more than 4.3V on  $V_{BUS}$  when On-The-Go is enabled, the bidirectional switching regulator will not try to drive  $V_{BUS}$ . If USB On-The-Go is enabled and an external supply is then connected to  $V_{BUS}$ , one of three things will happen depending on the properties of the external supply. If the external supply has a regulation voltage higher than 5.1V, the bidirectional switching regulator will stop

switching and  $V_{BUS}$  will be held at the regulation voltage of the external supply. If the external supply has a lower regulation voltage and is capable of only sourcing current, then  $V_{BUS}$  will be regulated to 5.1V. The external supply will not source current to  $V_{BUS}$ .

For a supply that can also sink current and has a regulation voltage less than 5.1V, the bidirectional switching regulator will source current into the external supply in an attempt to bring  $V_{BUS}$  up to 5.1V. As long as the external supply holds  $V_{BUS}$  to more than  $V_{OUT} + 70\text{mV}$ , the bidirectional switching regulator will source up to 680mA into the supply. If  $V_{BUS}$  is held to a voltage that is less than  $V_{OUT} + 70\text{mV}$  then the short circuit timer will shut off the switching regulator after 7.2ms. The  $\overline{\text{FAULT}}$  pin will then go low to indicate a short circuit current fault.

 $V_{BUS}$  Bypass Capacitance and USB On-The-Go Session Request Protocol

When two On-The-Go devices are connected, one will be the A device and the other will be the B device depending on whether the device is connected to a micro-A or micro-B plug. The A device provides power to the B device and starts as the host. To prolong battery life, the A device can power down  $V_{BUS}$  when the BUS is not being used. If the A device has powered down  $V_{BUS}$ , the B device can request the A device to power up  $V_{BUS}$  and start a new session using the session request protocol (SRP). The SRP consists of data-line pulsing and  $V_{BUS}$  pulsing. The B device must first pulse the  $D^+$  or  $D^-$  data lines. The B device must then pulse  $V_{BUS}$  only if the A device does not respond to the data-line pulse. The A device is required to respond to only one of the pulsing methods. USB A devices that never power down  $V_{BUS}$  are not required to respond to the SRP.

For  $V_{BUS}$  pulsing, the limit on the  $V_{BUS}$  capacitance on the A device allows a B device to differentiate between a powered down On-The-Go device and a powered down standard host. The B device will send out a pulse of current that will raise  $V_{BUS}$  to a voltage between 2.1 and 5.25V if connected to an On-The-Go A device which must have no more than  $6.5\mu\text{F}$ . An On-The-Go A device must drive  $V_{BUS}$  as soon as the current pulse raises  $V_{BUS}$  above 2.1V if the device is capable of responding to  $V_{BUS}$  pulsing.

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This same current pulse must not raise  $V_{BUS}$  any higher than 2V when connected to a standard host which must have at least 96 $\mu$ F. The 96 $\mu$ F for a standard host represents the minimum capacitance with  $V_{BUS}$  between 4.75V and 5.25V. Since the SRP pulse must not drive  $V_{BUS}$  greater than 2V, the capacitance seen at these voltage levels can be greater than 96 $\mu$ F, especially if MLCCs are used. Therefore, the 96 $\mu$ F represents a lower bound on the standard host bypass capacitance for determining the amplitude and duration of the current pulse. More capacitance will only decrease the maximum level that  $V_{BUS}$  will rise to for a given current pulse.

Figure 9 shows an On-The-Go device using the LTC4160/LTC4160-1 acting as the A device. Additional capacitance can be placed on the  $V_{BUS}$  pin of the LTC4160/LTC4160-1 when using the overvoltage protection circuit. The B device may not be able to distinguish between a powered down LTC4160/LTC4160-1 with overvoltage protection and a powered down standard host because of this extra capacitance. In addition, if the SRP pulse raises  $V_{BUS}$  above its UVLO threshold of 4.3V the LTC4160/LTC4160-1 will assume input power is available and will not attempt to drive  $V_{BUS}$ . Therefore, it is recommended that an On-The-Go device using the LTC4160/LTC4160-1 respond to data-line pulsing.

When an On-The-Go device using the LTC4160/LTC4160-1 becomes the B device, as in Figure 10, it must send out a data line pulse followed by a  $V_{BUS}$  pulse to request a session from the A device. The On-The-Go device designer can choose how much capacitance will be placed on the  $V_{BUS}$  pin of the LTC4160/LTC4160-1 and then generate a  $V_{BUS}$  pulse that can distinguish between a powered

down On-The-Go A device and a powered down standard host. A suitable pulse can be generated because of the disparity in the bypass capacitances of an On-The-Go A device and a standard host even if there is somewhat more than 6.5 $\mu$ F capacitance connected to the  $V_{BUS}$  pin of the LTC4160/LTC4160-1.

### Board Layout Considerations

The Exposed Pad on the backside of the LTC4160/LTC4160-1 package must be securely soldered to the PC board ground. This is the primary ground pin in the package, and it serves as the return path for both the control circuitry and N-channel MOSFET switch.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor, inductor, and output capacitor be as close to the LTC4160/LTC4160-1 as possible and that there be an unbroken ground plane under the LTC4160/LTC4160-1 and all of its external high frequency components. High frequency current, such as the  $V_{BUS}$  current tends to find its way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 11). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

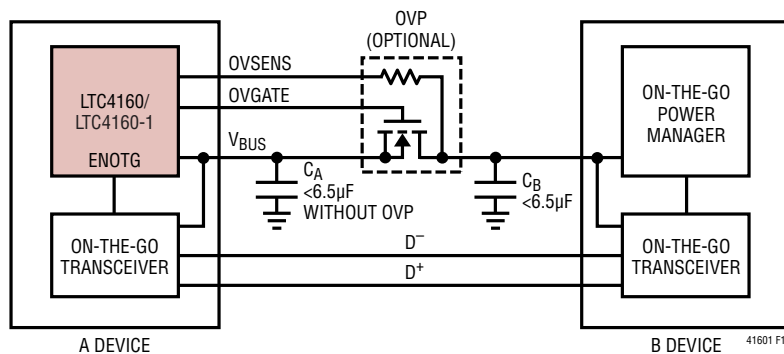


Figure 9. LTC4160/LTC4160-1 as the A Device

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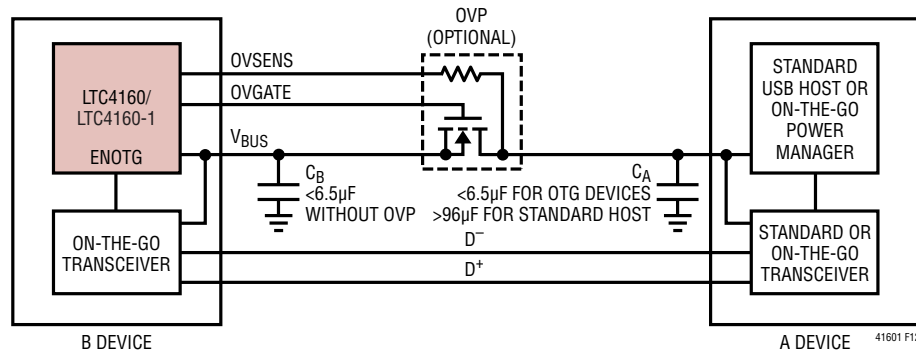


Figure 10. LTC4160/LTC4160-1 as the B Device

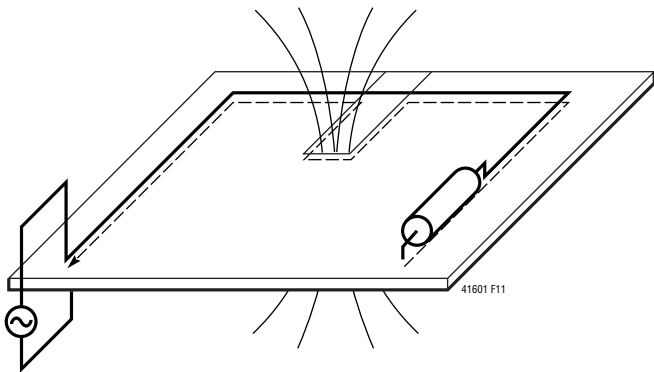


Figure 11. Higher Frequency Ground Current Follow Their Incident Path. Slices in the Ground Plane Create Large Loop Areas. The Large Loop Areas Increase the Inductance of the Path Leading to Higher System Noise.

The IDGATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional offset to the ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with  $V_{OUT}$  connected metal, which should generally be less than one volt higher than IDGATE.

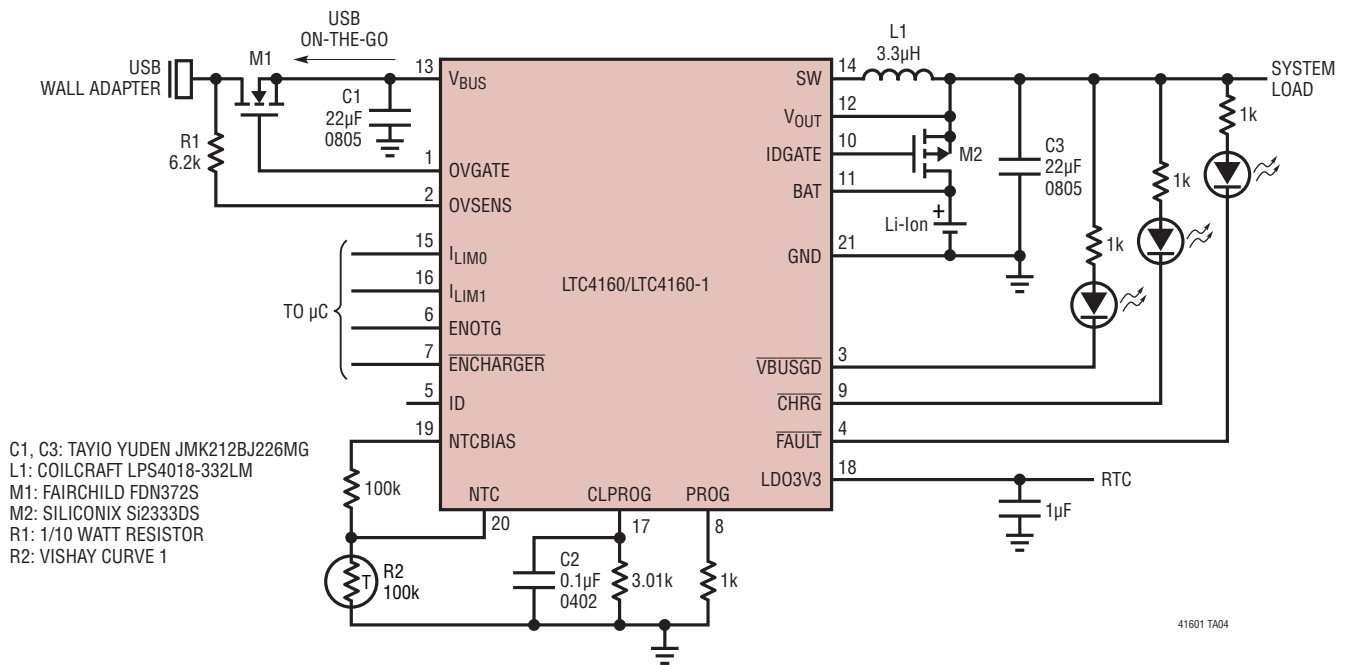
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC4160/LTC4160-1:

1. The Exposed Pad of the package (Pin 21) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The trace connecting  $V_{BUS}$  to its respective decoupling capacitor should be as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is critical to minimize inductance from these capacitors to the LTC4160/LTC4160-1.
3. Connections between the PowerPath switching regulator inductor and the output capacitor on  $V_{OUT}$  should be kept as short as possible. Use area fills whenever possible. The GND side of the output capacitors should connect directly to the thermal ground plane of the part.
4. The switching power trace connecting SW to its respective inductor should be minimized to reduce radiated EMI and parasitic coupling.

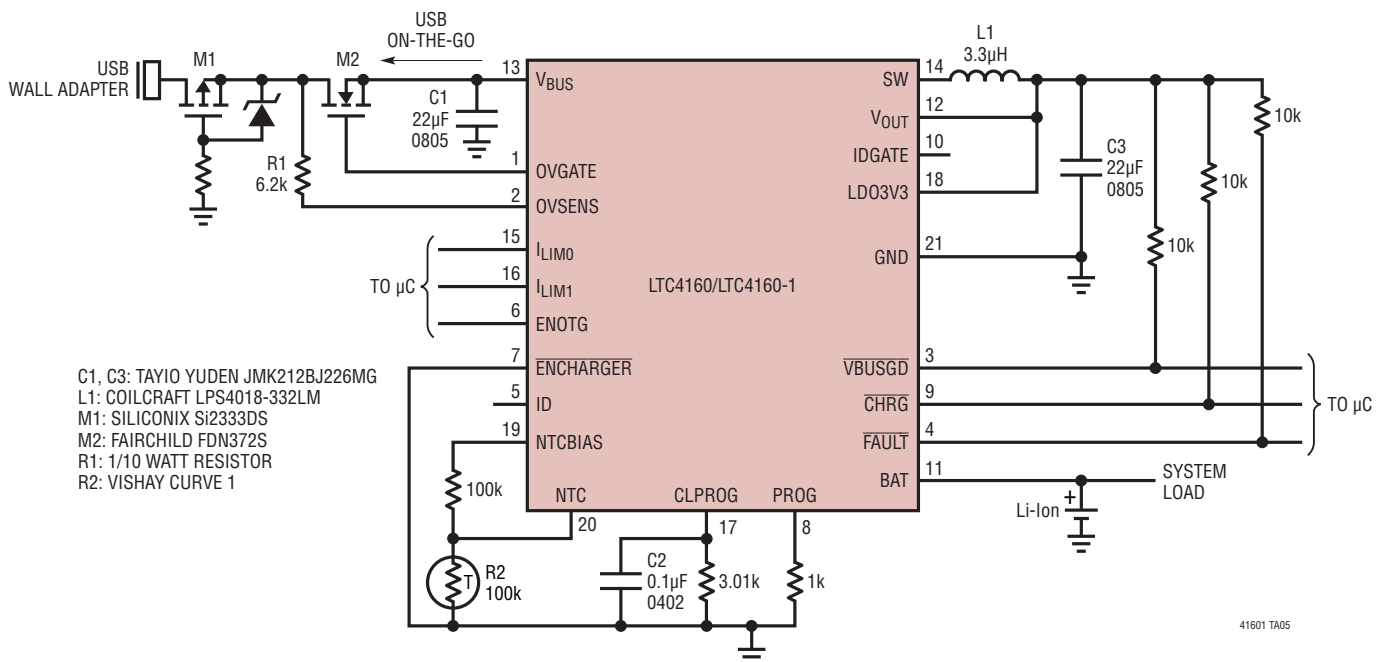


## TYPICAL APPLICATIONS

### High Efficiency Power Manager/Battery Charger with USB On-The-Go, Overvoltage Protection and Low Battery Start-Up



### High Efficiency Switching Battery Charger with USB On-The-Go, Overvoltage and Reverse-Voltage Protection





**REVISION HISTORY**

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/10	Removal of PDC package and inclusion of UDC package information in data sheet LTC4160EPDC and LTC4160EPDC-1 designated obsolete in Order Information section	1 to 32 2

