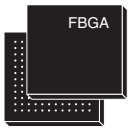
STM32TS60

Multi-touch screen controller device using a digital resistive touchpanel with I²C, SPI, UART and USB interfaces

Data brief

Features

- Patented digital resistive multi-touchpanel technology powered by Pmatrix™ firmware engine
- Able to track up to 10 independent touches simultaneously
- Finger, nail and any stylus touch capability
- Up to 0.17 mm resolution
- Touch actuation force information
- No calibration requirements
- Typical touchpanel scan rate of 125 Hz up to 250 Hz
- Single- or dual-chip architecture able to support up to 10.1” screens
- Single-chip controller able to support up to 129 rows/columns coming from the sensor matrix.
- Embedded compensation resistors for reduced BOM and easy connection to the touchpanel
- I²C, SPI, UART and USB communication interfaces
- Very low power mode allowing “wakeup on touch/release” mode
- Wakeup response time: 10 µs from Sleep mode and 100 µs from Standby mode



UFBGA144
(7 x 7 mm)

Applications

- Gaming devices
- Mobile handsets
- Smart phones
- Portable media players
- Personal navigation devices
- Mobile internet devices
- Netbooks

Table 1. STM32TS60 device summary

Feature	Description
Touchpanel size	2.5" to 6” (single-chip) / 6" to 10.1” (dual-chip)
Columns, rows	Up to 129 rows and columns with a maximum of 64 rows and 81 columns (see main architectures in *Section 3*)
Interface	I²C, SPI, UART and USB
Supply voltage range	2.4 to 3.6 V
Max. temperature range	-40 °C to +85 °C
Package	UFBGA 144 (7 x 7 mm, 0.5 pitch) ECOPACK® package

Contents

List of tables

List of figures

1 Description

1.1 Device overview

The STM32TS60 product is a multitouch controller device based on Stantum's patented digital resistive multitouch technology. This technology employs the connectivity power of the universal serial bus (USB) with Cortex™-M3 processors and ARM architecture.

Conventional resistive touch controllers are unable to detect more than one contact at a time. Thanks to the STM32TS60 device, it is possible to detect and track up to ten contacts over a touchpanel. The STM32TS60 delivers an exact image of what is happening on the touchpanel surface in the most reliable way with very fast response time and with high noise immunity performances.

The STM32TS60 represents a breakthrough over competing technologies, bringing outstanding multitouch performance with the best power budget.

The resistive technology does not require any panel scan during Standby. Consequently, the STM32TS60 device has very low standby power consumption. In addition, this device benefits from the industry-leading mW/MIPS power performance of the ARM Cortex-M3 core.

1.2 Main benefits

- Unique resistive true multitouch technology with up to 10 touches at a time
- Finger, nail and any stylus touch capability
- Fingers actuation force detection based on linear measurement of the touch area surface variation
- High responsiveness with low power consumption (at standby, near zero consumption)
- Homogeneous sensitivity on all points of the touchpanel area
- No calibration
- IP protected by solid patents based on proven resistive technology with very powerful EMI (electromagnetic insulation).
- Very low power Standby mode and zero power resistive panel
- Panel adapted from the proven high-volume resistive technology; able to reach high durability and 90 % transparency.

2 Ballout and pin description

Figure 1. STM32TS60 single-chip UFBGA144 ballout top view

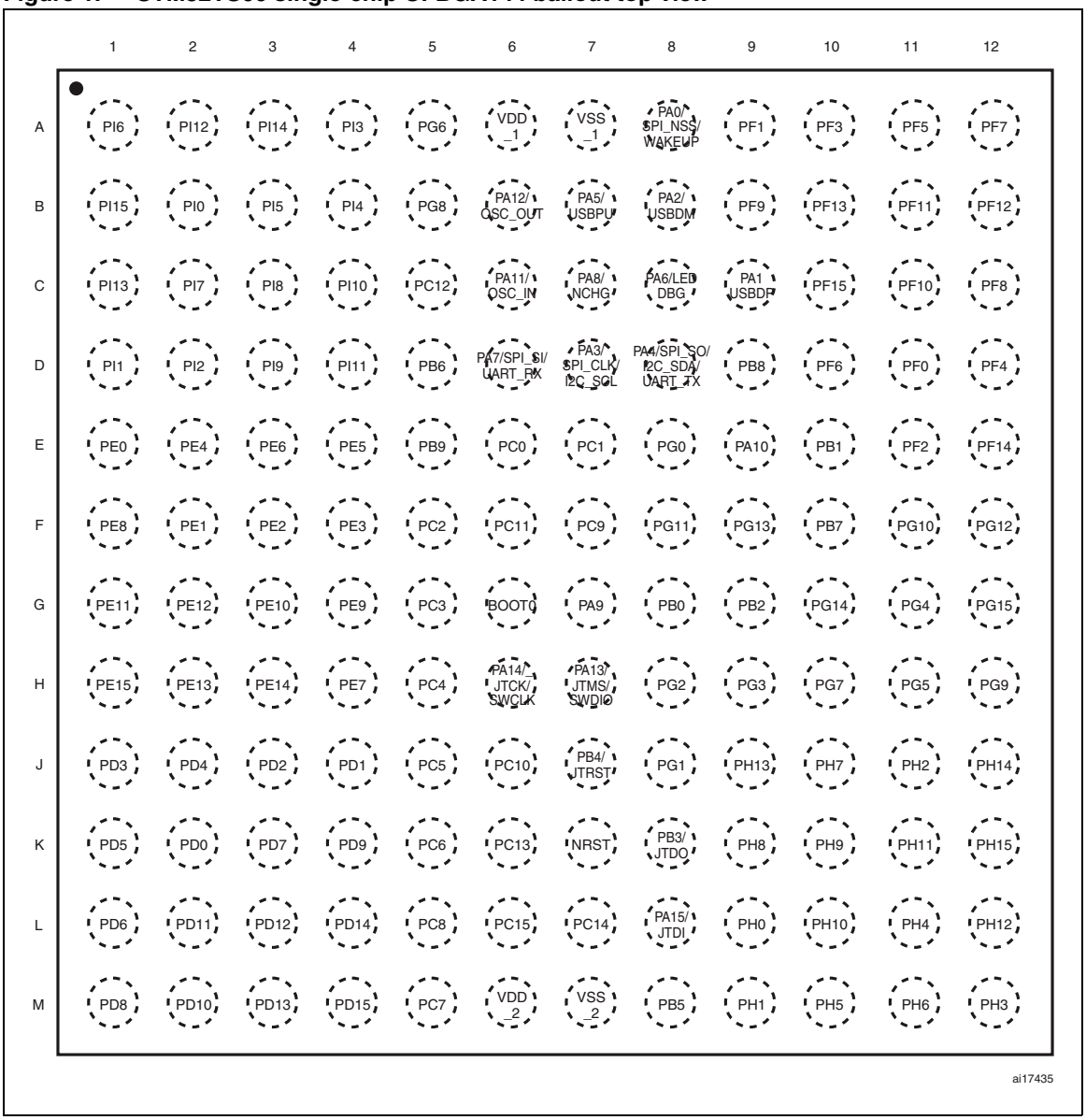


Figure 2. STM32TS60 dual-chip (master) UFBGA144 ballout top view

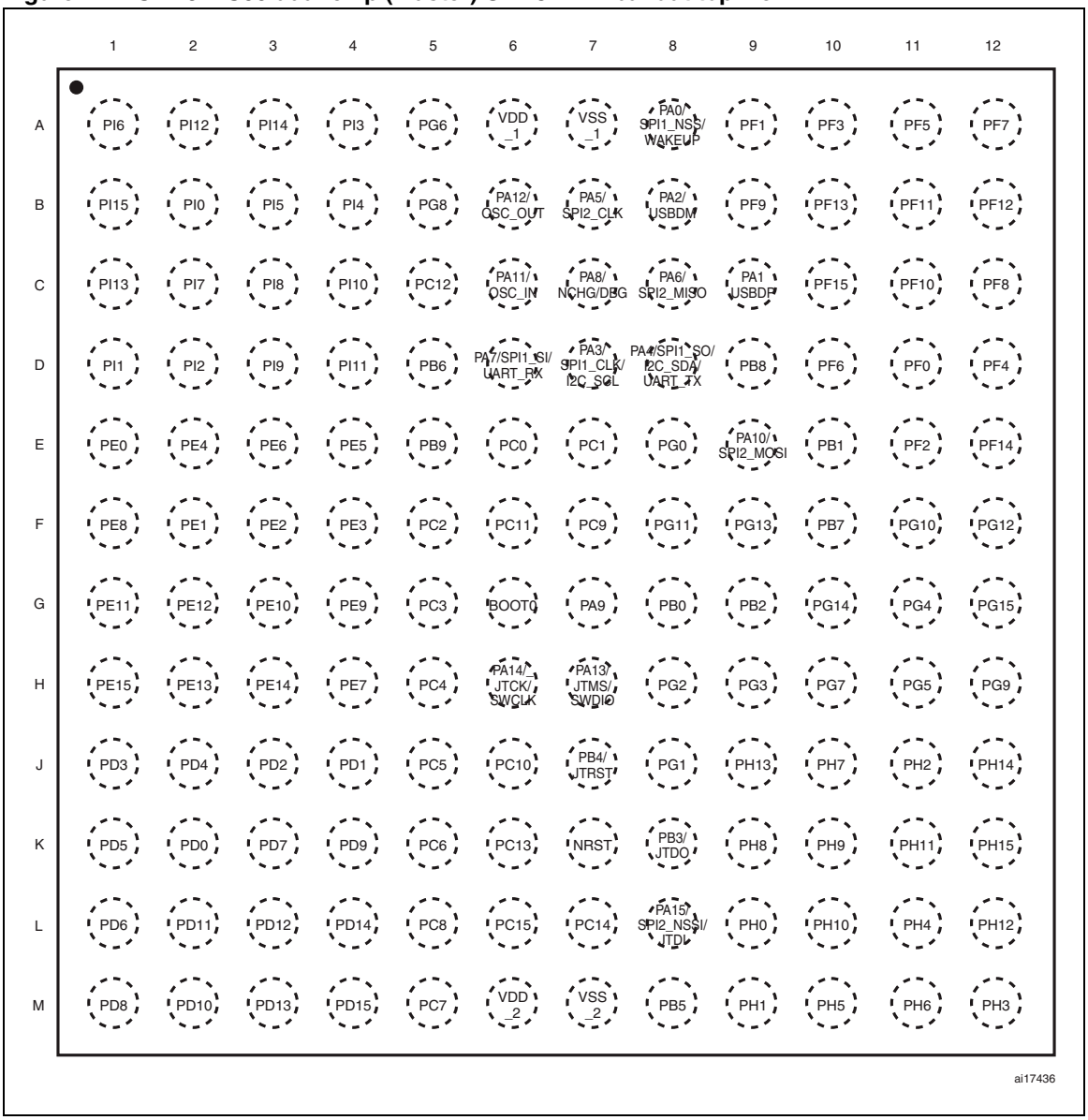


Figure 3. STM32TS60 dual-chip (slave) device UFBGA144 ballout top view

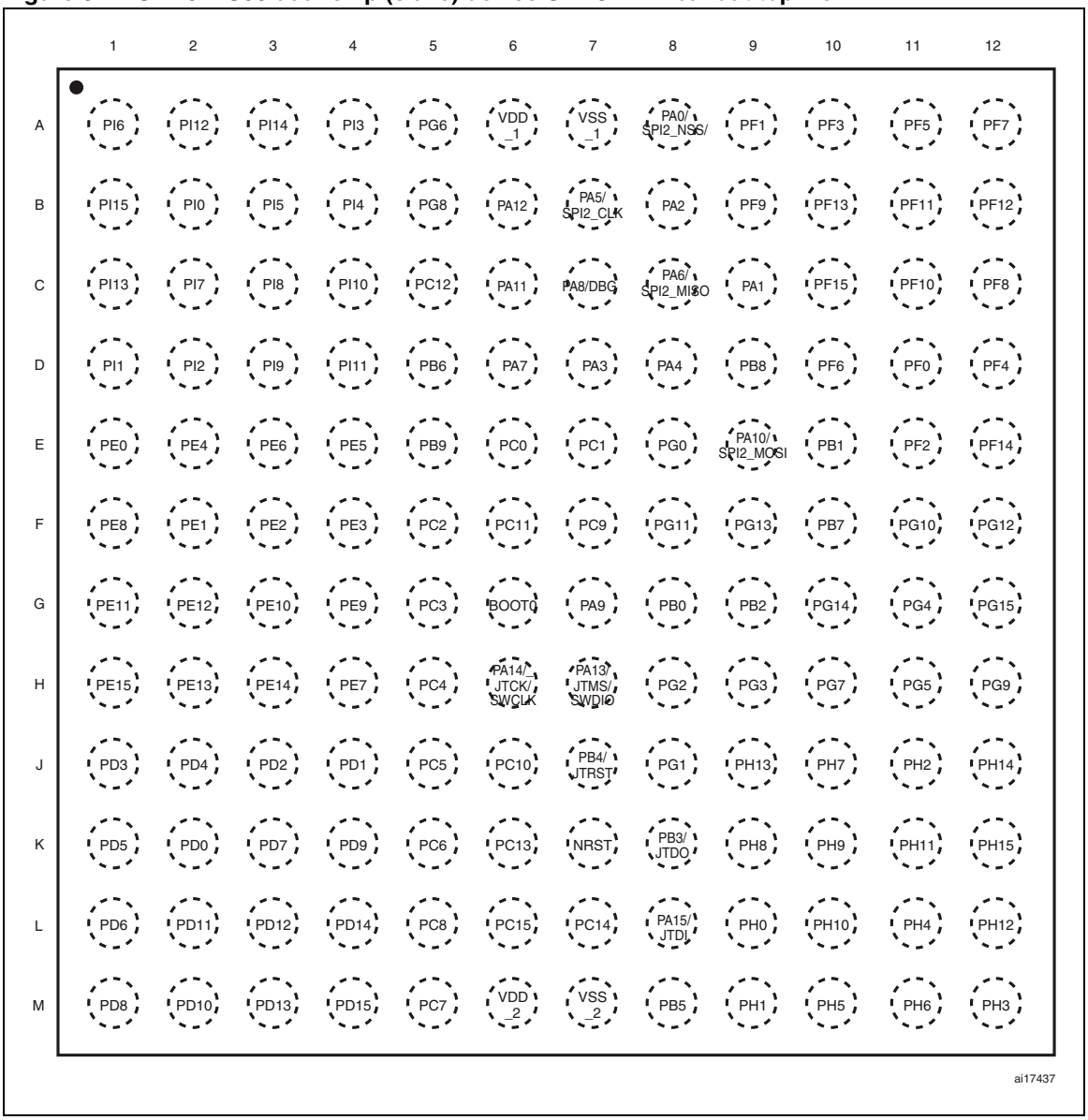


Table 2. STM32TS60 single-chip pin definitions

Pln no.	Pln type(1)	Pln level(2)	Pin name	Pin function
A1	O		PI6/COL	Touchpanel column
A2	O		PI12/COL	Touchpanel column
A3	O		PI14/COL	Touchpanel column
A4	O		PI3/COL	Touchpanel column
A5	O		PG6/COL	Touchpanel column
A6	S		VDD_1	Supply voltage pin 1
A7	S		VSS_1	Ground pin 1
A8	I		PA0/SPI_NSS/WAKEUP	SPI slave select from host Wakeup from host
A9	IO		PF1/COL/ROW	Touchpanel column Touchpanel row
A10	IO		PF3/COL/ROW	Touchpanel column Touchpanel row
A11	IO		PF5/COL/ROW	Touchpanel column Touchpanel row
A12	IO		PF7/COL/ROW	Touchpanel column Touchpanel row
B1	O		PI15/COL	Touchpanel column
B2	O		PI0/COL	Touchpanel column
B3	O		PI5/COL	Touchpanel column
B4	O		PI4/COL	Touchpanel column
B5	O		PG8/COL	Touchpanel column
B6	O		PA12/COL/OSC_OUT	Touchpanel column 16 MHz crystal/resonator oscillator output
B7	O	FT	PA5/USBPU	USB pull-up
B8	IO		PA2/USBDM	USB data-
B9	IO		PF9/COL/ROW	Touchpanel column Touchpanel row
B10	IO		PF13/COL/ROW	Touchpanel column Touchpanel row
B11	IO		PF11/COL/ROW	Touchpanel column Touchpanel row
B12	IO		PF12/COL/ROW	Touchpanel column Touchpanel row
C1	O		PI13/COL	Touchpanel column
C2	O		PI7/COL	Touchpanel column
C3	O		PI8/COL	Touchpanel column

Table 2. STM32TS60 single-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Pin name	Pin function
C4	O		PI10/COL	Touchpanel column
C5	IO		PC12/ROW	Touchpanel row
C6	O		PA11/COL/OSC_IN	Touchpanel column 16 MHz crystal/resonator oscillator input
C7	I	FT	PA8/NCHG	NCHG (pull-up required)
C8	OD		PA6/LED/DBG	Device activity LED Debug output
C9	IO		PA1/USBDP	USB data+
C10	IO		PF15/COL/ROW	Touchpanel column Touchpanel row
C11	IO		PF10/COL/ROW	Touchpanel column Touchpanel row
C12	IO		PF8/COL/ROW	Touchpanel column Touchpanel row
D1	O		PI1/COL	Touchpanel column
D2	O		PI2/COL	Touchpanel column
D3	O		PI9/COL	Touchpanel column
D4	O		PI11/COL	Touchpanel column
D5	O		PB6/COL	Touchpanel column
D6	I/I		PA7/SPI_SI/UART_RX	SPI slave in from host UART data receive from host
D7	I/OD	FT	PA3/SPI_CLK/I2C_SCL	SPI clock input from host I2C clock from/to host
D8	O/OD/O	FT	PA4/SPI_SO/I2C_SDA/UART_TX	SPI slave out to host I^2C data from/to host UART data transmit to host
D9	O		PB8/COL	Touchpanel column
D10	IO		PF6/COL/ROW	Touchpanel column Touchpanel row
D11	IO		PF0/COL/ROW	Touchpanel column Touchpanel row
D12	IO		PF4/COL/ROW	Touchpanel column Touchpanel row
E1	IO		PE0/ROW	Touchpanel row
E2	IO		PE4/ROW	Touchpanel row
E3	IO		PE6/ROW	Touchpanel row
E4	IO		PE5/ROW	Touchpanel row
E5	O		PB9/COL	Touchpanel column

Table 2. STM32TS60 single-chip pin definitions (continued)

Pln no.	Pln type(1)	Pln level(2)	Pin name	Pin function
E6	IO		PC0/ROW	Touchpanel row
E7	IO		PC1/ROW	Touchpanel row
E8	O		PG0/COL	Touchpanel column
E9	O		PA10/COL	Touchpanel column
E10	O		PB1/COL	Touchpanel column
E11	IO		PF2/COL/ROW	Touchpanel column Touchpanel row
E12	IO		PF14/COL/ROW	Touchpanel column Touchpanel row
F1	IO		PE8/ROW	Touchpanel row
F2	IO		PE1/ROW	Touchpanel row
F3	IO		PE2/ROW	Touchpanel row
F4	IO		PE3/ROW	Touchpanel row
F5	IO		PC2/ROW	Touchpanel row
F6	IO		PC11/ROW	Touchpanel row
F7	IO		PC9/ROW	Touchpanel row
F8	O		PG11/COL	Touchpanel column
F9	O		PG13/COL	Touchpanel column
F10	O		PB7/COL	Touchpanel column
F11	O		PG10/COL	Touchpanel column
F12	O		PG12/COL	Touchpanel column
G1	IO		PE11/ROW	Touchpanel row
G2	IO		PE12/ROW	Touchpanel row
G3	IO		PE10/ROW	Touchpanel row
G4	IO		PE9/ROW	Touchpanel row
G5	IO		PC3/ROW	Touchpanel row
G6	I		BOOT0	Boot mode selection
G7	O		PA9/COL	Touchpanel column
G8	O		PB0/COL	Touchpanel column
G9	O		PB2/COL	Touchpanel column
G10	O		PG14/COL	Touchpanel column
G11	O		PG4/COL	Touchpanel column
G12	O		PG15/COL	Touchpanel column
H1	IO		PE15/ROW	Touchpanel row
H2	IO		PE13/ROW	Touchpanel row

Table 2. STM32TS60 single-chip pin definitions (continued)

Pln no.	Pln type(1)	Pln level(2)	Pin name	Pin function
H3	IO		PE14/ROW	Touchpanel row
H4	IO		PE7/ROW	Touchpanel row
H5	IO		PC4/ROW	Touchpanel row
H6	O/I/I		PA14/COL/JTCK/SWCLK	Touchpanel column JTAG clock Serial wire clock
H7	O/I/OD		PA13/COL/JTMS/SWDIO	Touchpanel column JTAG mode selection Serial wire data input/output
H8	O		PG2/COL	Touchpanel column
H9	O		PG3/COL	Touchpanel column
H10	O		PG7/COL	Touchpanel column
H11	O		PG5/COL	Touchpanel column
H12	O		PG9/COL	Touchpanel column
J1	IO		PD3/ROW	Touchpanel row
J2	IO		PD4/ROW	Touchpanel row
J3	IO		PD2/ROW	Touchpanel row
J4	IO		PD1/ROW	Touchpanel row
J5	IO		PC5/ROW	Touchpanel row
J6	IO		PC10/ROW	Touchpanel row
J7	O/I		PB4/COL/JTRST	Touchpanel column JTAG reset
J8	O		PG1/COL	Touchpanel column
J9	O		PH13/COL	Touchpanel column
J10	O		PH7/COL	Touchpanel column
J11	O		PH2/COL	Touchpanel column
J12	O		PH14/COL	Touchpanel column
K1	IO		PD5/ROW	Touchpanel row
K2	IO		PD0/ROW	Touchpanel row
K3	IO		PD7/ROW	Touchpanel row
K4	IO		PD9/ROW	Touchpanel row
K5	IO		PC6/ROW	Touchpanel row
K6	IO		PC13/ROW	Touchpanel row
K7	I		NRST	Reset (active low)
K8	O/OD		PB3/COL/JTDO	Touchpanel column JTAG data output

Table 2. STM32TS60 single-chip pin definitions (continued)

Pin no.	Pin type(1)	Pin level(2)	Pin name	Pin function
K9	O		PH8/COL	Touchpanel column
K10	O		PH9/COL	Touchpanel column
K11	O		PH11/COL	Touchpanel column
K12	O		PH15/COL	Touchpanel column
L1	IO		PD6/ROW	Touchpanel row
L2	IO		PD11/ROW	Touchpanel row
L3	IO		PD12/ROW	Touchpanel row
L4	IO		PD14/ROW	Touchpanel row
L5	IO		PC8/ROW	Touchpanel row
L6	IO		PC15/ROW	Touchpanel row
L7	IO		PC14/ROW	Touchpanel row
L8	O/I		PA15/COL/JTDI	Touchpanel column JTAG data input
L9	O		PH0/COL	Touchpanel column
L10	O		PH10/COL	Touchpanel column
L11	O		PH4/COL	Touchpanel column
L12	O		PH12/COL	Touchpanel column
M1	IO		PD8/ROW	Touchpanel row
M2	IO		PD10/ROW	Touchpanel row
M3	IO		PD13/ROW	Touchpanel row
M4	IO		PD15/ROW	Touchpanel row
M5	IO		PC7/ROW	Touchpanel row
M6	S		VDD_2	Supply voltage pin 2
M7	S		VSS_2	Ground pin 2
M8	O		PB5/COL	Touchpanel column
M9	O		PH1/COL	Touchpanel column
M10	O		PH5/COL	Touchpanel column
M11	O		PH6/COL	Touchpanel column
M12	O		PH3/COL	Touchpanel column

1. I = input pin, O = output push-pull pin, IO = input/output pin, OD = output open drain pin, S = supply pin.
2. FT = 5 V tolerant

Table 3. STM32TS60 dual-chip pin definitions

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
A1	O		M/S	PI6/COL	Touchpanel column
A2	O		M/S	PI12/COL	Touchpanel column
A3	O		M/S	PI14/COL	Touchpanel column
A4	O		M/S	PI3/COL	Touchpanel column
A5	O		M/S	PG6/COL	Touchpanel column
A6	S		M/S	VDD_1	Supply voltage pin 1
A7	S		M/S	VSS_1	Ground pin 1
A8	I		M	PA0/SPI1_NSS/WAKEUP	SPI slave select from host Wakeup from host
			S	PA0/SPI2_NSS(3)	Interdevice SPI slave select
A9	IO		M/S	PF1/COL/ROW	Touchpanel column Touchpanel row
A10	IO		M/S	PF3/COL/ROW	Touchpanel column Touchpanel row
A11	IO		M/S	PF5/COL/ROW	Touchpanel column Touchpanel row
A12	IO		M/S	PF7/COL/ROW	Touchpanel column Touchpanel row
B1	O		M/S	PI15/COL	Touchpanel column
B2	O		M/S	PI0/COL	Touchpanel column
B3	O		M/S	PI5/COL	Touchpanel column
B4	O		M/S	PI4/COL	Touchpanel column
B5	O		M/S	PG8/COL	Touchpanel column
B6	O		M	PA12/COL/OSC_OUT	Touchpanel column 16 MHz crystal/resonator oscillator output
			S	PA12/COL	Touchpanel column
B7	O	FT	M/S	PA5/SPI2_CLK(3)	Interdevice SPI clock
B8	IO		M	PA2/USBDM	USB data-
			S	PA2	Not used
B9	IO		M/S	PF9/COL/ROW	Touchpanel column Touchpanel row
B10	IO		M/S	PF13/COL/ROW	Touchpanel column Touchpanel row

Table 3. STM32TS60 dual-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
B11	IO		M/S	PF11/COL/ROW	Touchpanel column Touchpanel row
B12	IO		M/S	PF12/COL/ROW	Touchpanel column Touchpanel row
C1	O		M/S	PI13/COL	Touchpanel column
C2	O		M/S	PI7/COL	Touchpanel column
C3	O		M/S	PI8/COL	Touchpanel column
C4	O		M/S	PI10/COL	Touchpanel column
C5	IO		M/S	PC12/ROW	Touchpanel row
C6	O		M	PA11/COL/OSC_IN	Touchpanel column 16 MHz crystal/resonator oscillator input
			S	PA11/COL	Touchpanel column
C7	I	FT	M	PA8/NCHG/DBG	NCHG (pullup required) Debug output
			S	PA8/DBG	Debug output
C8	OD		M/S	PA6/SPI2_MISO(3)	Interdevice SPI master in/slave out
C9	IO		M	PA1/USBDP	USB data+
			S	PA1	Not used
C10	IO		M/S	PF15/COL/ROW	Touchpanel column Touchpanel row
C11	IO		M/S	PF10/COL/ROW	Touchpanel column Touchpanel row
C12	IO		M/S	PF8/COL/ROW	Touchpanel column Touchpanel row
D1	O		M/S	PI1/COL	Touchpanel column
D2	O		M/S	PI2/COL	Touchpanel column
D3	O		M/S	PI9/COL	Touchpanel column
D4	O		M/S	PI11/COL	Touchpanel column
D5	O		M/S	PB6/COL	Touchpanel column
D6	I/I		M	PA7/SPI1_SI/UART_RX	SPI slave in from host UART data receive from host
			S	PA7	Not used

Table 3. STM32TS60 dual-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
D7	I/OD	FT	M	PA3/SPI1_CLK/I2C_SCL	SPI clock input from host I^2C clock from/to host
			S	PA3	Not used
D8	O/OD/O	FT	M	PA4/SPI1_SO/I2C_SDA/UART_TX	SPI slave out to host I^2C data from/to host UART data transmit to host
			S	PA4	Not used
D9	O		M/S	PB8/COL	Touchpanel column
D10	IO		M/S	PF6/COL/ROW	Touchpanel column Touchpanel row
D11	IO		M/S	PF0/COL/ROW	Touchpanel column Touchpanel row
D12	IO		M/S	PF4/COL/ROW	Touchpanel column Touchpanel row
E1	IO		M/S	PE0/ROW	Touchpanel row
E2	IO		M/S	PE4/ROW	Touchpanel row
E3	IO		M/S	PE6/ROW	Touchpanel row
E4	IO		M/S	PE5/ROW	Touchpanel row
E5	O		M/S	PB9/COL	Touchpanel column
E6	IO		M/S	PC0/ROW	Touchpanel row
E7	IO		M/S	PC1/ROW	Touchpanel row
E8	O		M/S	PG0/COL	Touchpanel column
E9	O		M/S	PA10/SPI2_MOSI(3)	Interdevice SPI master out/slave in
E10	O		M/S	PB1/COL	Touchpanel column
E11	IO		M/S	PF2/COL/ROW	Touchpanel column Touchpanel row
E12	IO		M/S	PF14/COL/ROW	Touchpanel column Touchpanel row
F1	IO		M/S	PE8/ROW	Touchpanel row
F2	IO		M/S	PE1/ROW	Touchpanel row
F3	IO		M/S	PE2/ROW	Touchpanel row
F4	IO		M/S	PE3/ROW	Touchpanel row
F5	IO		M/S	PC2/ROW	Touchpanel row
F6	IO		M/S	PC11/ROW	Touchpanel row

Table 3. STM32TS60 dual-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
F7	IO		M/S	PC9/ROW	Touchpanel row
F8	O		M/S	PG11/COL	Touchpanel column
F9	O		M/S	PG13/COL	Touchpanel column
F10	O		M/S	PB7/COL	Touchpanel column
F11	O		M/S	PG10/COL	Touchpanel column
F12	O		M/S	PG12/COL	Touchpanel column
G1	IO		M/S	PE11/ROW	Touchpanel row
G2	IO		M/S	PE12/ROW	Touchpanel row
G3	IO		M/S	PE10/ROW	Touchpanel row
G4	IO		M/S	PE9/ROW	Touchpanel row
G5	IO		M/S	PC3/ROW	Touchpanel row
G6	I		M/S	BOOT0	Boot mode selection
G7	O		M/S	PA9/USBPU	USB pullup
G8	O		M/S	PB0/COL	Touchpanel column
G9	O		M/S	PB2/COL	Touchpanel column
G10	O		M/S	PG14/COL	Touchpanel column
G11	O		M/S	PG4/COL	Touchpanel column
G12	O		M/S	PG15/COL	Touchpanel column
H1	IO		M/S	PE15/ROW	Touchpanel row
H2	IO		M/S	PE13/ROW	Touchpanel row
H3	IO		M/S	PE14/ROW	Touchpanel row
H4	IO		M/S	PE7/ROW	Touchpanel row
H5	IO		M/S	PC4/ROW	Touchpanel row
H6	O/I/I		M/S	PA14/COL/JTCK/SWCLK	Touchpanel column JTAG clock Serial wire clock
H7	O/I/OD		M/S	PA13/COL/JTMS/SWDIO	Touchpanel column JTAG mode selection Serial wire data input/output
H8	O		M/S	PG2/COL	Touchpanel column
H9	O		M/S	PG3/COL	Touchpanel column
H10	O		M/S	PG7/COL	Touchpanel column
H11	O		M/S	PG5/COL	Touchpanel column
H12	O		M/S	PG9/COL	Touchpanel column
J1	IO		M/S	PD3/ROW	Touchpanel row

Table 3. STM32TS60 dual-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
J2	IO		M/S	PD4/ROW	Touchpanel row
J3	IO		M/S	PD2/ROW	Touchpanel row
J4	IO		M/S	PD1/ROW	Touchpanel row
J5	IO		M/S	PC5/ROW	Touchpanel row
J6	IO		M/S	PC10/ROW	Touchpanel row
J7	O/I		M/S	PB4/COL/JTRST	Touchpanel column JTAG reset
J8	O		M/S	PG1/COL	Touchpanel column
J9	O		M/S	PH13/COL	Touchpanel column
J10	O		M/S	PH7/COL	Touchpanel column
J11	O		M/S	PH2/COL	Touchpanel column
J12	O		M/S	PH14/COL	Touchpanel column
K1	IO		M/S	PD5/ROW	Touchpanel row
K2	IO		M/S	PD0/ROW	Touchpanel row
K3	IO		M/S	PD7/ROW	Touchpanel row
K4	IO		M/S	PD9/ROW	Touchpanel row
K5	IO		M/S	PC6/ROW	Touchpanel row
K6	IO		M/S	PC13/ROW	Touchpanel row
K7	I		M/S	NRST	Reset (active low)
K8	O/OD		M/S	PB3/COL/JTDO	Touchpanel column JTAG data output
K9	O		M/S	PH8/COL	Touchpanel column
K10	O		M/S	PH9/COL	Touchpanel column
K11	O		M/S	PH11/COL	Touchpanel column
K12	O		M/S	PH15/COL	Touchpanel column
L1	IO		M/S	PD6/ROW	Touchpanel row
L2	IO		M/S	PD11/ROW	Touchpanel row
L3	IO		M/S	PD12/ROW	Touchpanel row
L4	IO		M/S	PD14/ROW	Touchpanel row
L5	IO		M/S	PC8/ROW	Touchpanel row
L6	IO		M/S	PC15/ROW	Touchpanel row
L7	IO		M/S	PC14/ROW	Touchpanel row

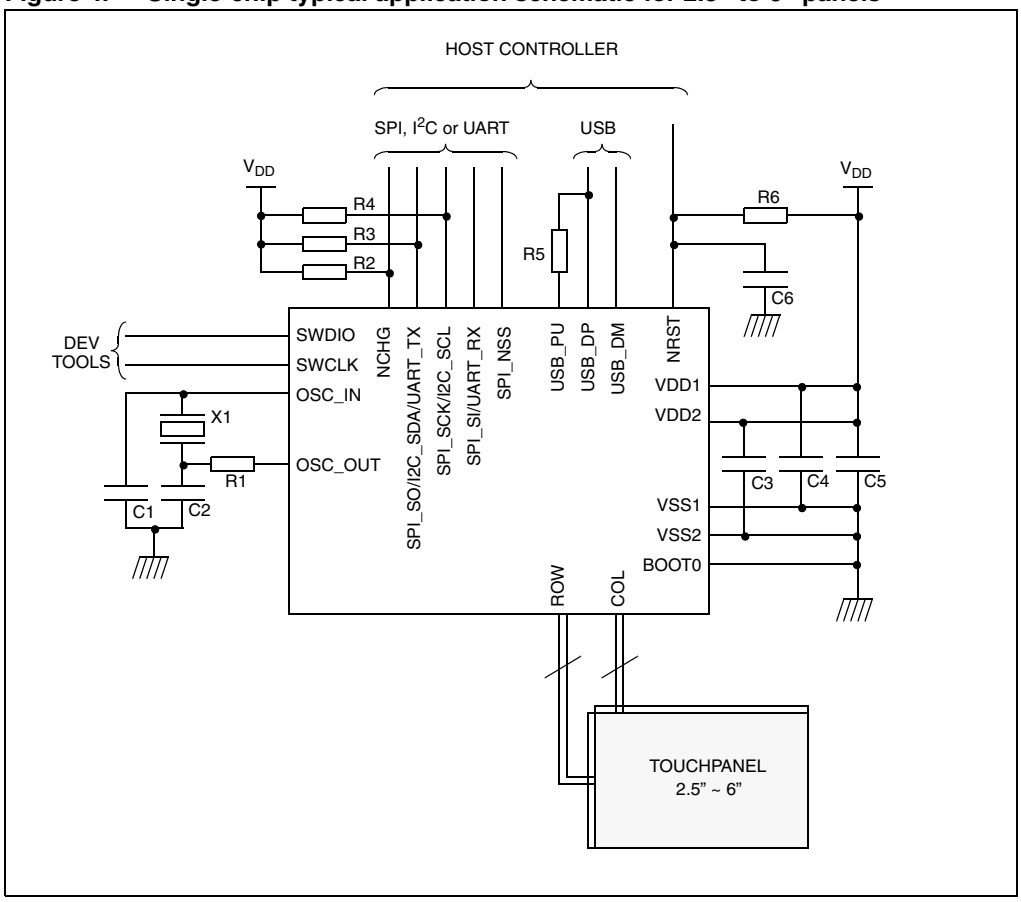
Table 3. STM32TS60 dual-chip pin definitions (continued)

PIn no.	PIn type(1)	PIn level(2)	Master (M) or slave (S) device	Pin name	Pin function
L8	O/I		M	PA15/SPI2_NSS(3)/JTDI	Interdevice SPI slave select JTAG data input
			S	PA15/COL/JTDI	Touchpanel column JTAG data input
L9	O		M/S	PH0/COL	Touchpanel column
L10	O		M/S	PH10/COL	Touchpanel column
L11	O		M/S	PH4/COL	Touchpanel column
L12	O		M/S	PH12/COL	Touchpanel column
M1	IO		M/S	PD8/ROW	Touchpanel row
M2	IO		M/S	PD10/ROW	Touchpanel row
M3	IO		M/S	PD13/ROW	Touchpanel row
M4	IO		M/S	PD15/ROW	Touchpanel row
M5	IO		M/S	PC7/ROW	Touchpanel row
M6	S		M/S	VDD_2	Supply voltage pin 2
M7	S		M/S	VSS_2	Ground pin 2
M8	O		M/S	PB5/COL	Touchpanel column
M9	O		M/S	PH1/COL	Touchpanel column
M10	O		M/S	PH5/COL	Touchpanel column
M11	O		M/S	PH6/COL	Touchpanel column
M12	O		M/S	PH3/COL	Touchpanel column

1. I = input pin, O = output push-pull pin, IO = input/output pin, OD = output open drain pin, S = supply pin.
2. FT = 5 V tolerant
3. The SPI2 is used to interconnect devices in multichip architecture solutions.

3 Application diagrams

Figure 4. Single-chip typical application schematic for 2.5” to 6” panels



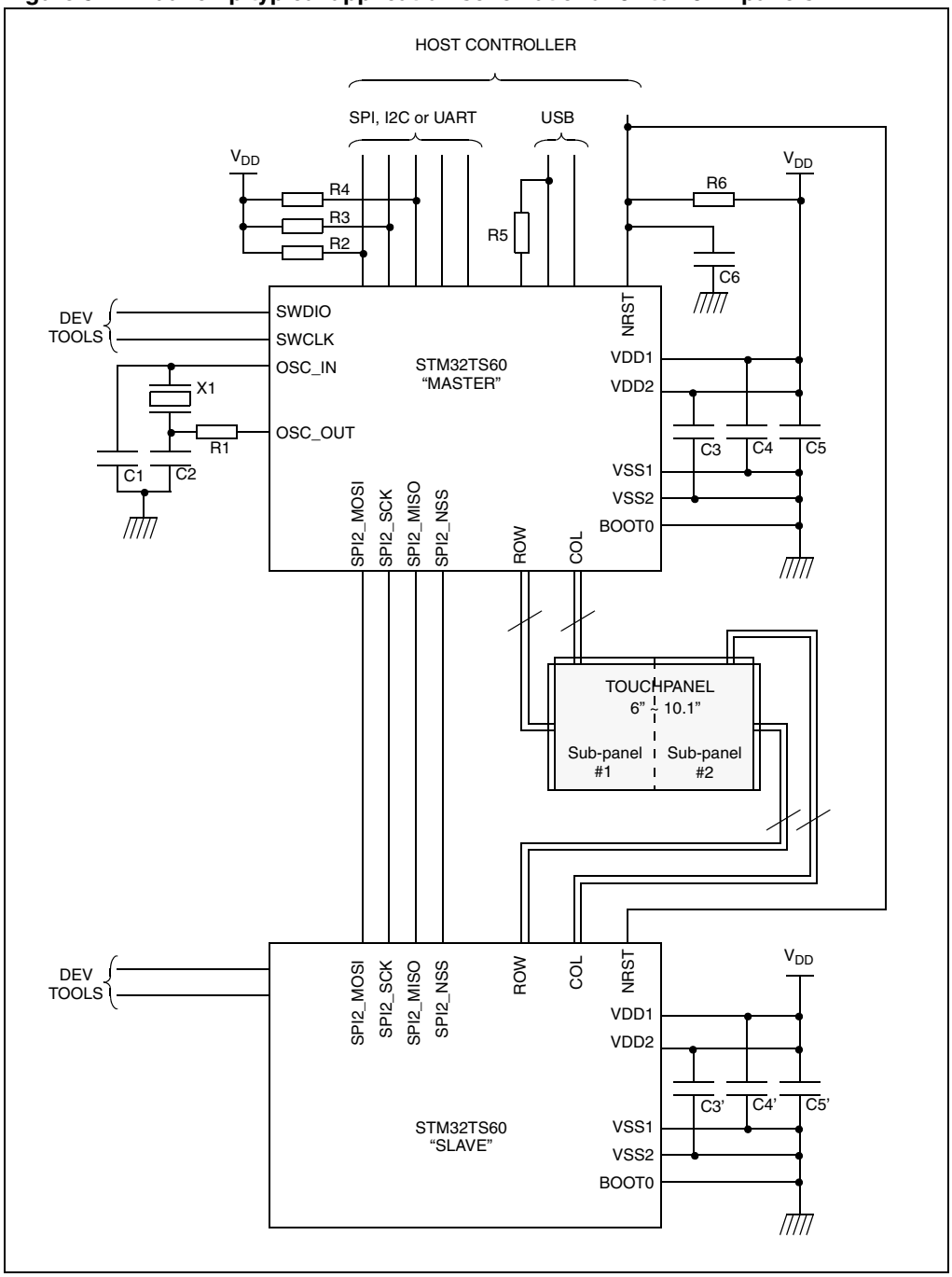
1. In single-chip architecture, up to 129 touchpanel signals are available, including a maximum of 81 columns and 64 rows.

Table 4. Single-chip typical application passive component list

Ref.	Typ. Value	Comment	Ref.	Typ. value	Comment
C1,C2	(1)	For USB interface only	C3,C4	100 nF	Decoupling capacitors
X1	16 MHz	For USB interface only	C5	1 µF	Filtering capacitors
R1	(1)	For USB interface only	C6	10 nF	Reset filter
R2	10 KΩ		R5	1.5 KΩ	For USB interface only
R3,R4	4.7 KΩ	For I2C interface only	R6	10 KΩ	Reset filter

1. Value depends on resonator or crystal characteristics.

Figure 5. Dual-chip typical application schematic for 6” to 10.1” panels



1. In dual-chip architecture, up to 124 touchpanel signals are available on master devices, including a maximum of 76 columns and 64 rows. On the slave side, up to 128 touchpanel signals are available, including a maximum of 80 columns and 64 rows.

Table 5. Dual-chip typical application passive component list

Ref.	Typ. value	Comment	Ref.	Typ. value	Comment
C1,C2	(1)	For USB interface only	C3,C4,C3',C4'	100 nF	Decoupling capacitors
X1	16 MHz	For USB interface only	C5, C5'	1 µF	Filtering capacitors
R1	(1)	For USB interface only	C6	10 nF	Reset filter
R2	10KΩ		R5	1.5 KΩ	For USB interface only
R3,R4	4.7KΩ	For I^2C interface only	R6	10 KΩ	Reset filter

1. Value depends on resonator or crystal characteristics.

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

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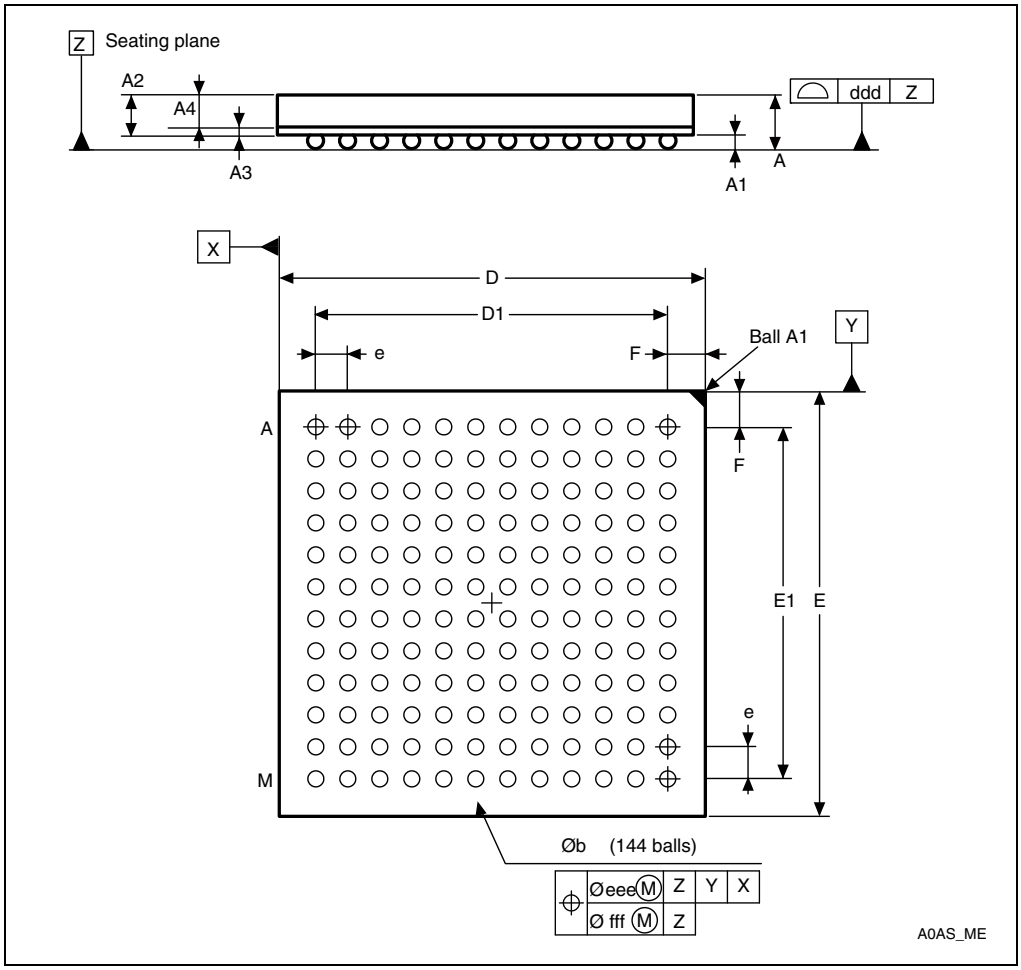
Figure 6. UFBGA144 - 7 x 7 mm ultra low profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 6. UFBGA144 - 7 x 7 mm ultra low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.530	0.460	0.600	0.0209	0.0181	0.0236
A1	0.080	0.060	0.100	0.0031	0.0024	0.0039
A2	0.450	0.400	0.500	0.0177	0.0157	0.0197
A3	0.130	0.080	0.180	0.0051	0.0031	0.0071
A4	0.320	0.270	0.370	0.0126	0.0106	0.0146
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	7.000	6.950	7.050	0.2756	0.2736	0.2776
D1	5.500	5.450	5.550	0.2165	0.2146	0.2185
E	7.000	6.950	7.050	0.2756	0.2736	0.2776
E1	5.500	5.450	5.550	0.2165	0.2146	0.2185
e	0.500	0.450	0.550	0.0197	0.0177	0.0217
F	0.750	0.700	0.800	0.0295	0.0276	0.0315
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.050			0.0020		

1. Values in inches are converted from mm and rounded to four decimal digits.

5 Ordering information

Table 7. Ordering information scheme

Example: **STM32 TS 60 Z H 6 xx y**

Device family

STM32 = ARM-based 32-bit microcontroller

Device sub-family

TS = touchscreen family

Touch sensing technology

60 = multitouch resistive

Pin count

Z = 144 pins

Package

H = UFBGA

Temperature range

6 = industrial temperature range –40°C to 85°C

Firmware configuration

Firmware revision

For further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Dec-2009	1	Initial release
02-Feb-2010	2	Updated *Table 1: STM32TS60 device summary*. Updated *Figure 1* and added *Figure 2* and *Figure 3* ballouts. Replaced *Table 2: STM32TS60 single-chip pin definitions*. Added *Table 3: STM32TS60 dual-chip pin definitions*. *Figure 4: Single-chip typical application schematic for 2.5" to 6" panels*: updated title and pins; added footnote. *Figure 5: Dual-chip typical application schematic for 6" to 10.1" panels*: updated title, added SPI2_NSS pin, and added footnote. Passive component list *Table 4* and *Table 5*: updated title and footnotes. Added *Section 4: Package mechanical data*. Renamed *Section 5: Ordering information*.

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