

# DDR2 SDRAM FBDIMM

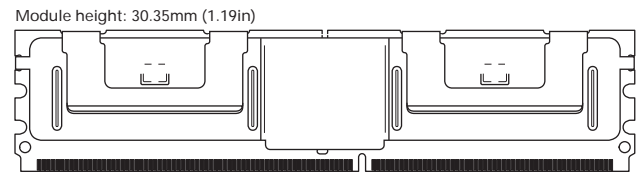
## MT36HTF51272FZ – 4GB

For the component data sheets, refer to Micron's Web site: [www.micron.com](http://www.micron.com)

### Features

- 240-pin, fully buffered dual in-line memory module (FBDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 4GB (512 Meg x 72)
- 3.2 Gb/s, 4 Gb/s, and 4.8 Gb/s link transfer rates
- SMBus interface to advanced memory buffer (AMB) for configuration register access
- High-speed, 1.5V differential, point-to-point link between host controller and AMB
- Fault-tolerant: can work around a bad bit lane in each direction
- High-density scaling: up to 8 FBDIMMs per channel
- In-band and out-of-band command access
- Deterministic protocol: enables memory controller to optimize DRAM accesses for maximum performance; delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis reduces intersymbol interference (ISI)
- MBIST and IBIST test functions
- Transparent mode for DRAM test support
- $V_{DD} = V_{DDQ} = +1.8V$  for DRAM
- $V_{REF} = 0.9V$  SDRAM command/address termination
- $V_{CC} = 1.5V$  for AMB
- $V_{DDSPD} = +3V$  to  $+3.6V$  for AMB and EEPROM
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank
- Supports 95°C operation with 2x refresh

Figure 1: 240-Pin FBDIMM (MO-256 R/C E)



### Options

- Package
  - 240-pin DIMM (halogen-free)
- Frequency/CAS latency (CL)
  - 2.5ns @ CL = 5 (DDR2-800)
  - 3ns @ CL = 5 (DDR2-667)

### Marking

Z  
-80E  
-667

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) |        |        |        | $t_{RCD}$ (ns) | $t_{RP}$ (ns) | $t_{RC}$ (ns) |
|-------------|-----------------------|------------------|--------|--------|--------|----------------|---------------|---------------|
|             |                       | CL = 6           | CL = 5 | CL = 4 | CL = 3 |                |               |               |
| -80E        | PC2-6400              | 800              | 800    | 533    | 400    | 12.5           | 12.5          | 55            |
| -667        | PC2-5300              | –                | 667    | 533    | 400    | 15             | 15            | 55            |
| -53E        | PC2-4200              | –                | –      | 533    | 400    | 15             | 15            | 55            |

**Table 2: Addressing**

| Parameter            | 4GB              |
|----------------------|------------------|
| Refresh count        | 8K               |
| Device bank address  | 8 BA[2:0]        |
| Device configuration | 1Gb (256 Meg x4) |
| Row address          | 16K A[13:0]      |
| Column address       | 2K A[11, 9:0]    |
| Module rank address  | 2 S#[1:0]        |

**Table 3: Part Numbers and Timing Parameters – 4GB**

 Base device: MT47H256M4,<sup>1</sup> 1Gb DDR2 SDRAM

| Part Number <sup>2</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Clock Cycles<br>(CL- <sup>t</sup> RCD- <sup>t</sup> RP) | Link Transfer Rate |
|--------------------------|----------------|---------------|------------------|----------------------------|---|--------------------|
| MT36HTF51272FZ-80E__     | 4GB            | 512 Meg x 72  | 6.4 GB/s         | 2.5ns/800 MT/s             | 5-5-5   | 4.8 GT/s           |
| MT36HTF51272FZ-667__     | 4GB            | 512 Meg x 72  | 5.3 GB/s         | 3ns/667 MT/s               | 5-5-5   | 4 GT/s             |

- Notes: 1. Data sheets for the base device can be found on Micron's Web site.  
 2. All part numbers end with a four-place code (not shown), designating component, PCB, and AMB revisions. Consult factory for current revision codes.  
 Example: MT36HTF51272FZ-667H1N8.

## General Description

The Micron FBDIMM adheres to the currently proposed industry specifications for FBDIMMs. The following specifications contain detailed information on FBDIMM design, interfaces, and theory of operation and are listed here for the system designers' convenience. Refer to the JEDEC Web site for available specifications.

- FBDIMM Design Specification – pending JEDEC approval
- FBDIMM: Architecture and Protocol – JESD206
- FBDIMM: Advanced Memory Buffer (AMB) – JESD82-20
- Design for Test, Design for Validation (DFx) Specification
- Serial Presence-Detect (SPD) for Fully Buffered DIMM – JEDEC Standard No. 21-C page 4.1.2.7-1

The MT36HTF51272FZ DDR2 SDRAM module is a high-bandwidth, large-capacity channel solution that has a narrow host interface. FBDIMMs use DDR2 SDRAM devices isolated from the channel behind an AMB buffer on the FBDIMM. Memory-device capacity remains high and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 2 on page 6, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase reliability and availability of the memory subsystem.

## Advanced Memory Buffer

The advanced memory buffer (AMB) isolates the DDR2 SDRAM devices from the channel. This single-chip component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, point-to-point interface at 1.5V. The AMB also enables buffering of memory traffic to support large memory capacities. Refer to the JEDEC JESD82-20 specification for further information.

## Pin Assignments and Descriptions

Table 4: Pin Assignments

| 240-Pin FBDIMM Front |                 |     |                    |     |                  |     |                   | 240-Pin FBDIMM Back |                 |     |                    |     |                  |     |                    |
|----------------------|-----------------|-----|--------------------|-----|------------------|-----|-------------------|---------------------|-----------------|-----|--------------------|-----|------------------|-----|--------------------|
| Pin                  | Symbol          | Pin | Symbol             | Pin | Symbol           | Pin | Symbol            | Pin                 | Symbol          | Pin | Symbol             | Pin | Symbol           |     |                    |
| 1                    | V <sub>DD</sub> | 31  | PN3                | 61  | PN9#             | 91  | PS9# <sup>1</sup> | 121                 | V <sub>DD</sub> | 151 | SN3                | 181 | SN9#             | 211 | SS9# <sup>1</sup>  |
| 2                    | V <sub>DD</sub> | 32  | PN3#               | 62  | V <sub>SS</sub>  | 92  | V <sub>SS</sub>   | 122                 | V <sub>DD</sub> | 152 | SN3#               | 182 | V <sub>SS</sub>  | 212 | V <sub>SS</sub>    |
| 3                    | V <sub>DD</sub> | 33  | V <sub>SS</sub>    | 63  | PN10             | 93  | PS5               | 123                 | V <sub>DD</sub> | 153 | V <sub>SS</sub>    | 183 | SN10             | 213 | SS5                |
| 4                    | V <sub>SS</sub> | 34  | PN4                | 64  | PN10#            | 94  | PS5#              | 124                 | V <sub>SS</sub> | 154 | SN4                | 184 | SN10#            | 214 | SS5#               |
| 5                    | V <sub>DD</sub> | 35  | PN4#               | 65  | V <sub>SS</sub>  | 95  | V <sub>SS</sub>   | 125                 | V <sub>DD</sub> | 155 | SN4#               | 185 | V <sub>SS</sub>  | 215 | V <sub>SS</sub>    |
| 6                    | V <sub>DD</sub> | 36  | V <sub>SS</sub>    | 66  | PN11             | 96  | PS6               | 126                 | V <sub>DD</sub> | 156 | V <sub>SS</sub>    | 186 | SN11             | 216 | SS6                |
| 7                    | V <sub>DD</sub> | 37  | PN5                | 67  | PN11#            | 97  | PS6#              | 127                 | V <sub>DD</sub> | 157 | SN5                | 187 | SN11#            | 217 | SS6#               |
| 8                    | V <sub>SS</sub> | 38  | PN5#               | 68  | V <sub>SS</sub>  | 98  | V <sub>SS</sub>   | 128                 | V <sub>SS</sub> | 158 | SN5#               | 188 | V <sub>SS</sub>  | 218 | V <sub>SS</sub>    |
| 9                    | V <sub>CC</sub> | 39  | V <sub>SS</sub>    | 69  | V <sub>SS</sub>  | 99  | PS7               | 129                 | V <sub>CC</sub> | 159 | V <sub>SS</sub>    | 189 | V <sub>SS</sub>  | 219 | SS7                |
| 10                   | V <sub>CC</sub> | 40  | PN13 <sup>1</sup>  | 70  | PS0              | 100 | PS7#              | 130                 | V <sub>CC</sub> | 160 | SN13 <sup>1</sup>  | 190 | SS0              | 220 | SS7#               |
| 11                   | V <sub>SS</sub> | 41  | PN13# <sup>1</sup> | 71  | PS0#             | 101 | V <sub>SS</sub>   | 131                 | V <sub>SS</sub> | 161 | SN13# <sup>1</sup> | 191 | SS0#             | 221 | V <sub>SS</sub>    |
| 12                   | V <sub>CC</sub> | 42  | V <sub>SS</sub>    | 72  | V <sub>SS</sub>  | 102 | PS8               | 132                 | V <sub>CC</sub> | 162 | V <sub>SS</sub>    | 192 | V <sub>SS</sub>  | 222 | SS8                |
| 13                   | V <sub>CC</sub> | 43  | V <sub>SS</sub>    | 73  | PS1              | 103 | PS8#              | 133                 | V <sub>CC</sub> | 163 | V <sub>SS</sub>    | 193 | SS1              | 223 | SS8#               |
| 14                   | V <sub>SS</sub> | 44  | DNU                | 74  | PS1#             | 104 | V <sub>SS</sub>   | 134                 | V <sub>SS</sub> | 164 | DNU                | 194 | SS1#             | 224 | V <sub>SS</sub>    |
| 15                   | V <sub>TT</sub> | 45  | DNU                | 75  | V <sub>SS</sub>  | 105 | DNU               | 135                 | V <sub>TT</sub> | 165 | DNU                | 195 | V <sub>SS</sub>  | 225 | DNU                |
| 16                   | DNU             | 46  | V <sub>SS</sub>    | 76  | PS2              | 106 | DNU               | 136                 | DNU             | 166 | V <sub>SS</sub>    | 196 | SS2              | 226 | DNU                |
| 17                   | RESET#          | 47  | V <sub>SS</sub>    | 77  | PS2#             | 107 | V <sub>SS</sub>   | 137                 | M_TEST (DNU)    | 167 | V <sub>SS</sub>    | 197 | SS2#             | 227 | V <sub>SS</sub>    |
| 18                   | V <sub>SS</sub> | 48  | PN12 <sup>1</sup>  | 78  | V <sub>SS</sub>  | 108 | V <sub>DD</sub>   | 138                 | V <sub>SS</sub> | 168 | SN12 <sup>1</sup>  | 198 | V <sub>SS</sub>  | 228 | SCK                |
| 19                   | DNU             | 49  | PN12# <sup>1</sup> | 79  | PS3              | 109 | V <sub>DD</sub>   | 139                 | DNU             | 169 | SN12# <sup>1</sup> | 199 | SS3              | 229 | SCK#               |
| 20                   | DNU             | 50  | V <sub>SS</sub>    | 80  | PS3#             | 110 | V <sub>SS</sub>   | 140                 | DNU             | 170 | V <sub>SS</sub>    | 200 | SS3#             | 230 | V <sub>SS</sub>    |
| 21                   | V <sub>SS</sub> | 51  | PN6                | 81  | V <sub>SS</sub>  | 111 | V <sub>DD</sub>   | 141                 | V <sub>SS</sub> | 171 | SN6                | 201 | V <sub>SS</sub>  | 231 | V <sub>DD</sub>    |
| 22                   | PNO             | 52  | PN6#               | 82  | PS4              | 112 | V <sub>DD</sub>   | 142                 | SN0             | 172 | SN6#               | 202 | SS4              | 232 | V <sub>DD</sub>    |
| 23                   | PNO#            | 53  | V <sub>SS</sub>    | 83  | PS4#             | 113 | V <sub>DD</sub>   | 143                 | SN0#            | 173 | V <sub>SS</sub>    | 203 | SS4#             | 233 | V <sub>DD</sub>    |
| 24                   | V <sub>SS</sub> | 54  | PN7                | 84  | V <sub>SS</sub>  | 114 | V <sub>SS</sub>   | 144                 | V <sub>SS</sub> | 174 | SN7                | 204 | V <sub>SS</sub>  | 234 | V <sub>SS</sub>    |
| 25                   | PN1             | 55  | PN7#               | 85  | V <sub>SS</sub>  | 115 | V <sub>DD</sub>   | 145                 | SN1             | 175 | SN7#               | 205 | V <sub>SS</sub>  | 235 | V <sub>DD</sub>    |
| 26                   | PN1#            | 56  | V <sub>SS</sub>    | 86  | DNU              | 116 | V <sub>DD</sub>   | 146                 | SN1#            | 176 | V <sub>SS</sub>    | 206 | DNU              | 236 | V <sub>DD</sub>    |
| 27                   | V <sub>SS</sub> | 57  | PN8                | 87  | DNU              | 117 | V <sub>TT</sub>   | 147                 | V <sub>SS</sub> | 177 | SN8                | 207 | DNU              | 237 | V <sub>TT</sub>    |
| 28                   | PN2             | 58  | PN8#               | 88  | V <sub>SS</sub>  | 118 | SA2               | 148                 | SN2             | 178 | SN8#               | 208 | V <sub>SS</sub>  | 238 | V <sub>DDSPD</sub> |
| 29                   | PN2#            | 59  | V <sub>SS</sub>    | 89  | V <sub>SS</sub>  | 119 | SDA               | 149                 | SN2#            | 179 | V <sub>SS</sub>    | 209 | V <sub>SS</sub>  | 239 | SA0                |
| 30                   | V <sub>SS</sub> | 60  | PN9                | 90  | PS9 <sup>1</sup> | 120 | SCL               | 150                 | V <sub>SS</sub> | 180 | SN9                | 210 | SS9 <sup>1</sup> | 240 | SA1                |

Notes: 1. The following signals are cyclic redundancy check (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, and SS9/SS9#.

**Table 5: Pin Descriptions**

| Symbol             | Type   | Description   |
|--------------------|--------|---|
| PS[9:0]            | Input  | Primary southbound data, positive lines.  |
| PS#[9:0]           | Input  | Primary southbound data, negative lines.  |
| SCL                | Input  | Serial presence-detect (SPD) clock input.   |
| SCK                | Input  | System clock input, positive line.  |
| SCK#               | Input  | System clock input, negative line.  |
| SS[9:0]            | Input  | Secondary southbound data, positive lines.  |
| SS#[9:0]           | Input  | Secondary southbound data, negative lines.  |
| PN[13:0]           | Output | Primary northbound data, positive lines.  |
| PN#[13:0]          | Output | Primary northbound data, negative lines.  |
| SN[13:0]           | Output | Secondary northbound data, positive lines.  |
| SN#[13:0]          | Output | Secondary northbound data, negative lines.  |
| SA[2:0]            | I/O    | SPD address inputs; also used to select the FBDIMM number in the AMB.   |
| SDA                | I/O    | SPD data input/output.  |
| RESET#             | Supply | AMB reset signal.   |
| V <sub>CC</sub>    | Supply | AMB core power and AMB channel interface power (1.5V).  |
| V <sub>DD</sub>    | Supply | DRAM power and AMB DRAM I/O power (1.8V).   |
| V <sub>DDSPD</sub> | Supply | SPD/AMB SMBus power (3.3V).   |
| V <sub>SS</sub>    | Supply | Ground.   |
| V <sub>TT</sub>    | Supply | DRAM address/command/clock termination power ( $V_{DD}/2$ ).  |
| M_TEST             | -      | The M_TEST pin provides an external connection for testing the margin of V <sub>REF</sub> , which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time. |
| DNU                | -      | Do not use.   |

## Block Diagrams

Figure 2: System Block Diagram

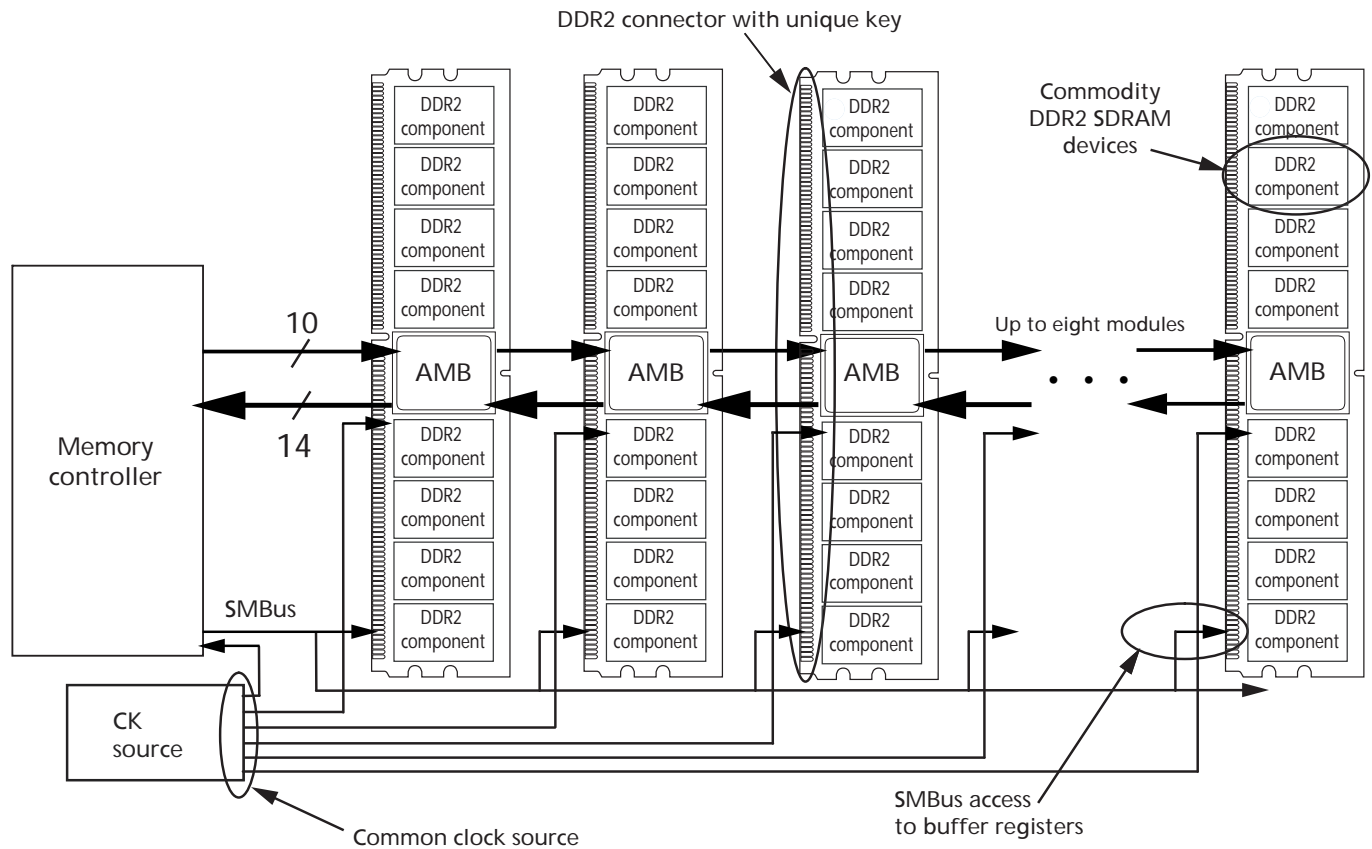
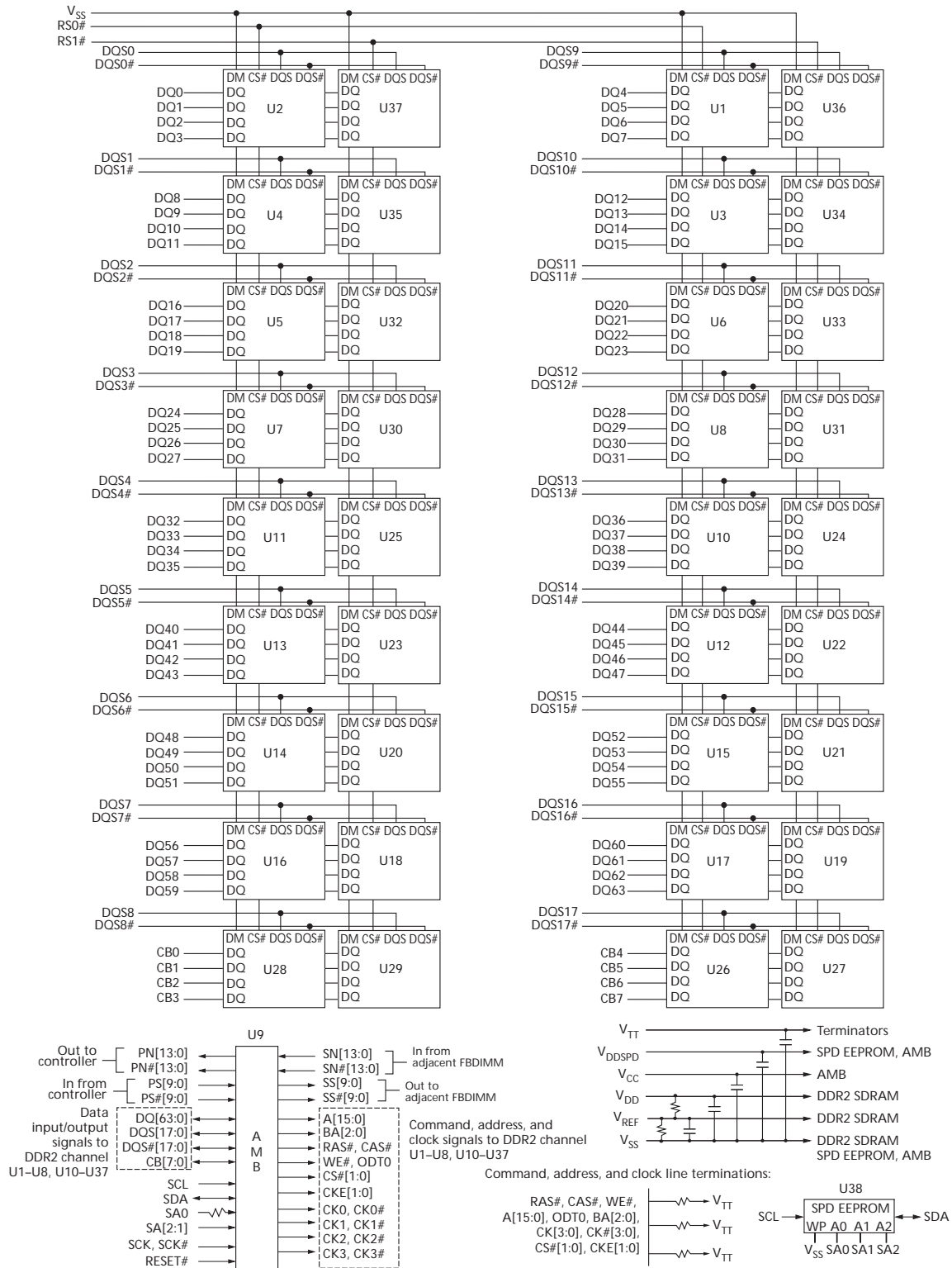


Figure 3: Functional Block Diagram



## Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the DRAM devices on the module. This is a stress rating only and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 6: Absolute Maximum Ratings**

| Parameter                                    | Symbol            | Min  | Max   | Units | Notes |
|--|-------------------|------|-------|-------|-------|
| Voltage on any pin relative to $V_{SS}$      | $V_{IN}, V_{OUT}$ | -0.3 | +1.75 | V     | 1     |
| Voltage on $V_{CC}$ pin relative to $V_{SS}$ | $V_{CC}$          | -0.3 | +1.75 | V     |       |
| Voltage on $V_{DD}$ pin relative to $V_{SS}$ | $V_{DD}$          | -0.5 | +2.3  | V     |       |
| Voltage on $V_{TT}$ pin relative to $V_{SS}$ | $V_{TT}$          | -0.5 | +2.3  | V     |       |
| DDR2 SDRAM device operating case temperature | $T_C$             | 0    | +95   | °C    | 2, 3  |
| AMB device operating temperature             |                   | 0    | +110  | °C    |       |

- Notes: 1.  $V_{IN}$  should not be greater than  $V_{CC}$ .  
 2.  $T_C$  is specified at 95°C only when using 2x refresh timing ( $t_{REFI} = 7.8\mu s$  at or below 85°C;  $t_{REFI} = 3.9\mu s$  above 85°C); refer to the DDR2 SDRAM component data sheet.  
 3. See applicable DDR2 SDRAM component data sheet for  $t_{REFI}$  and extended mode register settings. The  $t_{REFI}$  parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

**Table 7: Input DC Voltage and Operating Conditions**

| Parameter                          | Symbol       | Min                  | Nom                 | Max                  | Units   | Notes |
|------------------------------------|--------------|----------------------|---------------------|----------------------|---------|-------|
| AMB supply voltage                 | $V_{CC}$     | 1.46                 | 1.5                 | 1.54                 | V       |       |
| DDR2 SDRAM supply voltage          | $V_{DD}$     | 1.7                  | 1.8                 | 1.9                  | V       |       |
| Termination voltage                | $V_{TT}$     | $0.48 \times V_{DD}$ | $0.5 \times V_{DD}$ | $0.52 \times V_{DD}$ | V       |       |
| EEPROM supply voltage              | $V_{DDSPD}$  | 3                    | 3.3                 | 3.6                  | V       | 1     |
| SPD input high (logic 1) voltage   | $V_{IH(DC)}$ | 2.1                  | -                   | $V_{DDSPD}$          | V       | 2     |
| SPD input low (logic 0) voltage    | $V_{IL(DC)}$ | -                    | -                   | 0.8                  | V       | 2     |
| RESET input high (logic 1) voltage | $V_{IH(DC)}$ | 1                    | -                   | -                    | V       | 3     |
| RESET input low (logic 0) voltage  | $V_{IL(DC)}$ | -                    | -                   | 0.5                  | V       | 2     |
| Leakage current (RESET)            | $I_L$        | -90                  | -                   | +90                  | $\mu A$ | 3     |
| Leakage current (link)             | $I_L$        | -5                   | -                   | +5                   | $\mu A$ | 4     |

- Notes: 1. Applies to AMB and SPD.  
 2. Applies to serial memory buffer (SMB) and SPD bus signals.  
 3. Applies to AMB CMOS signal RESET#.  
 4. For all other AMB-related DC parameters, please refer to the high-speed differential link interface specification.



**Table 8: AMB Clock Ratios**

| FBDIMM Data Rate | DDR Data Link | Core Frequency | Reference Clock | FBDIMM Link: Core | Core: DDR |
|------------------|---------------|----------------|-----------------|-------------------|-----------|
| 4.0 Gb/s         | 666 Mb/s      | 333 MHz        | 167 MHz         | 12:1              | 1:2       |
| 4.8 Gb/s         | 800 Mb/s      | 400 MHz        | 200 MHz         | 12:1              | 1:2       |

## I<sub>DD</sub> Specifications and Conditions

**Table 9: I<sub>DD</sub> Conditions**

| Symbol                   | Condition  |
|--------------------------|--|
| I <sub>DD-Idle_0</sub>   | Idle current, single, or last DIMM: Low state; Idle (0 percent bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active                                      |
| I <sub>DD-Idle_1</sub>   | Idle current, first DIMM: Low state; Idle (0 percent bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active   |
| I <sub>DD-Active_1</sub> | Active power: Low state; 50 percent DRAM bandwidth; 67 percent READ, 33 percent WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH   |
| I <sub>DD-Active_2</sub> | Active power, data pass through: Low state; 50 percent DRAM bandwidth to downstream DIMM, 67 percent READ; 33 percent WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable |
| I <sub>DD-Training</sub> | Training: Primary and secondary channels enabled; 100 percent toggle on all channel lanes; DRAMs idle, 0 percent bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active  |
| I <sub>DD-IBIST</sub>    | IBIST over all IBIST modes: DRAM idle (0 percent bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active   |
| I <sub>DD-EI</sub>       | Electrical idle: DRAM idle (0 percent bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW                                      |

Notes: 1. Actual test conditions may vary from published JEDEC test conditions.

**Table 10: I<sub>DD</sub> Specifications – 4GB DDR2-667**

| Symbol          | I <sub>DD-Idle_0</sub> | I <sub>DD-Idle_1</sub> | I <sub>DD-Active_1</sub> | I <sub>DD-Active_2</sub> | I <sub>DD-Training</sub> | I <sub>DD-IBIST</sub> | I <sub>DD-EI</sub> | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I <sub>CC</sub> | 2600                   | 3400                   | 3900                     | 3700                     | 4000                     | 4500                  | 2500               | mA    |
| I <sub>DD</sub> | 2340                   | 2340                   | 3995                     | 2340                     | 2340                     | 2340                  | 452                | mA    |
| Total power     | 8.5                    | 9.8                    | 13.7                     | 10.3                     | 10.7                     | 11.5                  | 4.8                | W     |

**Table 11: I<sub>DD</sub> Specifications – 4GB DDR2-800**

| Symbol          | I <sub>DD-Idle_0</sub> | I <sub>DD-Idle_1</sub> | I <sub>DD-Active_1</sub> | I <sub>DD-Active_2</sub> | I <sub>DD-Training</sub> | I <sub>DD-IBIST</sub> | I <sub>DD-EI</sub> | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I <sub>CC</sub> | TBD                    | TBD                    | TBD                      | TBD                      | TBD                      | TBD                   | TBD                | mA    |
| I <sub>DD</sub> | TBD                    | TBD                    | TBD                      | TBD                      | TBD                      | TBD                   | TBD                | mA    |
| Total power     | TBD                    | TBD                    | TBD                      | TBD                      | TBD                      | TBD                   | TBD                | W     |

Notes: 1. Total power is based on maximum voltage levels, I<sub>CC</sub> @ 1.575V and I<sub>DD</sub> @ 1.9V.

## Serial Presence-Detect

**Table 12: Serial Presence-Detect EEPROM DC Operating Conditions**  
All voltages referenced to  $V_{SS}$

| Parameter/Condition  | Symbol      | Min                    | Max                    | Units         |
|--|-------------|------------------------|------------------------|---------------|
| EEPROM and AMB supply voltage                              | $V_{DDSPD}$ | 3                      | 3.6                    | V             |
| Input high voltage: Logic 1; all inputs                    | $V_{IH}$    | $V_{DDSPD} \times 0.7$ | $V_{DDSPD} + 0.5$      | V             |
| Input low voltage: Logic 0; all inputs                     | $V_{IL}$    | -0.6                   | $V_{DDSPD} \times 0.3$ | V             |
| Output low voltage: $I_{OUT} = 3\text{mA}$                 | $V_{OL}$    | -                      | 0.4                    | V             |
| Input leakage current: $V_{IN} = \text{GND to } V_{DD}$    | $I_{LI}$    | 0.10                   | 3                      | $\mu\text{A}$ |
| Output leakage current: $V_{OUT} = \text{GND to } V_{DD}$  | $I_{LO}$    | 0.05                   | 3                      | $\mu\text{A}$ |
| Standby current  | $I_{SB}$    | 1.6                    | 4                      | $\mu\text{A}$ |
| Power supply current, READ: SCL clock frequency = 100 kHz  | $I_{CCR}$   | 0.4                    | 1                      | mA            |
| Power supply current, WRITE: SCL clock frequency = 100 kHz | $I_{CCW}$   | 2                      | 3                      | mA            |

**Table 13: Serial Presence-Detect EEPROM AC Operating Conditions**  
All voltages referenced to  $V_{SS}$

| Parameter/Condition   | Symbol       | Min | Max | Units         | Notes |
|---|--------------|-----|-----|---------------|-------|
| SCL LOW to SDA data-out valid                               | $t_{AA}$     | 0.2 | 0.9 | $\mu\text{s}$ | 1     |
| Time the bus must be free before a new transition can start | $t_{BUF}$    | 1.3 | -   | $\mu\text{s}$ |       |
| Data-out hold time  | $t_{DH}$     | 200 | -   | ns            |       |
| SDA and SCL fall time                                       | $t_F$        | -   | 300 | ns            | 2     |
| Data-in hold time   | $t_{HD:DAT}$ | 0   | -   | $\mu\text{s}$ |       |
| Start condition hold time                                   | $t_{HD:STA}$ | 0.6 | -   | $\mu\text{s}$ |       |
| Clock HIGH period   | $t_{HIGH}$   | 0.6 | -   | $\mu\text{s}$ |       |
| Noise suppression time constant at SCL, SDA inputs          | $t_I$        | -   | 50  | ns            |       |
| Clock LOW period  | $t_{LOW}$    | 1.3 | -   | $\mu\text{s}$ |       |
| SDA and SCL rise time                                       | $t_R$        | -   | 0.3 | $\mu\text{s}$ | 2     |
| SCL clock frequency   | $f_{SCL}$    | -   | 400 | kHz           |       |
| Data-in setup time  | $t_{SU:DAT}$ | 100 | -   | ns            |       |
| Start condition setup time                                  | $t_{SU:STA}$ | 0.6 | -   | $\mu\text{s}$ | 3     |
| Stop condition setup time                                   | $t_{SU:STO}$ | 0.6 | -   | $\mu\text{s}$ |       |
| WRITE cycle time  | $t_{WRC}$    | -   | 10  | ms            | 4     |

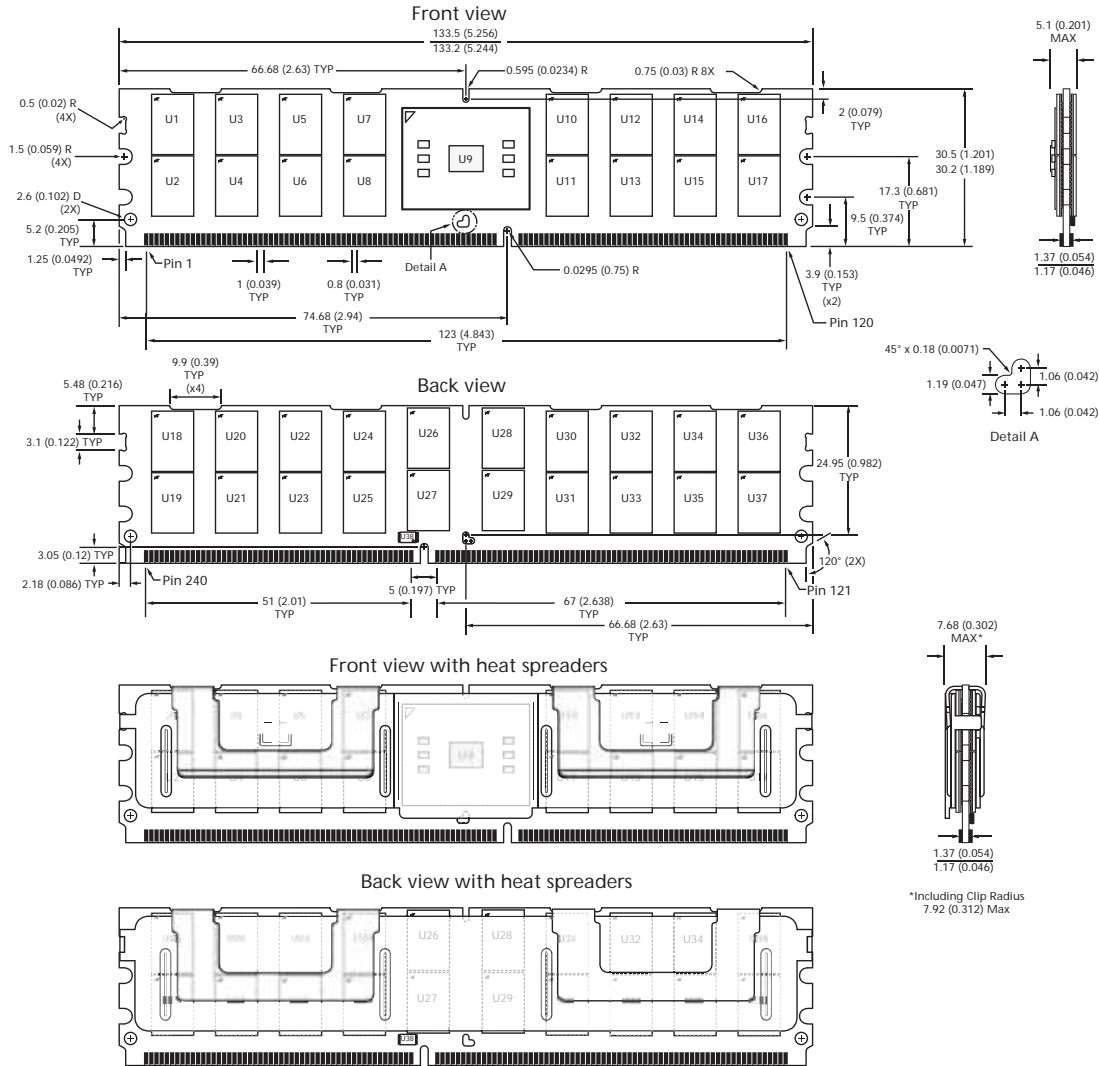
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
  2. This parameter is sampled.
  3. For a restart condition, or following a WRITE cycle.
  4. The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

## Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:  
[www.micron.com/SPD](http://www.micron.com/SPD).

## Module Dimensions

Figure 4: 240-pin DDR2 FBDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.