12-Bit, 20/40/65 MSPS 3 V A/D Converter

AD9235

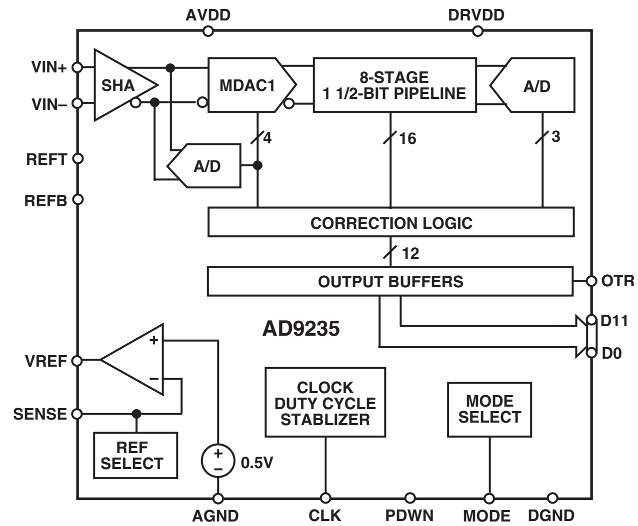
FEATURES

Single 3 V Supply Operation (2.7 V to 3.6 V)
SNR = 70 dBc to Nyquist at 65 MSPS
SFDR = 85 dBc to Nyquist at 65 MSPS
Low Power: 300 mW at 65 MSPS
Differential Input with 500 MHz Bandwidth
On-Chip Reference and SHA
DNL = ±0.4 LSB
Flexible Analog Input: 1 V p-p to 2 V p-p Range
Offset Binary or Twos Complement Data Format
Clock Duty Cycle Stabilizer

APPLICATIONS

Ultrasound Equipment
IF Sampling in Communications Receivers:
IS-95, CDMA-One, IMT-2000
Battery-Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9235 is a family of monolithic, single 3 V supply, 12-bit, 20/40/65 MSPS analog-to-digital converters. This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20/40/65 MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available analog-to-digital converters, the AD9235 is suitable for applications in communications, imaging, and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-lead thin shrink small outline package (TSSOP) and a 32-lead chip scale package (LFCSP) and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. The AD9235 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 300 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 100 MHz and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214-65, a 10-bit, 65 MSPS ADC. This allows a simplified upgrade path from 10 bits to 12 bits for 65 MSPS systems.
5. The clock DCS maintains overall ADC performance over a wide range of clock pulsewidths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD9235–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Temp	Test Level	AD9235BRU-20 Min	AD9235BRU-20 Typ	AD9235BRU-20 Max	AD9235BRU-40 Min	AD9235BRU-40 Typ	AD9235BRU-40 Max	AD9235BRU/BCP-65 Min	AD9235BRU/BCP-65 Typ	AD9235BRU/BCP-65 Max	Unit
RESOLUTION	Full	VI	12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	VI		±0.30	±1.20		±0.50	±1.20		±0.50	±1.20	% FSR
Gain Error[1]	Full	VI		±0.30	±2.40		±0.50	±2.50		±0.50	±2.60	% FSR
Differential Nonlinearity (DNL)[2]	Full	IV		±0.35	±0.65		±0.35	±0.75		±0.40	±0.80	LSB
	25°C	I		±0.35			±0.35			±0.35		LSB
Integral Nonlinearity (INL)[2]	Full	IV		±0.45	±0.80		±0.50	±0.90		±0.70	±1.30	LSB
	25°C	I		±0.40			±0.40			±0.45		LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±2			±2			±3		ppm/°C
Gain Error[1]	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5	±35		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	25°C	V		0.54			0.54			0.54		LSB rms
VREF = 1.0 V	25°C	V		0.27			0.27			0.27		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5 V	Full	IV		1			1			1		V p-p
Input Span, VREF = 1.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	V		30			55			100		mA
IDRVDD[2]	Full	V		2			5			7		mA
PSRR	Full	V		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		90			165			300		mW
Sine Wave Input[2]	Full	VI		95	110		180	205		320	350	mW
Standby Power[5]	Full	V		1.0			1.0			1.0		mW

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).

[2]Measured at maximum clock rate, f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.

[3]Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2 for the equivalent analog input structure.

[4]Measured with dc input at maximum clock rate.

[5]Standby power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Parameter	Temp	Test Level	AD9235BRU-20 Min	Typ	Max	AD9235BRU-40 Min	Typ	Max	AD9235BRU/BCP-65 Min	Typ	Max	Unit
LOGIC INPUTS												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	–10		+10	–10		+10	–10		+10	µA
Low Level Input Current	Full	IV	–10		+10	–10		+10	–10		+10	µA
Input Capacitance	Full	V		2			2			2		pF
LOGIC OUTPUTS*												
DRVDD = 3.3 V												
High-Level Output Voltage (IOH = 50 µA)	Full	IV	3.29			3.29			3.29			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	3.25			3.25			3.25			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)	Full	IV			0.05			0.05			0.05	V
DRVDD = 2.5 V												
High-Level Output Voltage (IOH = 50 µA)	Full	IV	2.49			2.49			2.49			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	2.45			2.45			2.45			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)	Full	IV			0.05			0.05			0.05	V

*Output voltage levels measured with 5 pF load on each output.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

Parameter	Temp	Test Level	AD9235BRU-20 Min	Typ	Max	AD9235BRU-40 Min	Typ	Max	AD9235BRU/BCP-65 Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS												
Maximum Conversion Rate	Full	VI	20			40			65			MSPS
Minimum Conversion Rate	Full	V			1			1			1	MSPS
CLK Period	Full	V	50.0			25.0			15.4			ns
CLK Pulsewidth High[1]	Full	V	15.0			8.8			6.2			ns
CLK Pulsewidth Low[1]	Full	V	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETERS												
Output Delay[2] (t_{PD})	Full	V		3.5			3.5			3.5		ns
Pipeline Delay (Latency)	Full	V		7			7			7		Cycles
Aperture Delay (t_A)	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty Jitter (t_J)	Full	V		0.5			0.5			0.5		ps rms
Wake-Up Time[3]	Full	V		3.0			3.0			3.0		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		1			1			2		Cycles

NOTES
[1]For the AD9235-65 model only, with duty cycle stabilizer enabled. DCS function not applicable for -20 and -40 models.
[2]Output delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load on each output.
[3]Wake-up time is dependent on value of decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

Specifications subject to change without notice.

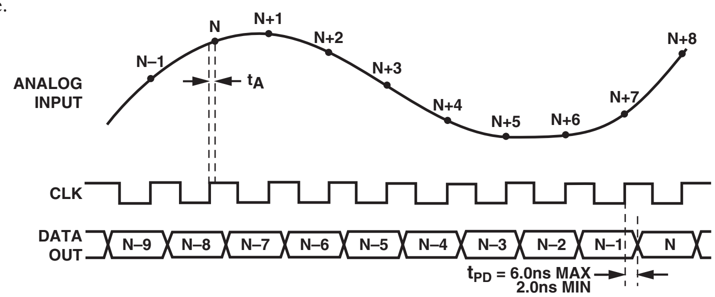


Figure 1. Timing Diagram

AD9235–SPECIFICATIONS

AC SPECIFICATIONS

(AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, AIN = –0.5 dBFS, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Temp	Test Level	AD9235BRU-20			AD9235BRU-40			AD9235BRU/BCP-65			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		70.8			70.6			70.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV	70.0	70.4								dBc
	25°C	I		70.6								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.9	70.3					dBc
	25°C	I					70.4					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.7	69.7		dBc
	25°C	I								70.1		dBc
f_{INPUT} = 100 MHz	25°C	V		68.7			68.5			68.3		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		70.6			70.5			70.4		dBc
f_{INPUT} = 9.7 MHz	Full	IV	69.9	70.3								dBc
	25°C	I		70.5								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.7	70.2					dBc
	25°C	I					70.3					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.3	69.5		dBc
	25°C	I								69.9		dBc
f_{INPUT} = 100 MHz	25°C	V		68.6			68.3			67.8		dBc
TOTAL HARMONIC DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		–88.0			–89.0			–87.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV		–86.0	–79.0							dBc
	25°C	I		–87.4								dBc
f_{INPUT} = 19.6 MHz	Full	IV					–85.5	–79.0				dBc
	25°C	I					–86.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV								–81.8	–74.0	dBc
	25°C	I								–82.0		dBc
f_{INPUT} = 100 MHz	25°C	V		–84.0			–82.5			–78.0		dBc
WORST HARMONIC (Second or Third)												
f_{INPUT} = 9.7 MHz	Full	IV		–90.0	–80.0							dBc
f_{INPUT} = 19.6 MHz	Full	IV					–90.0	–80.0				dBc
f_{INPUT} = 32.5 MHz	Full	IV								–83.5	–74.0	dBc
SPURIOUS FREE DYNAMIC RANGE												
f_{INPUT} = 2.4 MHz	25°C	V		92.0			92.0			92.0		dBc
f_{INPUT} = 9.7 MHz	Full	IV	80.0	88.5								dBc
	25°C	I		91.0								dBc
f_{INPUT} = 19.6 MHz	Full	IV				80.0	89.0					dBc
	25°C	I					90.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV							74.0	83.0		dBc
	25°C	I								85.0		dBc
f_{INPUT} = 100 MHz	25°C	V		84.0			85.0			80.5		dBc

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DGND	–0.3	+3.9	V
AGND	DGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
Digital Outputs	DGND	–0.3	DRVDD + 0.3	V
CLK, MODE	AGND	–0.3	AVDD + 0.3	V
VIN+, VIN–	AGND	–0.3	AVDD + 0.3	V
VREF	AGND	–0.3	AVDD + 0.3	V
SENSE	AGND	–0.3	AVDD + 0.3	V
REFB, REFT	AGND	–0.3	AVDD + 0.3	V
PDWN	AGND	–0.3	AVDD + 0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		–40	+85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		–65	+150	°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances (28-lead TSSOP), θ_{JA} = 67.7°C/W; (32-lead LFCSP), θ_{JA} = 32.5°C/W, θ_{JC} = 32.71°C/W. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-1.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9235BRU-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRU-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRU-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BCP-20*	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP) (Contact Factory)	CP-32
AD9235BCP-40*	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP) (Contact Factory)	CP-32
AD9235BCP-65*	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32
AD9235-20PCB		TSSOP Evaluation Board	
AD9235-40PCB		TSSOP Evaluation Board	
AD9235-65PCB		TSSOP Evaluation Board	
AD9235BCP-20EB		LFCSP Evaluation Board (Contact Factory)	
AD9235BCP-40EB		LFCSP Evaluation Board (Contact Factory)	
AD9235BCP-65EB		LFCSP Evaluation Board	

*It is recommended that the exposed paddle be soldered to the ground plane. There is an increased reliability of the solder joints and maximum thermal capability of the package is achieved with exposed paddle soldered to the customer board.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9235 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.