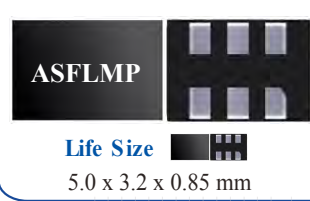


# PERFORMANCE PLASTIC PACKAGE ULTRA MINIATURE PURE SILICON™ CLOCK OSCILLATOR



ASFLMP



**Low Jitter  
High Performance  
3G MEMS Technology!**

## FEATURES:

- Ultra Miniature Pure Silicon™ Clock Oscillator
- High Performance MEMS Technology by Discera
- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- Available in 50kG Shock Resistance Configuration upon request
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc

## APPLICATIONS:

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T, KR/LR/SR, FCoE)
- HD/SD/SDI Video & Surveillance
- PCI Express
- Display port

## STANDARD SPECIFICATIONS:

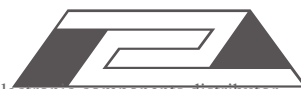
### Common Key Electrical Specifications – CMOS, LVPECL, LVDS, and HCSL

Parameters		Minimum	Typical	Maximum	Units	Notes
Frequency Range	CMOS	10.000	-----	170.000	MHz	Commercial, Industrial Temp range
	CMOS	10.000	-----	100.000		Automotive -55 ~ +125°C
	LVPECL	10.000	-----	425.000		Commercial, Industrial Temp range
	LVDS	10.000	-----	425.000		Commercial, Industrial Temp range
	HCSL	10.000	-----	425.000		Commercial, Industrial Temp range
Operating Temperature		-20	-----	+70	°C	See options
Storage Temperature		-55	-----	+150	°C	
Overall Frequency Stability*		-50	-----	+50	ppm	See options
Supply Voltage (Vdd)		+2.25	-----	+3.6	V	
Startup Time		-----	-----	10	ms	
Enable Time		-----	-----	0.005	ms	STD (Tri-state)
		-----	-----	10.0		PD option (Power Down)
Disable Time		-----	-----	100	ns	
Stand-by Current		-----	20	26	mA	STD (Tri-state)
Disable Current		-----	-----	0.1		PD option (Power Down)
Tri-state Function (Standby/Disable)		"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd) : Hi Z			V	33kΩ pull-up resistor embedded
Aging		-5.0	-----	+5.0	ppm	First year

### Key Electrical Specifications – CMOS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I <sub>dd</sub> )		-----	31	35	mA	CL=15p, 125MHz
Output Logic Level	V <sub>OH</sub>	0.9*V <sub>dd</sub>	-----	-----	V	I=±6mA
	V <sub>OL</sub>	-----	-----	0.1*V <sub>dd</sub>	V	
Rise Time	T <sub>r</sub>	-----	1.1	2.0	ns	CL=15pF
Fall Time	T <sub>f</sub>	-----	1.3	2.0	ns	20%/80%*VDD
Duty Cycle		45	-----	55	%	
Spurious Level				-50	dBc	Reference to carrier
Integrated Phase Jitter (J <sub>PH</sub> )		-----	0.35	3	ps	200kHz ~ 20MHz, 125MHz
		-----	0.5	3		100kHz ~ 20MHz, 125MHz
		-----	1.8	3		12kHz ~ 20MHz, 125MHz
Period Jitter RMS (J <sub>PER</sub> )		-----	4.3	-----	ps	CL=2pF, 125MHz
		-----	6	-----		CL=15pF, 125MHz

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ASFLMP

Life Size  
5.0 x 3.2 x 0.85 mm

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RoHS  
Compliant

## Key Electrical Specifications – LVPECL

Parameters	Minimum	Typical	Maximum	Units	Notes	
Supply Current ( $I_{dd}$ )	-----	51	60	mA	RL=50Ω, 156.25MHz	
Output Logic Level	$V_{OH}$	$V_{dd}-1.08$	-----	V	RL=50Ω, 156.25MHz	
	$V_{OL}$	-----	$V_{dd}-1.55$	V		
Peak to Peak Output Swing ( $V_{pp}$ )		830		mV	Single ended	
Rise Time	$T_r$	-----	250		RL=50Ω, CL=2pF 20%/80%*VDD	
Fall Time	$T_f$	-----	250	ps		
Duty Cycle		48	-----	52	%	Differential
Spurious Level				-50	dBc	Reference to carrier
Integrated Phase Jitter ( $J_{PH}$ )		-----	0.35	3	ps	200kHz ~ 20MHz, 156.25MHz
		-----	0.5	3		100kHz ~ 20MHz, 156.25MHz
		-----	1.8	3		12kHz ~ 20MHz, 156.25MHz
Period Jitter RMS ( $J_{PER}$ )		-----	3.3	-----	ps	RL=50Ω, 156.25MHz

## Key Electrical Specifications – LVDS

Parameters	Minimum	Typical	Maximum	Units	Notes	
Supply Current ( $I_{dd}$ )	-----	29	40	mA	RL=50Ω, 156.25MHz	
Output Offset Voltage ( $V_{OS}$ )	1.125	-----	1.4	V	RL=100Ω differential	
Delta Offset Voltage ( $\Delta V_{OS}$ )						
Output Logic Level	$V_{OH}$	$V_{dd}-1.08$	-----	V	RL=50Ω, 156.25MHz	
	$V_{OL}$	-----	$V_{dd}-1.55$	V		
Peak to Peak Output Swing ( $V_{pp}$ )		350		mV	Single ended	
Rise Time	$T_r$	-----	300		RL=50Ω, CL=2pF 20%/80%*VDD	
Fall Time	$T_f$	-----	300	ps		
Duty Cycle		45	-----	55	%	Differential
Spurious Level				-50	dBc	Reference to carrier
Integrated Phase Jitter ( $J_{PH}$ )		-----	0.43	3	ps	200kHz ~ 20MHz, 156.25MHz
		-----	0.55	3		100kHz ~ 20MHz, 156.25MHz
		-----	1.8	3		12kHz ~ 20MHz, 156.25MHz
Period Jitter RMS ( $J_{PER}$ )		-----	3.3	-----	ps	RL=50Ω, 156.25MHz

## Key Electrical Specifications – HCSL

Parameters	Minimum	Typical	Maximum	Units	Notes	
Supply Current ( $I_{dd}$ )	-----	40	60	mA	RL=50Ω, 156.25MHz	
Output Logic Level	$V_{OH}$	0.725	-----	V	RL=50Ω, 156.25MHz	
	$V_{OL}$	-----	0.1	V		
Peak to Peak Output Swing ( $V_{pp}$ )		675		mV	Single ended	
Rise Time	$T_r$	-----	250		RL=50Ω, CL=2pF 20%/80%*VDD	
Fall Time	$T_f$	-----	250	ps		
Duty Cycle		45	-----	55	%	Differential
Spurious Level				-50	dBc	Reference to carrier
Integrated Phase Jitter ( $J_{PH}$ )		-----	0.3	3	ps	200kHz ~ 20MHz, 156.25MHz
		-----	0.45	3		100kHz ~ 20MHz, 156.25MHz
		-----	1.9	3		12kHz ~ 20MHz, 156.25MHz
Period Jitter RMS ( $J_{PER}$ )		-----	2.8	-----	ps	RL=50Ω, 156.25MHz

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Life Size



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RoHS  
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## Absolute Maximum Ratings

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	Vdd+0.3	V	
Junction Temp.	-----	+150	°C	
Storage Temp.	-55	+150	°C	
Soldering Temp.	-----	+260	°C	40sec max
ESD			V	
HBM		4,000		
MM		200		
CDM		1,500		

## OPTIONS AND PART IDENTIFICATION: (Left Blank if Standard)

### Programmed Orders (Quantity > 1,000pcs)

ASFLMP  -  MHz -   -  -

Output Type	Frequency in MHz	Operating Temp.	Overall Freq. Stability	Tri-state (Pin 1)	Packaging
C: CMOS	e.g. 156.2500 MHz (Maximum 4 digits after decimal)	Blank: -20°C ~ +70°C	Blank: ±50ppm	Blank: Tri-state	Blank: Tube (72pcs / Tube)
LP: LVPECL		L: -40°C ~ +85°C	Y: ±10ppm*	PD: Power Down	T: Tape & Reel (1kpcs / reel)
LV: LVDS		X: -40°C ~ +105°C	R: ±25 ppm		
HC: HCSL		Z: -55°C ~ +125°C			

\*-20°C ~ +70°C, option L, or X only.

### Un-Programmed Orders

Blank un-programmed oscillators and our low cost portable programmer are available for quick turn engineering requirements. Please call ABRACON or visit MEMSpeed Pro II site <http://www.abracon.com/memspeedpro/MEMSpeedProFlyerII.pdf> for more information.

ASFLMP  - BLANK -   -

Output Type	Operating Temp.	Overall Freq. Stability	Packaging
C: CMOS	Blank: -20°C ~ +70°C	Blank: ±50ppm	Blank: Tube (72pcs / Tube)
LP: LVPECL	L: -40°C ~ +85°C	Y: ±10ppm*	T: Tape & Reel (1kpcs / reel)
LV: LVDS	X: -40°C ~ +105°C	R: ±25 ppm	
HC: HCSL	Z: -55°C ~ +125°C		

\*-20°C ~ +70°C, option L, or X only.

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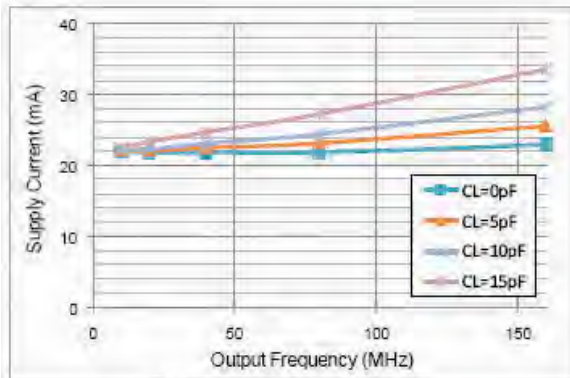
ASFLMP



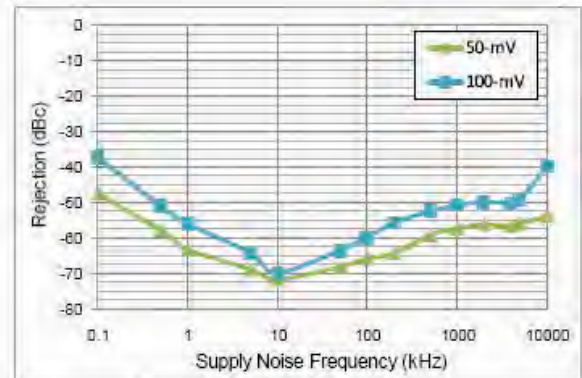
## NOMINAL PERFORMANCE PARAMETERS

(Unless specified otherwise: T=25° C, VDD=3.3 V)

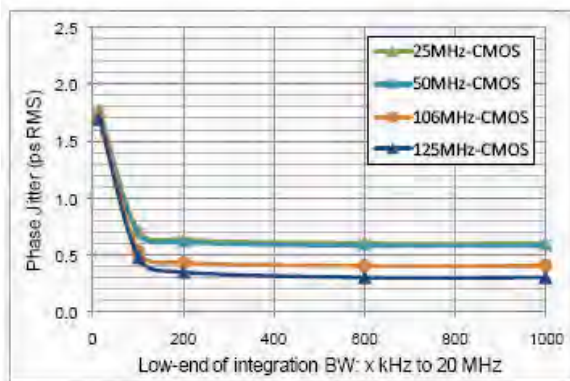
### CMOS OUTPUT



Supply current over freq

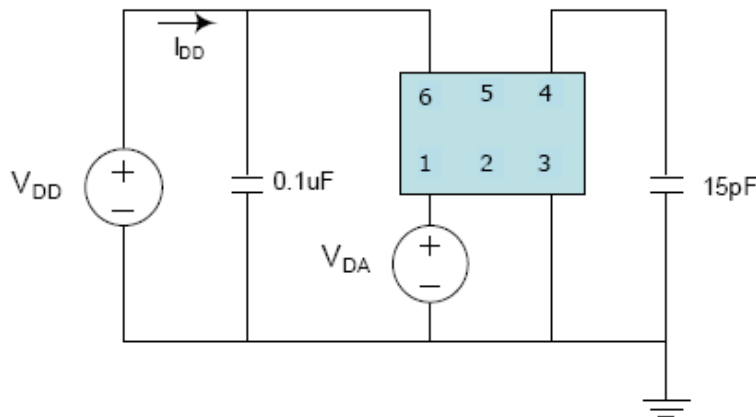


Power supply rejection ratio



Phase jitter (integrated phase noise)

### Test Circuit



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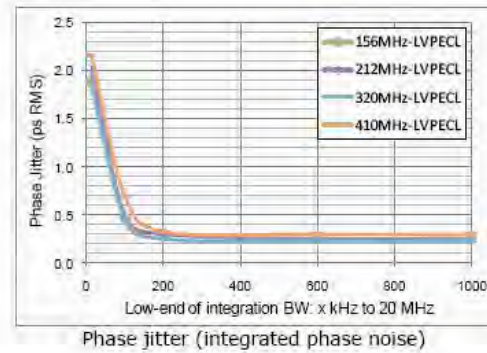
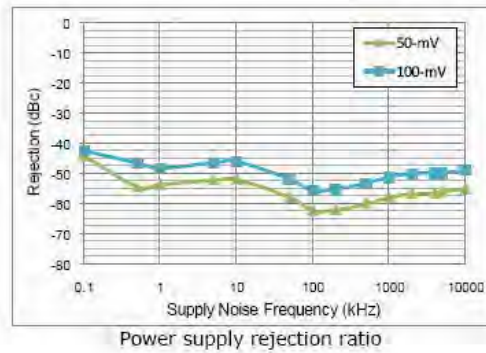


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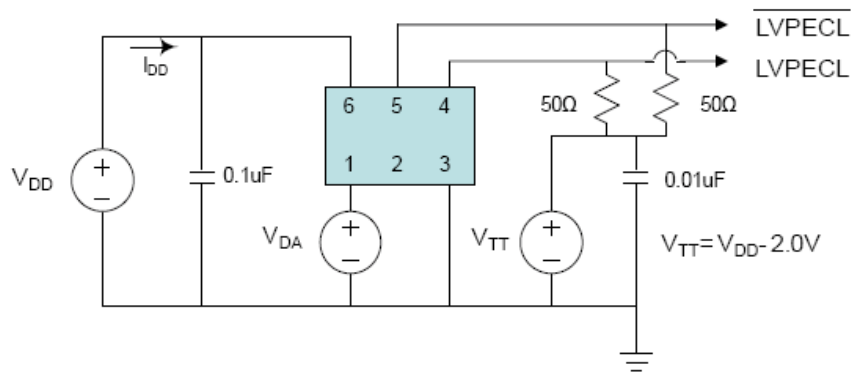
ASFLMP



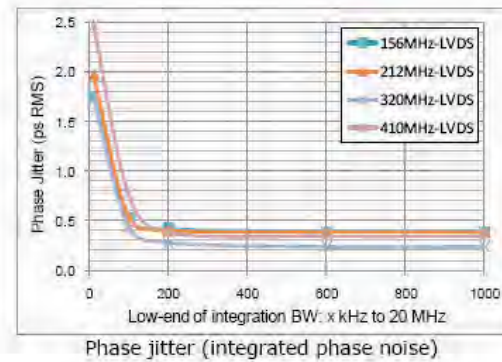
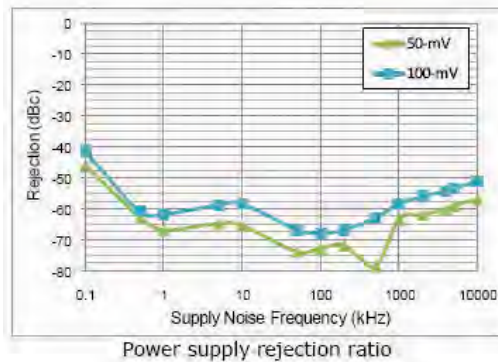
## LVPECL OUTPUT



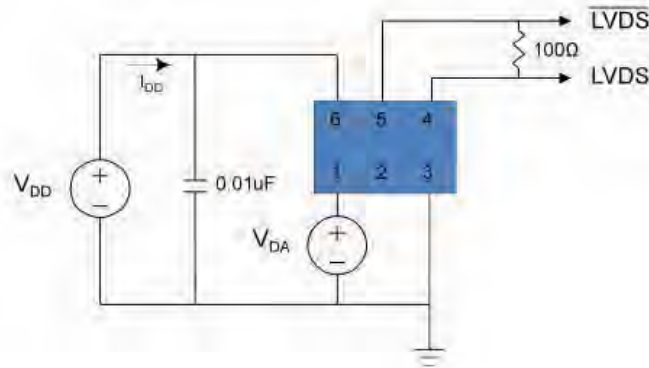
## Test Circuit



## LVDS OUTPUT



## Test Circuit



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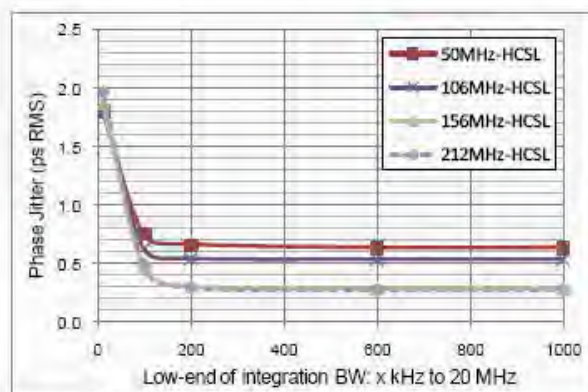
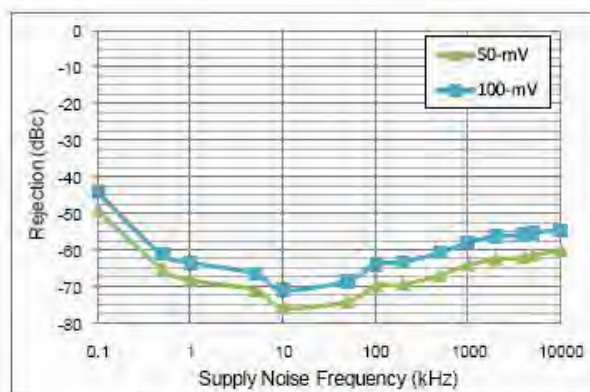
RoHS  
Compliant

Life Size

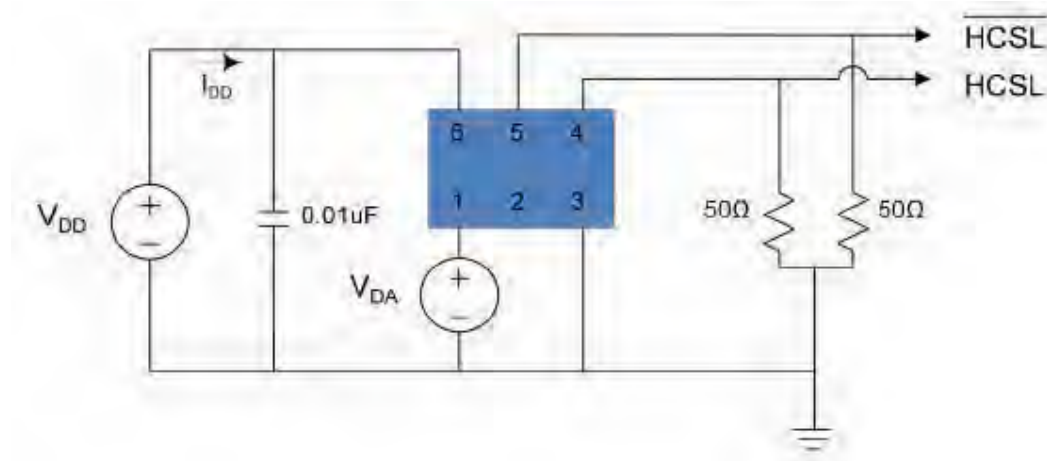


5.0 x 3.2 x 0.85 mm

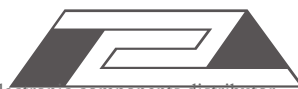
## HCSL OUTPUT



## Test Circuit



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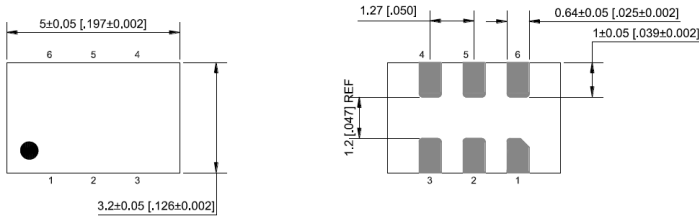


Life Size  
5.0 x 3.2 x 0.85 mm

ASFLMP



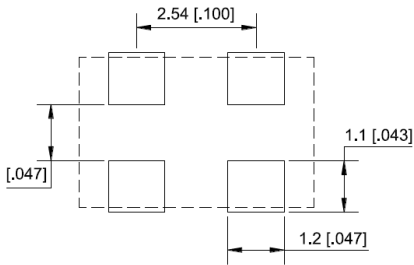
## OUTLINE DIMENSIONS:



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	nc
6	VDD

### Recommended Solder Pad Layout

units: mm [Inch]

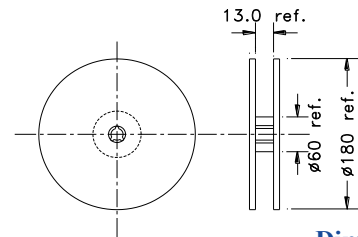
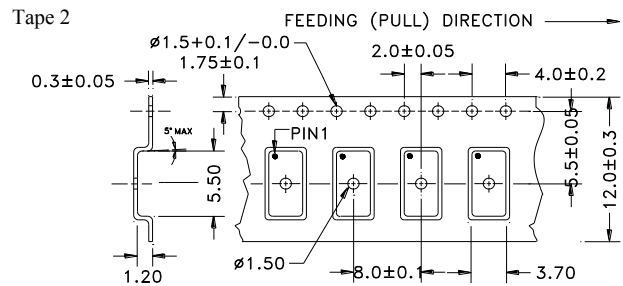
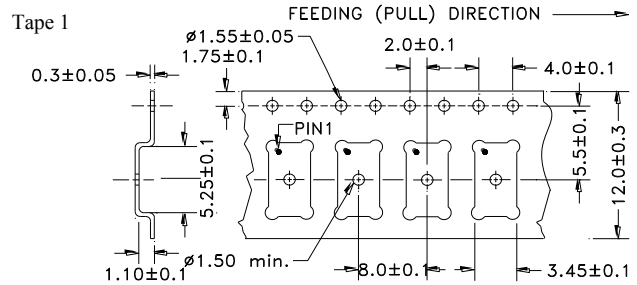


Note: Recommend using an approximately 0.01µF bypass capacitor between PIN 6 and 3.

Dimensions: mm (inches)

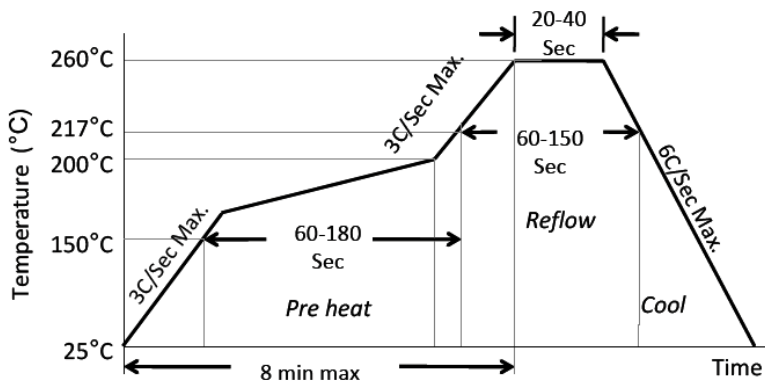
## TAPE AND REEL:

T= Tape and reel (1,000pcs/reel)



Dimensions: mm

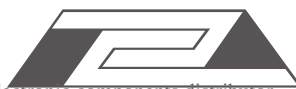
## REFLOW PROFILE:



Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

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