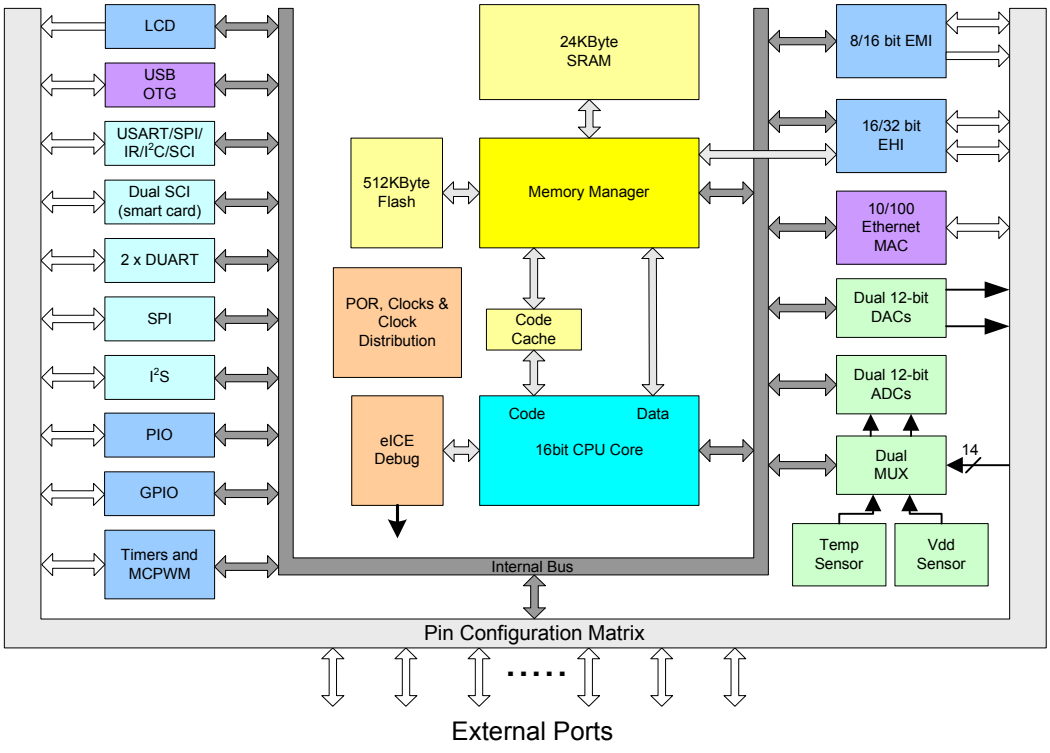
eCOG1X Microcontroller Product Family V1.17

The **eCOG1X** microcontroller family is a range of low-power microcontrollers, based on a 16-bit Harvard architecture with a 24-bit linear code address space (32Mbytes) and 16-bit linear data address space (128Kbytes). The devices are highly configurable, with options including USB 2.0 OTG, 10/100 Ethernet MAC and analogue I/O. Each combination is available with 512Kbytes of FLASH and 24Kbytes of SRAM. Products are available in a variety of QFN and BGA packages with pin counts between 68 and 208 pins. Comprehensive Development and Evaluation Kits are available. All are fully supported by Cyan's free, class-leading, integrated development environment, **CyanIDE**, which includes automatic peripheral configuration and an unrestricted ANSI C Compiler.

- 0 to 70MHz 1.8V core
- 3.3V I/O (some pins 5V tolerant)
- Powerful arithmetic operations
- Barrel Shifter
- Harvard Architecture
- Built in Emulator (eICE)
- Low power operation
- 512Kbytes Flash
- 24Kbytes SRAM
- Memory Management Unit
- Power-saving code cache
- Code security feature
- External Host Interface
- External Memory Interface
- Fast Vectored Interrupts
- 2 x DUARTs
- DUSART: SPI / I2C / SCI / IR
- ESPI
- I2S
- Separate Dual SCI
- Dual 7 channel 12-bit ADCs
- Dual 12-bit DACs
- Temperature Sensor
- Supply Voltage Sensor
- Power-On Reset
- USB 2.0 OTG 480Mbit/s
- 10/100 Ethernet MAC
- 4x32 LCD Controller
- 5 Multi Purpose Timers
  - Clock timer
  - 2 x counter / timer
  - 2 x PWM timer
- Capture timer with 6 inputs
- Watchdog Timer
- Long Interval Timer
- 6 x PWM timers for motor control
- Parallel I/O ports
- Up to 120 GPIO pins
- Low power relaxation oscillator
- Operating temperature range: –40°C to +85°C.

eCOG1X block diagram



eCOG1X Device Options

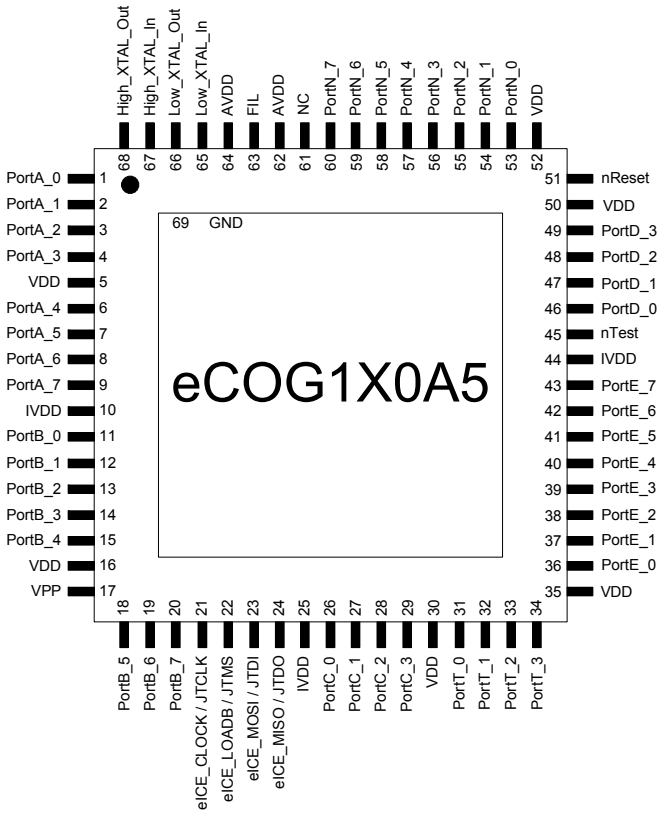
Part number	Flash size	ETH	USB	ADC	DAC	I/Os	Package	CyNet
eCOG1X0A5L	512K					44	68QFN	Disabled
eCOG1X1A5L	512K			4	2	36	68QFN	
eCOG1X4A5L	512K		Y			40	68QFN	
eCOG1X5A5L	512K		Y	4	2	32	68QFN	
eCOG1X8A5L	512K	Y				44	68QFN	
eCOG1X9A5L	512K	Y		4	2	36	68QFN	
eCOG1X10B5L	512K	Y		11	2	60	100QFN	
eCOG1X14B5L	512K	Y	Y	11	2	56	100QFN	
eCOG1X10Z5L	512K	Y		14	2	120	208BGA	
eCOG1X14Z5L	512K	Y	Y	14	2	120	208BGA	
eCOG1X0A5H	512K					44	68QFN	Enabled
eCOG1X1A5H	512K			4	2	36	68QFN	
eCOG1X4A5H	512K		Y			40	68QFN	
eCOG1X5A5H	512K		Y	4	2	32	68QFN	
eCOG1X8A5H	512K	Y				44	68QFN	
eCOG1X9A5H	512K	Y		4	2	36	68QFN	
eCOG1X10B5H	512K	Y		11	2	60	100QFN	
eCOG1X14B5H	512K	Y	Y	11	2	56	100QFN	
eCOG1X10Z5H	512K	Y		14	2	120	208BGA	
eCOG1X14Z5H	512K	Y	Y	14	2	120	208BGA	

Table 1: eCOG1X Device Options

eCOG1X0A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	PortA_0	18	PortB_5	35	VDD	52	VDD
2	PortA_1	19	PortB_6	36	PortE_0	53	PortN_0
3	PortA_2	20	PortB_7	37	PortE_1	54	PortN_1
4	PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	PortN_2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	PortN_3
6	PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	PortN_4
7	PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	PortN_5
8	PortA_6	25	IVDD	42	PortE_6	59	PortN_6
9	PortA_7	26	PortC_0	43	PortE_7	60	PortN_7
10	IVDD	27	PortC_1	44	IVDD	61	NC
11	PortB_0	28	PortC_2	45	nTest	62	AVDD
12	PortB_1	29	PortC_3	46	PortD_0	63	FIL
13	PortB_2	30	VDD	47	PortD_1	64	AVDD
14	PortB_3	31	PortT_0	48	PortD_2	65	Low_XTAL_In
15	PortB_4	32	PortT_1	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	PortT_2	50	VDD	67	High_XTAL_In
17	VPP	34	PortT_3	51	nReset	68	High_XTAL_Out
						69	GND [1]

Table 2: eCOG1X0A5 pin list

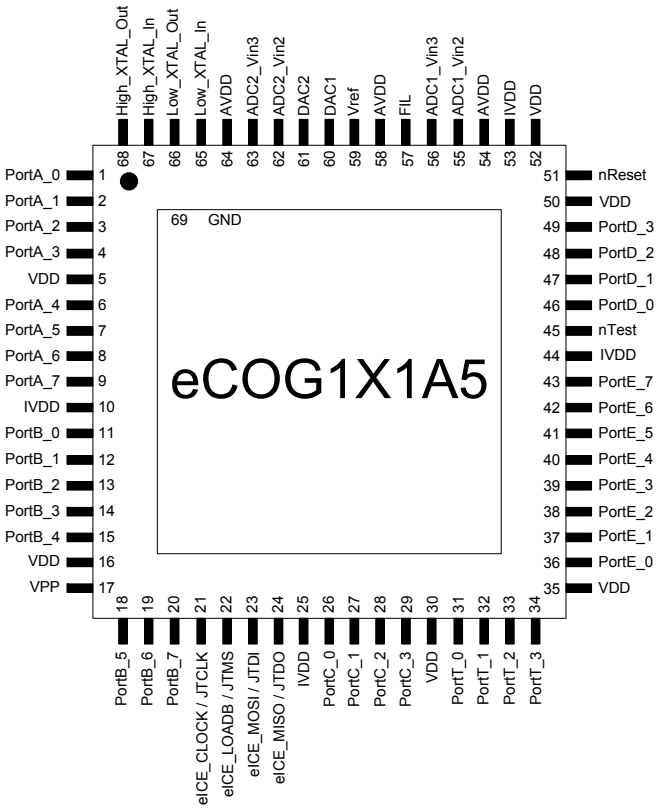
1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

2 Pins labelled NC may be connected internally and must be left open-circuit.

eCOG1X1A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	PortA_0	18	PortB_5	35	VDD	52	VDD
2	PortA_1	19	PortB_6	36	PortE_0	53	IVDD
3	PortA_2	20	PortB_7	37	PortE_1	54	AVDD
4	PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	ADC1_Vin2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	ADC1_Vin3
6	PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	FIL
7	PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	AVDD
8	PortA_6	25	IVDD	42	PortE_6	59	Vref
9	PortA_7	26	PortC_0	43	PortE_7	60	DAC1
10	IVDD	27	PortC_1	44	IVDD	61	DAC2
11	PortB_0	28	PortC_2	45	nTest	62	ADC2_Vin2
12	PortB_1	29	PortC_3	46	PortD_0	63	ADC2_Vin3
13	PortB_2	30	VDD	47	PortD_1	64	AVDD
14	PortB_3	31	PortT_0	48	PortD_2	65	Low_XTAL_In
15	PortB_4	32	PortT_1	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	PortT_2	50	VDD	67	High_XTAL_In
17	VPP	34	PortT_3	51	nReset	68	High_XTAL_Out
						69	GND [1]

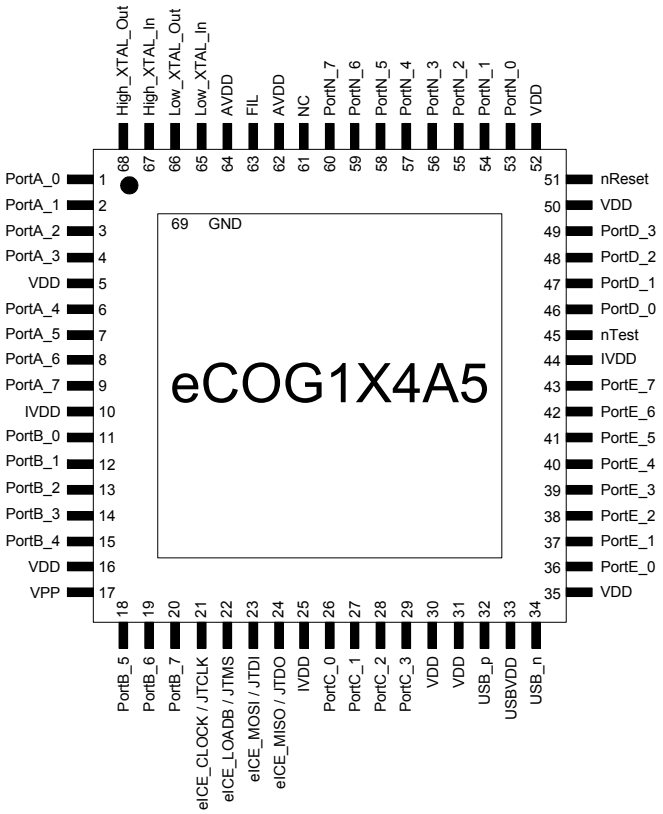
Table 3: eCOG1X1A5 pin list

1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

eCOG1X4A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	PortA_0	18	PortB_5	35	VDD	52	VDD
2	PortA_1	19	PortB_6	36	PortE_0	53	PortN_0
3	PortA_2	20	PortB_7	37	PortE_1	54	PortN_1
4	PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	PortN_2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	PortN_3
6	PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	PortN_4
7	PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	PortN_5
8	PortA_6	25	IVDD	42	PortE_6	59	PortN_6
9	PortA_7	26	PortC_0	43	PortE_7	60	PortN_7
10	IVDD	27	PortC_1	44	IVDD	61	NC
11	PortB_0	28	PortC_2	45	nTest	62	AVDD
12	PortB_1	29	PortC_3	46	PortD_0	63	FIL
13	PortB_2	30	VDD	47	PortD_1	64	AVDD
14	PortB_3	31	VDD	48	PortD_2	65	Low_XTAL_In
15	PortB_4	32	USB_p	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	USBVDD	50	VDD	67	High_XTAL_In
17	VPP	34	USB_n	51	nReset	68	High_XTAL_Out
						69	GND [1]

Table 4: eCOG1X4A5 pin list

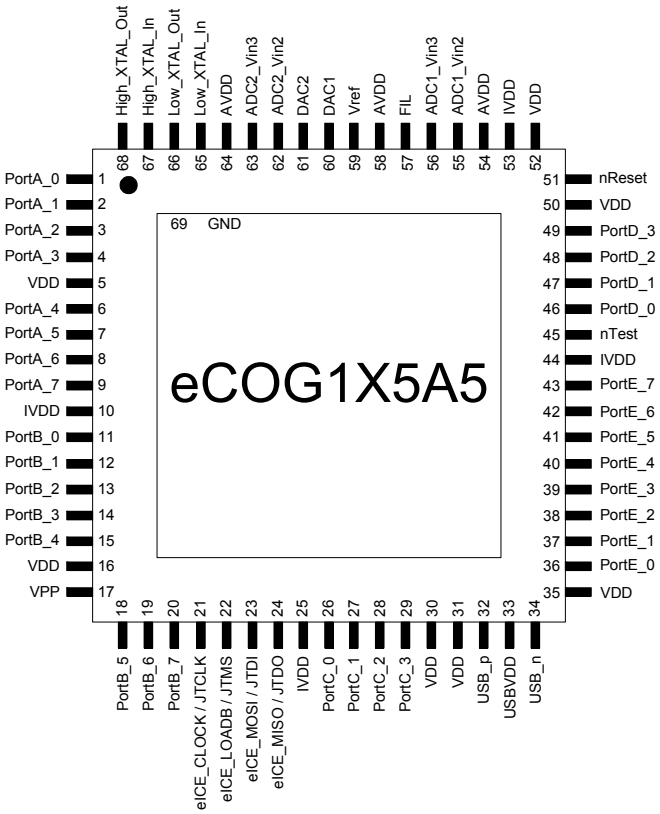
1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

2 Pins labelled NC may be connected internally and must be left open-circuit.

eCOG1X5A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	PortA_0	18	PortB_5	35	VDD	52	VDD
2	PortA_1	19	PortB_6	36	PortE_0	53	IVDD
3	PortA_2	20	PortB_7	37	PortE_1	54	AVDD
4	PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	ADC1_Vin2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	ADC1_Vin3
6	PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	FIL
7	PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	AVDD
8	PortA_6	25	IVDD	42	PortE_6	59	Vref
9	PortA_7	26	PortC_0	43	PortE_7	60	DAC1
10	IVDD	27	PortC_1	44	IVDD	61	DAC2
11	PortB_0	28	PortC_2	45	nTest	62	ADC2_Vin2
12	PortB_1	29	PortC_3	46	PortD_0	63	ADC2_Vin3
13	PortB_2	30	VDD	47	PortD_1	64	AVDD
14	PortB_3	31	VDD	48	PortD_2	65	Low_XTAL_In
15	PortB_4	32	USB_p	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	USBVDD	50	VDD	67	High_XTAL_In
17	VPP	34	USB_n	51	nReset	68	High_XTAL_Out
						69	GND [1]

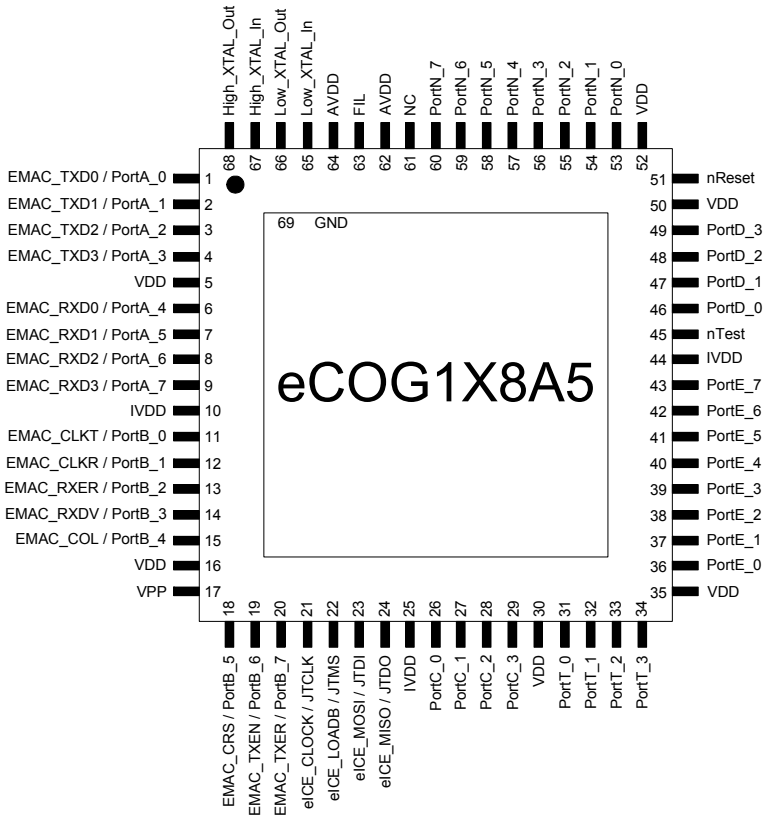
Table 5: eCOG1X5A5 pin list

1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

eCOG1X8A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	EMAC_TXD0 / PortA_0	18	EMAC_CRS / PortB_5	35	VDD	52	VDD
2	EMAC_TXD1 / PortA_1	19	EMAC_TXEN / PortB_6	36	PortE_0	53	PortN_0
3	EMAC_TXD2 / PortA_2	20	EMAC_TXER / PortB_7	37	PortE_1	54	PortN_1
4	EMAC_TXD3 / PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	PortN_2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	PortN_3
6	EMAC_RXD0 / PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	PortN_4
7	EMAC_RXD1 / PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	PortN_5
8	EMAC_RXD2 / PortA_6	25	IVDD	42	PortE_6	59	PortN_6
9	EMAC_RXD3 / PortA_7	26	PortC_0	43	PortE_7	60	PortN_7
10	IVDD	27	PortC_1	44	IVDD	61	NC
11	EMAC_CLKT / PortB_0	28	PortC_2	45	nTest	62	AVDD
12	EMAC_CLKR / PortB_1	29	PortC_3	46	PortD_0	63	FIL
13	EMAC_RXER / PortB_2	30	VDD	47	PortD_1	64	AVDD
14	EMAC_RXDV / PortB_3	31	PortT_0	48	PortD_2	65	Low_XTAL_In
15	EMAC_COL / PortB_4	32	PortT_1	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	PortT_2	50	VDD	67	High_XTAL_In
17	VPP	34	PortT_3	51	nReset	68	High_XTAL_Out
						69	GND [1]

Table 6: eCOG1X8A5 pin list

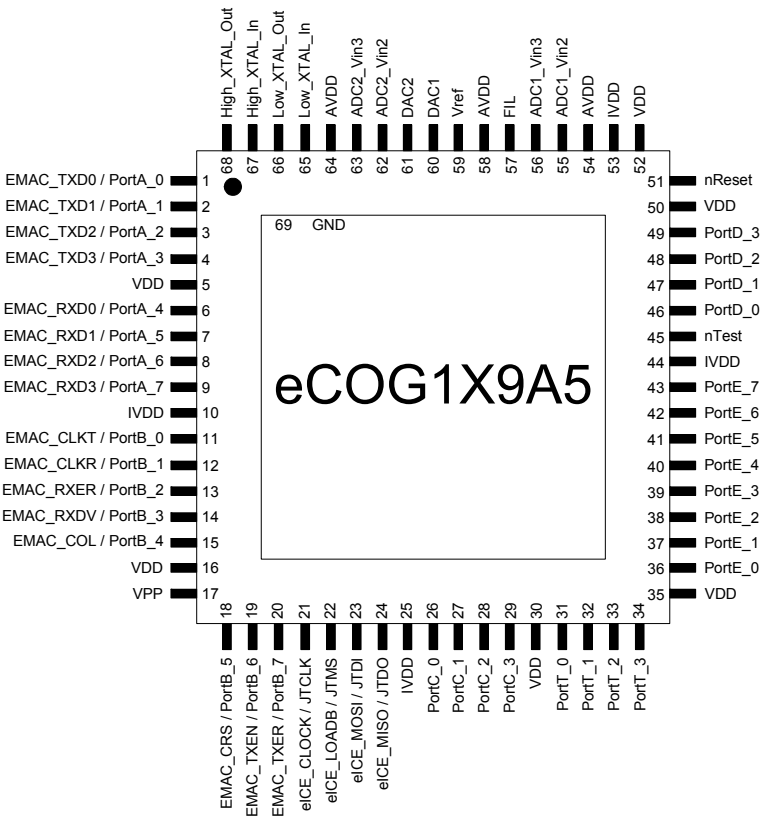
1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

2 Pins labelled NC may be connected internally and must be left open-circuit.

eCOG1X9A5

Pin Diagram

68 pin QFN - A package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	EMAC_TXD0 / PortA_0	18	EMAC_CRS / PortB_5	35	VDD	52	VDD
2	EMAC_TXD1 / PortA_1	19	EMAC_TXEN / PortB_6	36	PortE_0	53	IVDD
3	EMAC_TXD2 / PortA_2	20	EMAC_TXER / PortB_7	37	PortE_1	54	AVDD
4	EMAC_TXD3 / PortA_3	21	eICE_CLOCK / JTCLK	38	PortE_2	55	ADC1_Vin2
5	VDD	22	eICE_LOADB / JTMS	39	PortE_3	56	ADC1_Vin3
6	EMAC_RXD0 / PortA_4	23	eICE_MOSI / JTDI	40	PortE_4	57	FIL
7	EMAC_RXD1 / PortA_5	24	eICE_MISO / JTDO	41	PortE_5	58	AVDD
8	EMAC_RXD2 / PortA_6	25	IVDD	42	PortE_6	59	Vref
9	EMAC_RXD3 / PortA_7	26	PortC_0	43	PortE_7	60	DAC1
10	IVDD	27	PortC_1	44	IVDD	61	DAC2
11	EMAC_CLKT / PortB_0	28	PortC_2	45	nTest	62	ADC2_Vin2
12	EMAC_CLKR / PortB_1	29	PortC_3	46	PortD_0	63	ADC2_Vin3
13	EMAC_RXER / PortB_2	30	VDD	47	PortD_1	64	AVDD
14	EMAC_RXDV / PortB_3	31	PortT_0	48	PortD_2	65	Low_XTAL_In
15	EMAC_COL / PortB_4	32	PortT_1	49	PortD_3	66	Low_XTAL_Out
16	VDD	33	PortT_2	50	VDD	67	High_XTAL_In
17	VPP	34	PortT_3	51	nReset	68	High_XTAL_Out
						69	GND [1]

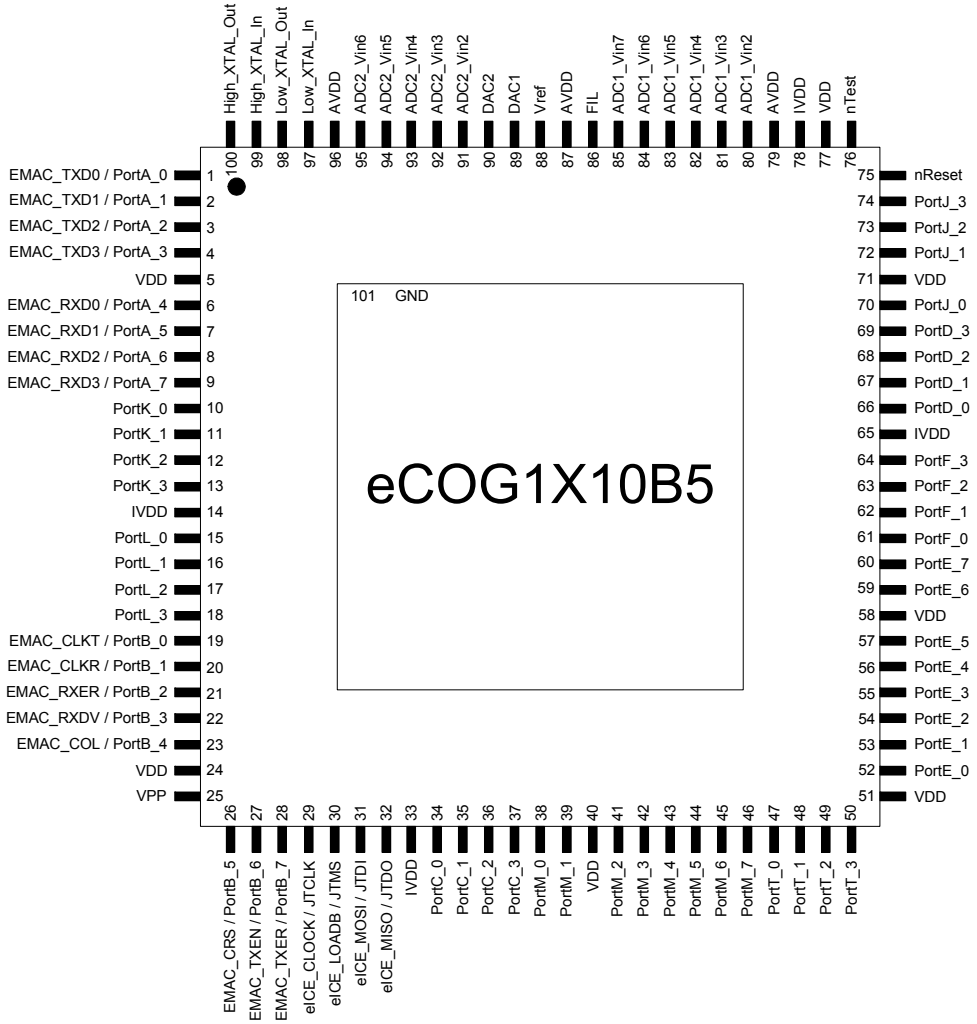
Table 7: eCOG1X9A5 pin list

1 The 68QFN package has a large central body contact which forms the GND pad. This is listed as pin 69.

eCOG1X10B5

Pin Diagram

100 pin QFN - B package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	EMAC_TXD0 / PortA_0	26	EMAC_CRS / PortB_5	51	VDD	76	nTest
2	EMAC_TXD1 / PortA_1	27	EMAC_TXEN / PortB_6	52	PortE_0	77	VDD
3	EMAC_TXD2 / PortA_2	28	EMAC_TXER / PortB_7	53	PortE_1	78	IVDD
4	EMAC_TXD3 / PortA_3	29	eICE_CLOCK / JTCLK	54	PortE_2	79	AVDD
5	VDD	30	eICE_LOADB / JTMS	55	PortE_3	80	ADC1_Vin2
6	EMAC_RXD0 / PortA_4	31	eICE_MOSI / JTDI	56	PortE_4	81	ADC1_Vin3
7	EMAC_RXD1 / PortA_5	32	eICE_MISO / JTDO	57	PortE_5	82	ADC1_Vin4
8	EMAC_RXD2 / PortA_6	33	IVDD	58	VDD	83	ADC1_Vin5
9	EMAC_RXD3 / PortA_7	34	PortC_0	59	PortE_6	84	ADC1_Vin6
10	PortK_0	35	PortC_1	60	PortE_7	85	ADC1_Vin7
11	PortK_1	36	PortC_2	61	PortF_0	86	FIL
12	PortK_2	37	PortC_3	62	PortF_1	87	AVDD
13	PortK_3	38	PortM_0	63	PortF_2	88	Vref
14	IVDD	39	PortM_1	64	PortF_3	89	DAC1
15	PortL_0	40	VDD	65	IVDD	90	DAC2
16	PortL_1	41	PortM_2	66	PortD_0	91	ADC2_Vin2
17	PortL_2	42	PortM_3	67	PortD_1	92	ADC2_Vin3
18	PortL_3	43	PortM_4	68	PortD_2	93	ADC2_Vin4
19	EMAC_CLKT / PortB_0	44	PortM_5	69	PortD_3	94	ADC2_Vin5
20	EMAC_CLKR / PortB_1	45	PortM_6	70	PortJ_0	95	ADC2_Vin6
21	EMAC_RXER / PortB_2	46	PortM_7	71	VDD	96	AVDD
22	EMAC_RXDV / PortB_3	47	PortT_0	72	PortJ_1	97	Low_XTAL_In
23	EMAC_COL / PortB_4	48	PortT_1	73	PortJ_2	98	Low_XTAL_Out
24	VDD	49	PortT_2	74	PortJ_3	99	High_XTAL_In
25	VPP	50	PortT_3	75	nReset	100	High_XTAL_Out
						101	GND [1]

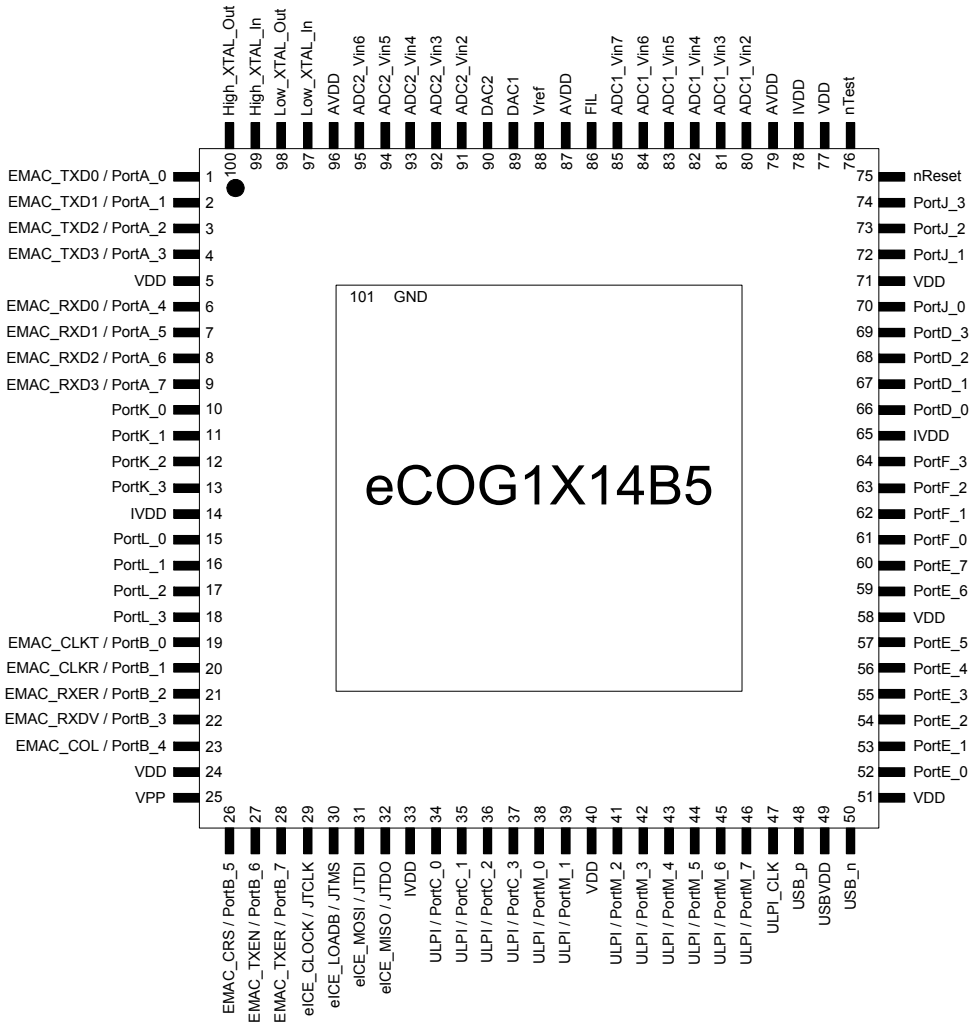
Table 8: eCOG1X10B5 pin list

1 The 100QFN package has a large central body contact which forms the GND pad. This is listed as pin 101.

eCOG1X14B5

Pin Diagram

100 pin QFN - B package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	EMAC_TXD0 / PortA_0	26	EMAC_CRS / PortB_5	51	VDD	76	nTest
2	EMAC_TXD1 / PortA_1	27	EMAC_TXEN / PortB_6	52	PortE_0	77	VDD
3	EMAC_TXD2 / PortA_2	28	EMAC_TXER / PortB_7	53	PortE_1	78	IVDD
4	EMAC_TXD3 / PortA_3	29	eICE_CLOCK / JTCLK	54	PortE_2	79	AVDD
5	VDD	30	eICE_LOADB / JTMS	55	PortE_3	80	ADC1_Vin2
6	EMAC_RXD0 / PortA_4	31	eICE_MOSI / JTDI	56	PortE_4	81	ADC1_Vin3
7	EMAC_RXD1 / PortA_5	32	eICE_MISO / JTDO	57	PortE_5	82	ADC1_Vin4
8	EMAC_RXD2 / PortA_6	33	IVDD	58	VDD	83	ADC1_Vin5
9	EMAC_RXD3 / PortA_7	34	ULPI_RST / PortC_0	59	PortE_6	84	ADC1_Vin6
10	PortK_0	35	ULPI_DIR / PortC_1	60	PortE_7	85	ADC1_Vin7
11	PortK_1	36	ULPI_NXT / PortC_2	61	PortF_0	86	FIL
12	PortK_2	37	ULPI_STOP / PortC_3	62	PortF_1	87	AVDD
13	PortK_3	38	ULPI_DATA0 / PortM_0	63	PortF_2	88	Vref
14	IVDD	39	ULPI_DATA1 / PortM_1	64	PortF_3	89	DAC1
15	PortL_0	40	VDD	65	IVDD	90	DAC2
16	PortL_1	41	ULPI_DATA2 / PortM_2	66	PortD_0	91	ADC2_Vin2
17	PortL_2	42	ULPI_DATA3 / PortM_3	67	PortD_1	92	ADC2_Vin3
18	PortL_3	43	ULPI_DATA4 / PortM_4	68	PortD_2	93	ADC2_Vin4
19	EMAC_CLKT / PortB_0	44	ULPI_DATA5 / PortM_5	69	PortD_3	94	ADC2_Vin5
20	EMAC_CLKR / PortB_1	45	ULPI_DATA6 / PortM_6	70	PortJ_0	95	ADC2_Vin6
21	EMAC_RXER / PortB_2	46	ULPI_DATA7 / PortM_7	71	VDD	96	AVDD
22	EMAC_RXDV / PortB_3	47	ULPI_CLK	72	PortJ_1	97	Low_XTAL_In
23	EMAC_COL / PortB_4	48	USB_p	73	PortJ_2	98	Low_XTAL_Out
24	VDD	49	USBVDD	74	PortJ_3	99	High_XTAL_In
25	VPP	50	USB_n	75	nReset	100	High_XTAL_Out
						101	GND [1]

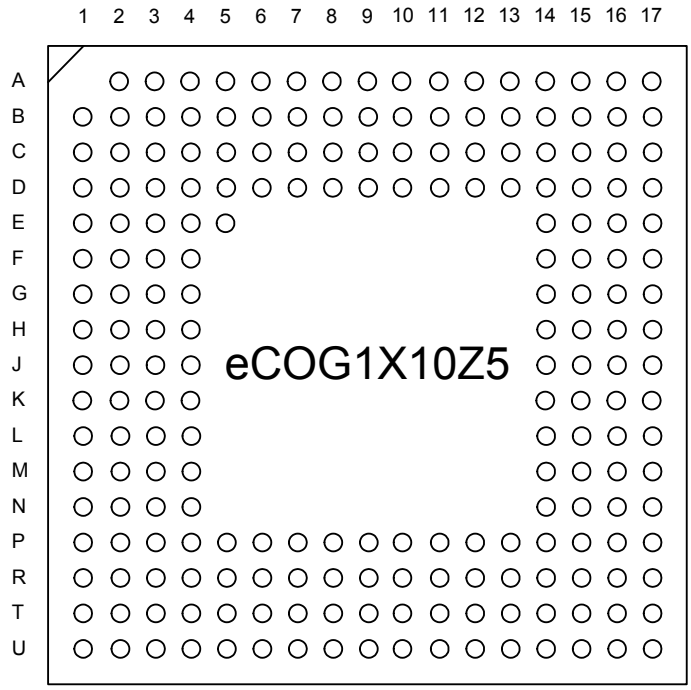
Table 9: eCOG1X14B5 pin list

1 The 100QFN package has a large central body contact which forms the GND pad. This is listed as pin 101.

eCOG1X10Z5

Pin Diagram

208 pin BGA - Z package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
		B1	High_XTAL_Out	C1	NC [1]	D1	EMAC_RXD0 / A_4
A2	Low_XTAL_Out	B2	AGND	C2	EMAC_TXD1 / A_1	D2	EMAC_TXD3 / A_3
A3	ADC2_Vin6	B3	Low_XTAL_In	C3	High_XTAL_In	D3	EMAC_TXD0 / A_0
A4	ADC2_Vin4	B4	ADC2_Vin5	C4	AVDD	D4	GND
A5	ADC2_Vin1	B5	ADC2_Vin2	C5	ADC2_Vin7	D5	GND
A6	DAC1	B6	DAC2	C6	ADC2_Vin3	D6	GND
A7	AGND	B7	Vref	C7	NC [1]	D7	VDD
A8	ADC1_Vin7	B8	FIL	C8	AVDD	D8	GND
A9	ADC1_Vin6	B9	ADC1_Vin5	C9	ADC1_Vin2	D9	GND
A10	ADC1_Vin4	B10	ADC1_Vin3	C10	AVDD	D10	IVDD
A11	ADC1_Vin1	B11	AVDD	C11	Rext	D11	VDD
A12	NC [1]	B12	NC [1]	C12	PortN_6	D12	VDD
A13	PortN_7	B13	PortN_5	C13	PortN_3	D13	GND
A14	PortN_4	B14	PortN_2	C14	nTest	D14	GND
A15	PortN_1	B15	PortN_0	C15	nReset_out	D15	PortJ_3
A16	nReset_in	B16	PortJ_2	C16	PortJ_1	D16	PortD_2
A17	PortJ_0	B17	PortD_3	C17	PortD_1	D17	PortI_5

Table 10: eCOG1X10Z5 pin list

Pin	Description	Pin	Description	Pin	Description	Pin	Description
E1	EMAC_RXD2 / A_6	F1	PortK_1	G1	PortK_3	H1	PortP_2
E2	EMAC_RXD1 / A_5	F2	PortK_0	G2	PortK_2	H2	PortP_1
E3	EMAC_TXD2 / A_2	F3	EMAC_RXD3 / A_7	G3	PortP_0	H3	PortP_3
E4	GND	F4	GND	G4	VDD	H4	GND
E5	GND						
E14	GND	F14	IVDD	G14	VDD	H14	GND
E15	PortD_0	F15	PortI_6	G15	PortI_3	H15	PortH_1
E16	PortI_7	F16	PortI_4	G16	PortI_1	H16	PortH_6
E17	PortI_2	F17	PortI_0	G17	PortH_7	H17	PortH_5
J1	PortP_6	K1	PortQ_1	L1	PortQ_2	M1	PortQ_4
J2	PortP_5	K2	PortP_7	L2	PortQ_3	M2	PortQ_6
J3	PortP_4	K3	PortQ_0	L3	PortQ_5	M3	EMAC_CLKR / B_1
J4	GND	K4	IVDD	L4	GND	M4	GND
J14	GND	K14	IVDD	L14	GND	M14	GND
J15	PortH_0	K15	PortG_1	L15	PortF_3	M15	PortE_7
J16	PortH_4	K16	PortG_3	L16	PortG_0	M16	PortF_2
J17	PortH_3	K17	PortH_2	L17	PortG_2	M17	PortF_1
N1	PortQ_7						
N2	PortL_2						
N3	VPP						
N4	GND						
N14	VDD						
N15	PortE_2						
N16	PortE_6						
N17	PortF_0						
P1	PortL_0	R1	PortL_1	T1	PortL_3	U1	EMAC_TXEN / B_6
P2	EMAC_CLKT / B_0	R2	EMAC_RXER / B_2	T2	EMAC_CRS / B_5	U2	eICE_LOADB / JTMS
P3	EMAC_RXDV / B_3	R3	EMAC_COL / B_4	T3	eICE_CLOCK / JTCLK	U3	eICE_MOSI / JTDI
P4	GND	R4	EMAC_TXER / B_7	T4	PortR_0	U4	PortR_2
P5	GND	R5	eICE_MISO / JTDO	T5	PortR_1	U5	PortR_4
P6	VDD	R6	PortR_3	T6	PortR_5	U6	PortR_6
P7	GND	R7	PortR_7	T7	PortS_0	U7	PortS_1
P8	IVDD	R8	PortS_2	T8	PortS_3	U8	IVDD
P9	VDD	R9	PortS_6	T9	PortS_5	U9	PortS_4
P10	VDD	R10	PortM_1	T10	PortC_0	U10	PortS_7
P11	VDD	R11	PortT_0	T11	PortC_2	U11	PortC_1
P12	VDD	R12	PortT_1	T12	PortM_2	U12	PortC_3
P13	GND	R13	NC [1]	T13	PortM_3	U13	PortM_0
P14	GND	R14	NC [1]	T14	PortM_6	U14	PortM_4
P15	PortT_2	R15	USBVDD	T15	PortM_7	U15	PortM_5
P16	PortE_4	R16	PortE_0	T16	GND	U16	PortT_3
P17	PortE_5	R17	PortE_3	T17	PortE_1	U17	GND

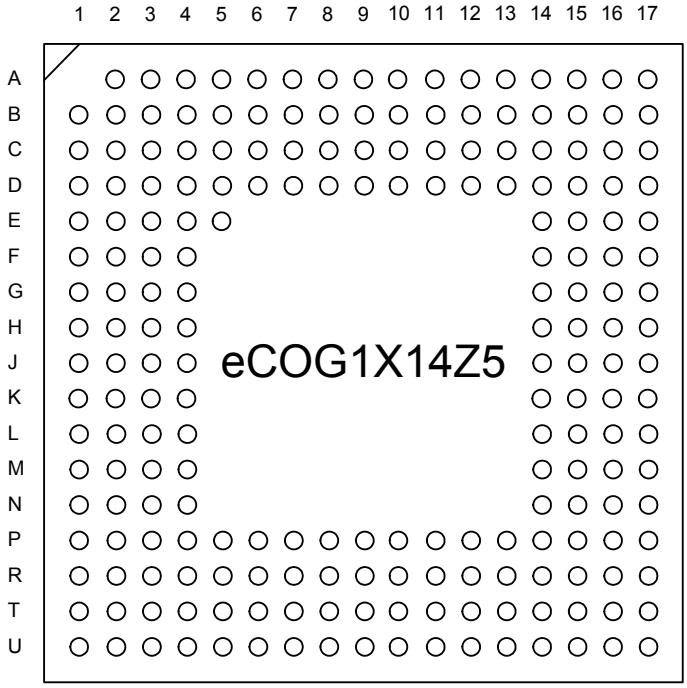
Table 10: eCOG1X10Z5 pin list

1 Pins labelled NC may be connected internally and must be left open-circuit.

eCOG1X14Z5

Pin Diagram

208 pin BGA - Z package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
		B1	High_XTAL_Out	C1	NC [1]	D1	EMAC_RXD0 / A_4
A2	Low_XTAL_Out	B2	AGND	C2	EMAC_TXD1 / A_1	D2	EMAC_TXD3 / A_3
A3	ADC2_Vin6	B3	Low_XTAL_In	C3	High_XTAL_In	D3	EMAC_TXD0 / A_0
A4	ADC2_Vin4	B4	ADC2_Vin5	C4	AVDD	D4	GND
A5	ADC2_Vin1	B5	ADC2_Vin2	C5	ADC2_Vin7	D5	GND
A6	DAC1	B6	DAC2	C6	ADC2_Vin3	D6	GND
A7	AGND	B7	Vref	C7	NC [1]	D7	VDD
A8	ADC1_Vin7	B8	FIL	C8	AVDD	D8	GND
A9	ADC1_Vin6	B9	ADC1_Vin5	C9	ADC1_Vin2	D9	GND
A10	ADC1_Vin4	B10	ADC1_Vin3	C10	AVDD	D10	IVDD
A11	ADC1_Vin1	B11	AVDD	C11	Rext	D11	VDD
A12	NC [1]	B12	NC [1]	C12	PortN_6	D12	VDD
A13	PortN_7	B13	PortN_5	C13	PortN_3	D13	GND
A14	PortN_4	B14	PortN_2	C14	nTest	D14	GND
A15	PortN_1	B15	PortN_0	C15	nReset_out	D15	PortJ_3
A16	nReset_in	B16	PortJ_2	C16	PortJ_1	D16	PortD_2
A17	PortJ_0	B17	PortD_3	C17	PortD_1	D17	PortI_5

Table 11: eCOG1X14Z5 pin list

Pin	Description	Pin	Description	Pin	Description	Pin	Description
E1	EMAC_RXD2 / A_6	F1	PortK_1	G1	PortK_3	H1	PortP_2
E2	EMAC_RXD1 / A_5	F2	PortK_0	G2	PortK_2	H2	PortP_1
E3	EMAC_TXD2 / A_2	F3	EMAC_RXD3 / A_7	G3	PortP_0	H3	PortP_3
E4	GND	F4	GND	G4	VDD	H4	GND
E5	GND						
E14	GND	F14	IVDD	G14	VDD	H14	GND
E15	PortD_0	F15	PortI_6	G15	PortI_3	H15	PortH_1
E16	PortI_7	F16	PortI_4	G16	PortI_1	H16	PortH_6
E17	PortI_2	F17	PortI_0	G17	PortH_7	H17	PortH_5
J1	PortP_6	K1	PortQ_1	L1	PortQ_2	M1	PortQ_4
J2	PortP_5	K2	PortP_7	L2	PortQ_3	M2	PortQ_6
J3	PortP_4	K3	PortQ_0	L3	PortQ_5	M3	EMAC_CLKR / B_1
J4	GND	K4	IVDD	L4	GND	M4	GND
J14	GND	K14	IVDD	L14	GND	M14	GND
J15	PortH_0	K15	PortG_1	L15	PortF_3	M15	PortE_7
J16	PortH_4	K16	PortG_3	L16	PortG_0	M16	PortF_2
J17	PortH_3	K17	PortH_2	L17	PortG_2	M17	PortF_1
N1	PortQ_7						
N2	PortL_2						
N3	VPP						
N4	GND						
N14	VDD						
N15	PortE_2						
N16	PortE_6						
N17	PortF_0						
P1	PortL_0	R1	PortL_1	T1	PortL_3	U1	EMAC_TXEN / B_6
P2	EMAC_CLKT / B_0	R2	EMAC_RXER / B_2	T2	EMAC_CRS / B_5	U2	eICE_LOADB / JTMS
P3	EMAC_RXDV / B_3	R3	EMAC_COL / B_4	T3	eICE_CLOCK / JTCLK	U3	eICE_MOSI / JTDI
P4	GND	R4	EMAC_TXER / B_7	T4	PortR_0	U4	PortR_2
P5	GND	R5	eICE_MISO / JTDO	T5	PortR_1	U5	PortR_4
P6	VDD	R6	PortR_3	T6	PortR_5	U6	PortR_6
P7	GND	R7	PortR_7	T7	PortS_0	U7	PortS_1
P8	IVDD	R8	PortS_2	T8	PortS_3	U8	IVDD
P9	VDD	R9	PortS_6	T9	PortS_5	U9	PortS_4
P10	VDD	R10	ULPI_DATA1 / M_1	T10	ULPI_RST / C_0	U10	PortS_7
P11	VDD	R11	PortT_0	T11	ULPI_NXT / C_2	U11	ULPI_DIR / C_1
P12	VDD	R12	PortT_1	T12	ULPI_DATA2 / M_2	U12	ULPI_STOP / C_3
P13	GND	R13	USB_n	T13	ULPI_DATA3 / M_3	U13	ULPI_DATA0 / M_0
P14	GND	R14	USB_p	T14	ULPI_DATA6 / M_6	U14	ULPI_DATA4 / M_4
P15	PortT_2	R15	USBVDD	T15	ULPI_DATA7 / M_7	U15	ULPI_DATA5 / M_5
P16	PortE_4	R16	PortE_0	T16	GND	U16	PortT_3
P17	PortE_5	R17	PortE_3	T17	PortE_1	U17	ULPI_CLK

Table 11: eCOG1X14Z5 pin list

1 Pins labelled NC may be connected internally and must be left open-circuit.

Pin Functions

Label	Function	I/O
ADC1_Vin1-7	ADC1 analogue inputs	I
ADC2_Vin1-7	ADC2 analogue inputs	I
AGND	Analogue GND	PWR
AVDD	Analogue power supply 1.8V	PWR
DAC1	DAC1 analogue output	O
DAC2	DAC2 analogue output	O
eICE_CLOCK	eICE clock input	I
eICE_LOADB [1]	eICE LoadB handshake signal	I/O
eICE_MISO	eICE Master In Slave Out	O
eICE_MOSI	eICE Master Out Slave In	I
EMAC_TXD0-3	Ethernet MAC Transmit Data	O
EMAC_RXD0-3	Ethernet MAC Receive Data	I
EMAC_CLKT	Ethernet MAC Transmit Clock	I
EMAC_CLKR	Ethernet MAC Receive Clock	I
EMAC_RXER	Ethernet MAC Receive Error	I
EMAC_RXDV	Ethernet MAC Receive Data Valid	I
EMAC_COL	Ethernet MAC Collision Detect	I
EMAC_CRS	Ethernet MAC Carrier Sense	I
EMAC_TXEN	Ethernet MAC Transmit Enable	O
EMAC_TXER	Ethernet MAC Transmit Error	O
FIL [2]	Low PLL external filter	
GND	Digital GND	PWR
High_XTAL_In [3]	High frequency crystal oscillator input	I
High_XTAL_Out [3]	High frequency crystal oscillator output	O
IVDD	Internal core logic power supply 1.8V	PWR
JTCLK	JTAG Test Clock input	I
JTDI	JTAG Test Data Input	I
JTDO	JTAG Test Data Output	O
JTMS	JTAG Test Mode Select	I
Low_XTAL_In [4]	Low frequency crystal oscillator input	I
Low_XTAL_Out [4]	Low frequency crystal oscillator output	O
NC	No Connect	
nReset [5]	Power-on reset (bidirectional, open-drain)	I/O
nReset_In [6]	Power-on reset input	I
nReset_Out [6]	Power-on reset sense output	O
nTest [7]	Test mode select input	I
PortA_0-7	Port A pins 0-7	I/O
PortB_0-7	Port B pins 0-7	I/O
PortC_0-3	Port C pins 0-3	I/O
PortD_0-3	Port D pins 0-3	I/O
PortE_0-7	Port E pins 0-7	I/O
PortF_0-3	Port F pins 0-3	I/O
PortG_0-3	Port G pins 0-3	I/O
PortH_0-7	Port H pins 0-7	I/O
PortI_0-7	Port I pins 0-7	I/O
PortJ_0-3	Port J pins 0-3	I/O
PortK_0-3	Port K pins 0-3	I/O
PortL_0-3	Port L pins 0-3	I/O
PortM_0-7	Port M pins 0-7	I/O
PortN_07	Port N pins 0-7	I/O
PortP_0-7	Port P pins 0-7	I/O
PortQ_0-7	Port Q pins 0-7	I/O
PortR_0-7	Port R pins 0-7	I/O
PortS_0-7	Port S pins 0-7	I/O
PortT_0-3	Port T pins 0-3	I/O

Table 12: Pin functions

Label	Function	I/O
Rext [8]	External resistor to set relaxation oscillator frequency	
ULPI_CLK [9]	USB ULPI Clock input	I
ULPI_DATA0-7	USB ULPI Data bus	I/O
USB_n	USB data negative	I/O
USB_p	USB data positive	I/O
USBVDD	USB power supply 3.3V	PWR
ULPI_STOP	USB ULPI Stop	O
ULPI_NXT	USB ULPI Next	I
ULPI_DIR	USB ULPI Direction	I
ULPI_RST	USB ULPI Reset	
VDD	Digital power supply 3.3V	PWR
VPP [10]	Flash memory high speed programming power supply	PWR
Vref [11]	Analogue reference voltage	

Table 12: Pin functions

1 The eICE_LOADB pin has an internal pull-up resistor connected to VDD with a value of 20kΩ-100kΩ. This is sufficient for normal operation when the eICE debug port is not in use or disconnected. When the eICE port is used for debugging, a 4.7kΩ pull-up resistor is recommended to reduce the rise time on this open-drain signal and increase the speed of eICE data transfers. If the system is used with an external eICE programming adaptor, then the external adaptor has the 4.7kΩ pull-up resistor fitted, and the target system does not need any additional pull-up resistor connected to this signal.
It is also recommended that the eICE input signals (eICE_CLK, eICE_MOSI) are connected to GND via 100kΩ pull-down resistors as a precaution against noise when the eICE port is not in use or disconnected.

2 The FIL pin requires external low pass filter components for the low frequency PLL to be fitted. The filter consists of a 2.2nF capacitor from FIL to GND, in parallel with a 68nF capacitor and an 8.2kΩ resistor in series.

3 The external quartz crystal used with the 8MHz high reference oscillator requires two load capacitors. The maximum load capacitance value for the high reference oscillator is 32pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 22pF. If an external clock source is used instead of the 8MHz quartz crystal oscillator, then High_XTAL_Out is not connected and the external clock signal is connected to High_XTAL_In. If the high reference clock is not required, then High_XTAL_Out is not connected and High_XTAL_In is connected to AGND via a 10kΩ resistor.

4 The external quartz crystal used with the 32.768kHz low reference oscillator requires two load capacitors. The maximum load capacitance value for the low reference oscillator is 25pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 10pF. If an external clock source is used instead of the 32.768kHz quartz crystal oscillator, then Low_XTAL_Out is not connected and the external clock signal is connected to Low_XTAL_In. If the low reference clock is not required, then Low_XTAL_Out is not connected and Low_XTAL_In is connected to AGND via a 10kΩ resistor.

5 On smaller package variants (68QFN, 100QFN), the nReset pin is bidirectional. It is driven low internally as an open-drain output by the on-chip power-on reset supply voltage sense circuit, and is also connected as an input to the device from the pin. This allows the use of an external reset circuit if required. The nReset input has a Schmitt trigger input circuit and an internal pull-up resistor.

6 On larger package variants (208BGA), the nReset_Out and nReset_In pins are not connected internally. This allows the use of an external reset circuit. An active low power-on reset signal must be connected to nReset_In for correct operation of the device, from the internal reset circuit or an external power-on reset circuit. To use the internal power-on reset circuit, connect nReset_Out to nReset_In, either directly or via external logic for any additional external reset source such as a pushbutton switch. The nReset_In input has a Schmitt trigger input circuit and an internal pull-up resistor. The nReset_Out output is open-drain with an internal pull-up resistor, and can be used in a wired-OR connection with an external power-on reset if the external device also has an active-low open-drain output.

7 The nTest pin is not used in normal applications and should be connected to VDD, directly or via a pull-up resistor.

8 The Rext pin for the external resistor to set the frequency of the relaxation oscillator is available only on the 208BGA package. For all devices in the smaller 68QFN and 100QFN packages, the relaxation oscillator runs at the frequency corresponding to an open circuit at Rext with the external resistor not fitted.

9 The ULPI_CLK input should be pulled low or tied to GND if the ULPI high-speed USB connection is not used.

10 The VPP pin is used with a higher voltage supply to support faster programming of the internal flash memory via JTAG. If this function is not required, then the VPP pin should be connected to GND to minimise power consumption in normal operation. If this function is required, then connect VPP to GND via a pull-down resistor or jumper link so that the fast programming supply can be connected.

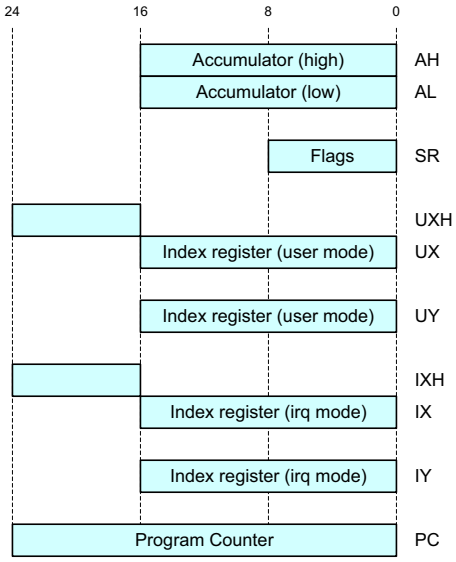
11 Applications which use the analogue inputs or outputs with the internal reference voltage must have external decoupling capacitors connected to the Vref pin. The recommended decoupling on this pin is a 100nF ceramic capacitor in parallel with a 4.7µF tantalum or aluminium electrolytic capacitor.

Description

This section gives a brief description of the main features of the eCOG1X device family. For a complete description, see the eCOG1X User Manual.

CPU

The eCOG1X has an advanced high speed, low power CPU with an instruction set targeted at high level languages, in particular C. The CPU operates at internal clock frequencies up to 70MHz. Full details of the instruction set are contained in the eCOG1 Macro Assembler User Manual.



The main features of the processor are:

- 16-bit RISC.
- Sleep mode to support low power applications.
- Harvard architecture (separate internal address and data buses for faster memory accesses).
- 16-bit data space addressing range (64K by 16 bits).
- 24-bit code space addressing range (16M by 16 bits).
- Support for debugging and multiple breakpoints.
- Single level of interrupt.
- Powerful mathematical functions including:
  - 16 by 16 signed and unsigned multiply.
  - 32 by 16 unsigned divide.
  - Single cycle barrel shifter.

Instruction Set

The eCOG1 instruction set includes 42 instructions with 6 addressing modes. Most instructions operate on 16-bit word data values, while the LD and ST instructions also have variants for handling byte data values.

Address mode	Syntax	Data address
Immediate	#arg	arg
Direct	@arg	Contents of address (arg)
Indexed X	@(arg,x)	Contents of address (arg + X reg)
Indexed Y	@(arg,y)	Contents of address (arg + Y reg)

Table 13: Data addressing modes

Address mode	Syntax	Branch address (new PC value)
PC relative	arg	PC + arg
X relative	arg,x	XH:X + arg
Direct	@arg	XH:contents of address (arg)
Indexed Y	@(arg,y)	XH:contents of address (arg + Y reg)

Table 14: Branch addressing modes

Operating Modes

There are three independent aspects of the processor operating modes.

Processor State	awake or asleep
Processor Mode	interrupt or user mode
Program State	running or stopped (used when debugging)

Processor State

When the processor is awake, it fetches and executes instructions normally. When the processor is asleep, no instructions are executed. The *SLEEP* instruction changes from the awake to the asleep state, and selected peripherals are stopped automatically to reduce power consumption. External I/O activity triggers a wake up event, and selected peripherals are started automatically.

Processor Mode

Interrupts from internal or external peripherals are enabled in user mode. When an interrupt is serviced, the processor changes from user to interrupt mode. No further interrupts are serviced until the processor completes the current interrupt service routine and returns with an *RTI* instruction.

In user mode, the processor uses the UX and UY registers. In interrupt mode, it uses the IX and IY registers. It is possible to switch between user and interrupt modes in software by changing the state of the interrupt mode bit in the flags register.

Program State

When executing an application, the program is in the normal running state. When debug mode is enabled via the eICE debug port, the program can change to the stopped state on the following events.

- A *BRK* instruction is executed.
- The PC register becomes equal to one of the code address breakpoint registers.
- A data space access matches the configuration in the data breakpoint registers.
- An eICE *stop* command is received via the debug port.

Once the program is stopped, a *run* command received via the eICE debug port restarts execution.

Instruction Cache

The eCOG1X has an on-chip instruction cache, implemented using fast SRAM. This fast memory area can be configured as a direct mapped four word 256 line instruction cache, or as an additional 1280 words of on-chip SRAM. The cache increases the processing speed when executing code from flash memory, and reduces the power consumption.

The instruction cache also provides support for large numbers of breakpoints when debugging. Many *BRK* instructions can be locked in the cache as soft breakpoints, even when executing code from internal flash memory.

Memory Management Unit

The Memory Management Unit (MMU) allows a variety of internal and external memories to be combined into a single logical memory structure. The memory structure or model has both code space and data space address locations to match the Harvard architecture CPU. The MMU provides both code space translations for program code and data space translations for variables and constants. A single physical memory can be mapped into both code and data space.

Flash Memory

The eCOG1X contains 512K bytes of on-chip flash memory for program and data storage, organised as 256K words x 16 bits. The flash memory is programmed with and operates from the eCOG1X's normal 3.3V supply; no external high voltages are required for erasing or programming.

The flash memory contains 11 sectors of various sizes. The following table shows the organisation of the flash memory:

Sector	A18	A17	A16	A15	A14	A13	Sector size (Kbytes)	Address Range (hexadecimal)
SA0	0	0	0	0	0	X	16	0x00000-0x03FFF
SA1	0	0	0	0	1	0	8	0x04000-0x05FFF
SA2	0	0	0	0	1	1	8	0x06000-0x07FFF
SA3	0	0	0	1	X	X	32	0x08000-0x0FFFF
SA4	0	0	1	X	X	X	64	0x10000-0x1FFFF
SA5	0	1	0	X	X	X	64	0x20000-0x2FFFF
SA6	0	1	1	X	X	X	64	0x30000-0x3FFFF
SA7	1	0	0	X	X	X	64	0x40000-0x4FFFF
SA8	1	0	1	X	X	X	64	0x50000-0x5FFFF
SA9	1	1	0	X	X	X	64	0x60000-0x6FFFF
SA10	1	1	1	X	X	X	64	0x70000-0x7FFFF

Table 15: Flash memory organisation

The flash memory can be programmed via the eICE debug port or in-system by the CPU. It supports the following functions.

- Read accesses in code space or data space.
- Complete flash memory erase (chip erase).
- Individual or multiple sector erase.
- Programming of single words.
- Buffered programming of up to 64 bytes in one write operation.
- Global write protection.
- Individual sector write protection.

The flash memory can be used in three different operating modes, each with different power consumption and timing requirements. These modes are:

Fast The flash memory has its fastest access time, but it also requires the largest power supply current.

Slow The power consumption is decreased significantly. The access time is increased such that the CPU clock speed must be reduced or the device must be configured for a large number of wait states on flash memory read cycles.

Stop The flash memory draws only leakage current. However, it cannot be accessed in this mode for either instruction fetch or data read cycles.

Internal Memory

The eCOG1X contains 24K bytes of on-chip static RAM, organised as 12K x 16 bits. The internal SRAM (IRAM) is divided into three banks. Bank 0 is always available, while banks 1 and 2 may be enabled or disabled.

Bank	Physical address	Function	Control
0	0x0000 to 0x3FFF (0 to 16K bytes)	Main IRAM block	Always available for IRAM access
1	0x4000 to 0x4FFF (16K to 20K bytes)	Optional extra IRAM	Normally enabled Can be disabled to save power
2	0x5000 to 0x5FFF (20K to 24K bytes)	Optional extra IRAM, also used for USB endpoint data buffer	Normally enabled Can be disabled to save power Available for USB when disabled

Table 16: Internal memory organisation

Interrupts

After power on or a hardware reset, execution starts from code space address zero mapped into the internal flash memory. The first four words of code space should contain an instruction to branch to the start of the application code.

The eCOG1X CPU supports 64 vectored interrupts and exceptions. The interrupt vector table follows immediately after the eight bytes containing the reset vector branch instruction. Each vector contains a 16-bit offset. When an interrupt occurs, the interrupt service routine address is found by reading the corresponding 16-bit vector offset and sign-extending it to a 25-bit code space address. It follows that all interrupt service routines must be located in the first 64K bytes (address range 0x0000000 to 0x000FFFF) or last 64K bytes (address range 0x1FF0000 to 0x1FFFFFF) of code space.

Address	Interrupt	Source
0x00 to 0x07	reset	Reset vector at location 0x0. User must insert a branch instruction at this address.
0x08	_ex_debug	Debug exception
0x0A	_ex_wdog_exp	Timer/counters, watchdog timer expired
0x0C	_ex_adr_err	MMU: access to an unmapped address EMI: access to a chip select that is disabled
0x0E	_ex_reserved	
0x10	_ex_tim	Exception interrupt from timer/counter module
0x12	_ex_v33	Exception interrupt from VDD 3.3V sense
0x14	_ex_usarta	Exception interrupt from DUSART channel A
0x16	_ex_usartb	Exception interrupt from DUSART channel B
0x18	_ex_uart1a	Exception interrupt from DUART1 channel A
0x1A	_ex_uart1b	Exception interrupt from DUART1 channel B
0x1C	_ex_uart2a	Exception interrupt from DUART2 channel A
0x1E	_ex_uart2b	Exception interrupt from DUART2 channel B
0x20	_int_tmr_exp	Timer/counters, timer TMR underflow
0x22	_int_cnt1_exp	Timer/counters, counter CNT1 underflow
0x24	_int_cnt2_exp	Timer/counters, counter CNT2 underflow
0x26	_int_cnt1_match	Timer/counters, counter CNT1 comparator match
0x28	_int_cnt2_match	Timer/counters, counter CNT2 comparator match
0x2A	_int_pwm1_exp	Timer/counters, PWM1 underflow
0x2C	_int_pwm2_exp	Timer/counters, PWM2 underflow
0x2E	_int_pwm1_match	Timer/counters, PWM1 transition value match
0x30	_int_pwm2_match	Timer/counters, PWM2 transition value match
0x32	_int_cap_exp	Timer/counters, input capture timer overflow
0x34	_int_cap1	Timer/counters, input capture timer event 1
0x36	_int_cap2	Timer/counters, input capture timer event 2
0x38	_int_cap3	Timer/counters, input capture timer event 3
0x3A	_int_cap4	Timer/counters, input capture timer event 4
0x3C	_int_cap5	Timer/counters, input capture timer event 5
0x3E	_int_cap6	Timer/counters, input capture timer event 6
0x40	_int_ltmr_exp	Timer/counters, long interval timer LTMR underflow
0x42	_int_espi	ESPI interrupts, tx ready, rx ready
0x44	_int_emac	Ethernet MAC interrupts
0x46	_int_mcpwm	MCPWM interrupts, period, transition
0x48	_int_usb_core	USB core interrupts
0x4A	_int_usb_wakeup	USB wakeup event interrupt
0x4C	_int_usb_fifo	USB FIFO interrupts
0x4E	_int_usb_dma	USB DMA interrupts
0x50	_int_aci	ACI module, ADC/DAC ready (conversion complete)
0x52	_int_i2s	I^2S port interrupts
0x54	_int_usarta_rx_rdy	DUSART channel A receive port ready

Table 17: Interrupt vectors

Address	Interrupt	Source
0x56	_int_usarta_tx_rdy	DUSART channel A transmit port ready
0x58	_int_usartb_rx_rdy	DUSART channel B receive port ready
0x5A	_int_usartb_tx_rdy	DUSART channel B transmit port ready
0x5C	_int_sci_tx_done	DUSART smart card transmit data complete
0x5E	_int_sci_tx_err	DUSART smart card transmit error detected
0x60	_int_sci	DUSART general smart card interrupt
0x62	_int_ifr_tx_done	DUSART infrared transmit data complete
0x64	_int_ifr_rx_done	DUSART infrared receive data complete
0x66	_int_ifr_rx_err	DUSART infrared receive error detected
0x68	_int_ifr_frame_done	DUSART infrared frame complete
0x6A	_int_uart1a_tx_rdy	UART1A transmit port ready
0x6C	_int_uart1a_rx_rdy	UART1A receive port ready
0x6E	_int_uart1b_tx_rdy	UART1B transmit port ready
0x70	_int_uart1b_rx_rdy	UART1B receive port ready
0x72	_int_uart2a_tx_rdy	UART2A transmit port ready
0x74	_int_uart2a_rx_rdy	UART2A receive port ready
0x76	_int_uart2b_tx_rdy	UART2B transmit port ready
0x78	_int_uart2b_rx_rdy	UART2B receive port ready
0x7A	_int_ehi	EHI module interrupt.
0x7C	_int_gpio	GPIO interrupt (edge or level detect)
0x7E	_int_dsci	DSCI interrupt (dual smart card interface)

Table 17: Interrupt vectors

eICE Debug Interface

The eICE debug interface provides a serial communication interface allowing an external device (the eICE master) to have read and write access in the memory and register space of the eCOG1 (slave), and to control the CPU state and program execution with various debug commands. Access to memory and registers can take place in real time, with the CPU running or halted.

eICE functions include:

- Interactive, real time debug.
- Non-intrusive (real time) access to memory and CPU registers.
- Single or double word memory accesses anywhere in CPU logical code and data spaces.
- Run/Step/Stop commands to control program execution.
- Address error detection.
- 32 bit data ICE operations.
- Synchronised (deterministic) access mode available by inserting instructions in code.
- Hardware address and data breakpoint registers.
- Flash programming.
- Version register to identify ICE interface.

The eICE debug interface requires only a 10-pin header on the target system. A low cost USB eICE adaptor plugs into this header and connects to the host PC via USB. This adaptor is used by the CyanIDE software development tool, allowing single stepping at C source code level and inspection or modification of variables or memory, while running the application on the target system.

Peripherals

This section gives a brief description of the eCOG1X device peripherals. For a complete description, see the eCOG1X User Manual.

System Support Module

The System Support Module (SSM) controls all internal clocks and reset signals for the eCOG1X CPU and peripherals.

The SSM has four principal functional blocks.

- Clock oscillators and PLL multipliers.
- CPU/memory clock selector.
- Divider chains.
- Peripheral clock selectors.

Clock sources

Five clock sources are used to provide all eCOG1X internal system clocks. Two crystal oscillators provide accurate reference clocks, which can be driven into two PLL multipliers providing a further two reference clocks. A relaxation oscillator provides a fifth clock source that requires no external components and provides very short startup times. The programmable PLL multipliers allow a wide range of clock frequencies to be generated.

- Low reference oscillator.
  A low power 32kHz oscillator using an external quartz watch crystal.
- Low PLL.
  Phase locked loop with a programmable multiplication factor from x2 to x305. The low reference oscillator provides the clock input to the low PLL.
- Relaxation oscillator.
  A simple RC oscillator that requires no external components for low cost systems. On the 208BGA packaged devices, an external resistor can be used to adjust the oscillator frequency, in the range 1-11MHz.
- High reference oscillator.
  A high performance oscillator using an external 5-10MHz quartz crystal (8MHz nominal).
- High PLL.
  Phase locked loop with a programmable multiplication factor from x2 to x50. The high PLL can be driven from the high reference oscillator, the relaxation oscillator, or the output of the low PLL.

CPU/Memory Clock Selector

The CPU/memory clock selector contains logic for detecting valid running clocks and selecting the master clock from the available clock signals. It also provides a prescaler and divider to control the frequencies of the clocks to both the CPU and the memory subsystem.

Divider Chains

Five 16-bit divider chains, each clocked from one of the principal system clock sources, provide the source clock signals for all the internal peripheral modules. The divider chains provide a range of clock frequencies to the peripherals, to be selected according to the speed of the peripheral or any low power requirements of the application. The output frequency division factors range from $\div 2$ to $\div 2^{16}$.

Peripheral Clock Selectors

Each of the 16 outputs from the five divider chains are fed into the peripheral clock selector block, giving a total of 80 possible clock frequencies for each peripheral from the five clock sources. For each peripheral module, one output from one of the five divider chains is selected to provide its clock signal. Most peripherals also have a 4-bit prescaler providing a further frequency division of $\div 1$ to $\div 16$.

Summary

The source clock and peripheral clock selections provide an extremely flexible system for controlling independently the frequencies of the clock signals to each peripheral. This has significant benefits in managing the power consumption of the device. High frequency clocks can be provided selectively to the high speed peripherals that need them, while low speed peripherals can use low frequency clocks, reducing unnecessary power consumption. Unused peripherals can have their clock stopped altogether, reducing their supply current to a minimum.

The following diagram shows the complete eCOG1X SSM clocking scheme.

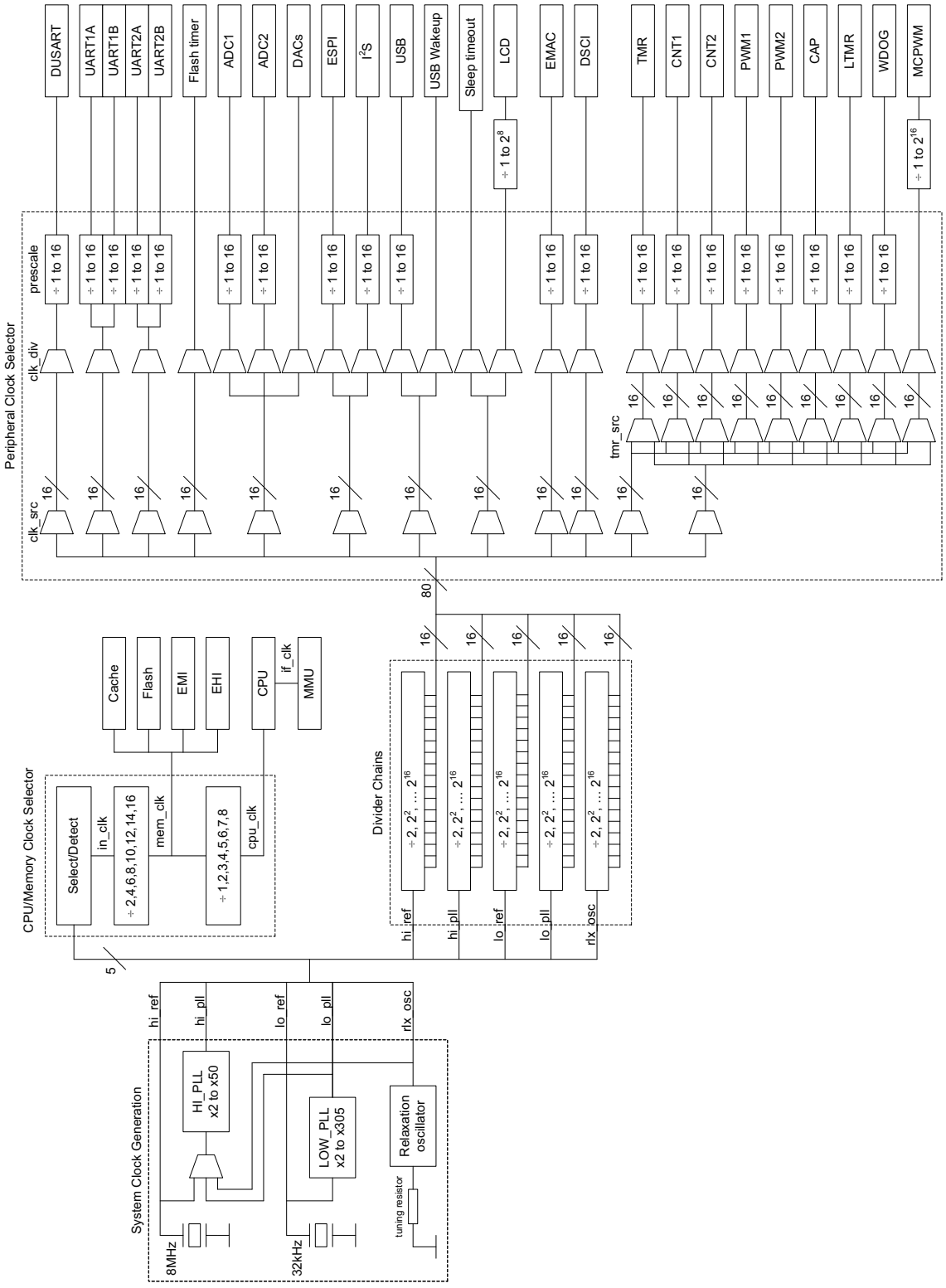


Figure 1: Detailed eCOG1X clocking scheme

Port Configurator

The eCOG1X devices in the 208BGA package include 19 I/O ports, consisting of eleven 8-bit ports and eight 4-bit ports. Devices in the smaller packages provide a subset of these I/O ports. The Port Configurator selects how the internal peripherals are connected to the external I/O ports. Each port may be assigned to a specified peripheral function, used for general-purpose I/O, or disabled.

The port configuration options are described in more detail later in this data sheet and in the eCOG1X User Manual.

General-Purpose I/O

In addition to the peripheral selections available through the Port Configurator, all I/O port pins can be configured individually for general-purpose I/O (GPIO) if required. GPIO pins can be configured as inputs, outputs or bidirectional. All GPIO pins can be configured for interrupts, either edge-triggered or level-triggered.

- Up to 120 GPIO port pins.
- Individually configurable as inputs, outputs or bidirectional.
- Outputs driven, open-drain or tristate controlled.
- 2mA source/sink output current (ports A, B, K, L, N, P, Q, R, S, T).
- 4mA source/sink output current (ports C, D, E, F, G, H, I, J, M).
- Open-drain output option with internal pull-up resistor (ports A, B, K, L, N, P, R, S, T).
- 5V tolerance (ports B0-4, K, L, N, P, Q).

Parallel I/O

eCOG1X also contains parallel I/O (PIO) peripheral functions. PIO allows users to control groups of 8 or 16 I/O signals at a time, whereas the GPIO function provides users with signals that can be individually controlled.

PIO is typically used for bus signals where it is necessary for the whole bus to change simultaneously, for example driving parallel output data signals into a DAC. GPIO is typically used for controlling individual signals, for example the output update signal to a DAC or start conversion signal to an ADC.

- Two 8/16-bit parallel data ports, configurable as inputs, outputs or bidirectional.
- Outputs driven, open-drain or tristate controlled.

Timers and Counters

The timer/counter (TIM) peripheral module provides a set of hardware timing and counting functions. Eight independent timers support a range of functions.

- 16-bit timer TMR.
- Two 16-bit timer/counters CNT1, CNT2.
- Two 16-bit timers PWM1, PWM2, providing a pulse-width modulated output signal.
- 16-bit watchdog timer WDOG.
- 16-bit event capture timer CAP with up to 6 capture inputs.
- 24-bit long interval timer LTMR.

Timer

The clock timer TMR is a 16-bit down count timer. An interrupt is generated when the timer counts past zero. The count duration may be preset or reset at any time. When enabled, the timer counts at its input clock frequency, set by the SSM.

Counter

The two timer/counters CNT1 and CNT2 are 16-bit down counters. An interrupt is triggered when the counter passes the value stored in a compare register. A second interrupt is generated when the counter passes zero. The count duration may be preset or reset at any time, and reload can be manual or automatic. In addition these timers may be configured to count on either or both edges of an external clock input.

When configured as timers, they count at their input clock frequencies, set by the SSM. Alternatively, when configured as counters, they count when a selected edge occurs on their external clock signal inputs. These timer/counters are therefore suitable for counting external events in a target system.

PWM

The two PWM timers are implemented as 16-bit down counters. An interrupt is generated when the timer passes a 'transition' value stored in one of the configuration registers, and a second interrupt is generated when the timer passes zero. The count duration may be preset or reset at any time.

When enabled, the PWM timers count at their input clock frequencies, set by the SSM. The PWM output signal inverts on each interrupt (transition or zero value). The sense of the output signal is programmable.

Typical applications are to generate a variable frequency output or a pulse width modulated output. Note that by adding an external low-pass filter, it is possible to use a PWM output as a low speed digital-to-analogue converter (DAC).

Capture Timer

The input capture timer CAP is a 16-bit up counter. An interrupt is generated when the timer wraps around to zero, and it may be reset to zero at any time. When enabled, the capture timer counts at its input clock rate, set by the SSM.

The capture timer value is transferred to one of the six capture registers when an edge is detected on one of the six capture inputs. Capture inputs 1-4 store all 16 bits of the capture timer value, while capture inputs 5 and 6 store only the high 8 bits of the capture timer value.

Watchdog Timer

The watchdog timer WDOG is a 16-bit down counter. The count duration may be preset to a new value or reset to the current period value at any time. When enabled, the watchdog timer counts at its input clock frequency, set by the SSM.

When the watchdog timer reaches zero for the first time, a watchdog timeout exception interrupt is generated and the counter restarts automatically to begin a new countdown period. If the watchdog timer reaches zero for a second time without being restarted by the application software, then a hardware watchdog timeout reset signal is generated on the power-on reset output pin (nRESET or nRESET_OUT).

Long Interval Timer

The long interval timer LTMR is a 24-bit down counter, allowing a maximum count of 2^{24}. An interrupt is generated when the timer passes zero. The upper 16 bits of the timer may be set at any time to the value in a load register; the lower 8 bits are reset to zero when the upper 16 bits are written. When enabled, the long interval timer counts at its input clock frequency, set by the SSM.

DUARTs

The eCOG1X includes two identical DUART modules, DUART1 and DUART2. Each DUART module provides two separate UART channels, labelled A and B.

The four UART channels support the following features:

- Programmable format: 5, 6, 7 or 8 data bits; 1, 1.5 or 2 stop bits; even, odd or no parity.
- Programmable baud rate divider.
- 8-bit and 16-bit transmit data registers (one and two data frames).
  Interrupts generated on transmit ready and overflow.
- 8-bit receive data register (one data frame) with two byte receive FIFO.
  Receive data ready interrupt generated on one or two bytes received.
- Oversampled received data with noise filter.
  Receiver error detection for false start bits, parity and frame errors.
- Configurable data signal polarities.
- Receive timeout detection of 1 to 63 bit periods.
- Line Break (15 consecutive data zero bits) generation in software, detection in hardware.
- Prescaled UART clock to reduce power consumption.
- Power saving features to start the UART clock automatically when the receiver detects a start bit and to hold the clock active during transmission.
- Operates independently of the CPU, allowing the CPU to be put to sleep while the DUART transmit or receive is still active.

DUSART

The DUSART is a general purpose dual synchronous/asynchronous serial port. Each of the two channels can implement one of the supported protocols. Note that each serial protocol may only be used once, the same protocol cannot be used simultaneously on both channels (except for the generic User Serial Port function which can be used on both channels).

The following protocols are supported by the DUSART peripheral.

- Standard UART.
- Serial Peripheral Interface (SPI).
- I^2C multi-master, multi-drop 2 wire bus.
- Low rate IrDA and general purpose infrared controller protocol (IFR).
- ISO 7816 smart card interface (SCI).
- Generic User Serial Port (USR).

UART

The UART implementation within the DUSART peripheral provides all of the common functions required.

- Programmable format: 5, 6, 7 or 8 data bits; 1, 1.5 or 2 stop bits, even, odd or no parity.
- Programmable baud rate.
- 8-bit and 16-bit transmit data registers (one and two data frames).
  Interrupts generated on transmit ready and overflow.
- 8-bit and 16-bit receive data register (one and two data frames).
  Interrupts generated on one or two bytes received.
- Configurable data signal polarities.
- Transmit break control.
- Receive break interrupt and status bit.
- Receive frame error detection interrupt and status bit.
- Receive timeout.
- Transmit guard time.

SPI

SPI is one of the protocols supported by the DUSART peripheral. This gives the eCOG1X both SPI master and slave capability, with the option of supporting multiple slave devices in master mode.

The SPI function includes the following features.

- Master and slave operation.
- Programmable serial clock polarity and phase.
- Data transfer size 1 to 16 bits.
- Programmable serial clock frequency (master mode).
- Up to four chip select outputs (master mode).
- Slave mode chip select uses up to four inputs with a pattern match and mask function.

I^2C

The Inter-IC Communication standard (I^2C) is a bidirectional, multi-drop, multi-master, two wire interface for connecting microcontrollers to their peripheral devices such as memories and interface ICs. It is capable of serial data transfer up to speeds of 100 kbps (standard), 400 kbps (fast mode) and 3.4 Mbits/s (high speed mode). The DUSART I^2C function supports 100 kbps operation only.

The I^2C function includes the following features.

- Start, stop, and restart operations.
- Address matching and arbitration.
- Supports multi-master and master/slave operations.
- Automatic acknowledge generation.
- 7 bit, 10 bit and broadcast addressing.

IFR

The IFR function in the DUSART provides a configurable CODEC designed for the transmission and reception of infra-red data frames. Input signals should be demodulated externally before being supplied to the device for decoding. The IFR transmit data output signal may be provided both modulated and unmodulated.

The module is designed to be flexible, supporting current consumer protocols (RC-5, ASK, PPM) and other infra-red protocols. Some support is also provided for low-rate IrDA format signals.

SCI

The Smart Card Interface (SCI) function in the DUSART contains all of the logic functionality required for the terminal (controller) part of a smart card interface. Activation and deactivation sequences are supported with various degrees of (configurable) automation. Protocol type T=0 is supported; refer to the Smart Card standard ISO 7816 parts 1-10.

The SPI function includes the following features.

- Card activation sequencer with hardware delay timer.
- Card deactivation sequencer with hardware delay timer.
- Data transmit sequencer with hardware guard time, error detection and retransmission.
- Data receive sequencer with hardware error detection and retransmit request.
- Programmable signal polarities.
- UART serial port operation.
- Normal or inverse data convention.

USR

The USR function provides flexible, low-level access to the core features of the DUSART peripheral. It may be used to implement synchronous or asynchronous protocols that are not already supported by the other DUSART functions, for example a 9-bit UART protocol, with less software overhead than a GPIO based emulation.

The USR function includes the following features.

- Provides direct access to internal USART features.
- Allows custom serial protocols to be emulated.
- Up to 255 symbols per frame.
- Automatic parity generation and checking.
- Start bit edge detection.
- Transmit and receive data interrupts.

External Memory Interface

The External Memory Interface (EMI) allows connection of external memories to both code and data space of the CPU via the memory manager.

The EMI supports two memory interface modes:

- Bus Interface Mode:
  (a) Independent 25-bit address and 8-bit data, or
  (b) Multiplexed 24-bit address and 16-bit data.
  This interface can connect to external devices such as flash memory, SRAM, ROM or memory mapped peripherals.
- SDRAM Interface Mode:
  Supports direct connection to 16-bit wide single data rate SDRAM (up to 32Mbytes) with no external components.

The EMI has two chip select outputs that can be programmed individually to operate with either the SDRAM or Bus interfaces. If both chip selects are configured for the same interface type, then the settings are the same for both external memories. This means that the memories' timing parameters and control signals must be compatible.

The EMI peripheral includes the following features.

- 8 or 16-bit data bus.
- 16 or 24-bit address bus.
- Multiplexed address/data in 16-bit data bus mode.
- External devices can be mapped into both code and data space.
- Configurable cycle and signal timing.
- Four SDRAM row/column address multiplexing schemes.
- Supports SDRAM auto and self refresh.
- Supports low-power SDRAM suspend/standby modes.
- Single cycle data space accesses.
- Burst accesses in code space, using instruction cache.
- Add wait states for slow devices with the EMI_WAIT input signal.

External Host Interface

The External Host Interface (EHI) allows the eCOG1X and an external processor to share an area of the eCOG1X internal SRAM which can be directly accessed by both the eCOG1X processor and the external device. The eCOG1X processor can write and read to the locations via the MMU, whilst the external device can write and read to the locations via the EHI.

The external device has two modes in which it can access the internal SRAM. In MMP mode, the eCOG1X is seen as a memory mapped peripheral and the shared SRAM area is mapped into the memory map of the external device. In DMA mode, the external device accesses the shared SRAM area using the DMA control signals.

MMP mode is intended for small random accesses, whilst DMA mode is intended for large block copy data transfers. The EHI provides a means for enabling both modes to assist the interleaving of large and small data accesses.

The EHI peripheral includes the following features.

DMA mode:

- Supports master and slave mode timings.
- 16 or 32-bit data bus.
- Request and acknowledge control signals.
- Programmable transfer cycle timing in master mode.
- DMA connection into internal SRAM.
- 11-bit block address, maximum block size 256 bytes.

MMP mode:

- Selectable block size: 256 x 16-bit data, or 8 x 32-bit data.
- Three control signals: chip select, read/write direction, and wait.
- Configurable control signal senses.

Analogue Input and Output

The eCOG1X includes a flexible analogue control interface peripheral (ACI) providing analogue inputs and outputs.

The main features of the Analogue Control Interface include:

- Two-channel successive approximation Analogue to Digital Converter (ADC).
- Two-channel 12-bit Digital to Analogue Converter (DAC).
- Internal 1.2V nominal bandgap voltage reference.
- Analogue multiplexer with one internal and seven external input signals for each ADC.
- Internal ADC inputs for temperature sensor and analogue supply voltage sensor.
- Single-ended and differential input configurations.
- Selectable ADC resolution of 6, 8, 10 or 12 bits.
- Maximum conversion rates on each ADC channel:
  - 200ks/s at 12 bits resolution.
  - 350ks/s at 10 bits resolution.
  - 500ks/s at 8 bits resolution.
  - 800ks/s at 6 bits resolution.
- Simultaneous sampling on the two ADC channels.
- Sample/hold time can be increased for higher source impedances.
- Automatic multiplexer channel scanning in hardware.
- Interrupt on conversion scan complete.
- Flexible software or hardware triggered conversion for both ADCs and DACs.
- Analogue outputs settle to 12 bits accuracy within 4µs.
- Power on reset circuit and low I/O supply voltage status bit.

I^2S

The I^2S (Inter-IC Sound) standard bus was developed by Philips Semiconductors to provide a simple, low pin count serial link for digital audio data. The eCOG1X I^2S peripheral provides both master and slave capability, programmable data size and clock frequencies, and simultaneous bidirectional data transfers.

The I^2S peripheral has the following main features.

- Programmable data word size up to 32 bits for each channel.
- Internal or external clock source.
  - Internal clock source is set in the SSM.
  - Alternate clock input supports frequencies that cannot be achieved by the SSM.
- Master or slave mode.
  - The master device outputs SCLK and WS to the slave device.
  - Selection of master or slave mode is independent of the clock source selection.
- Master clock output, required by some CODECs for oversampling and digital filtering.
  - MCLK frequency = selected input clock frequency.
- Programmable divider for bit clock SCLK.
  - SCLK is divided down from the selected input clock (= MCLK).
  - Division ratios: ÷ 2, 4, 8, 16, 32, 48, 64, 96, 128, 192, 256, 384, 512, 768, 1024.
  - Option to bypass MCLK and set SCLK = input clock.
- Word select clock WS is set according to the number of data bits selected.
  - WS clock frequency = SCLK frequency divided by number of data bits x 2 (stereo audio has two data values per sample).
- Programmable clock and data signal polarities.

ESPI

The Enhanced Serial Peripheral Interface (ESPI) provides the eCOG1X with both SPI master and slave capability, and has the option of supporting multiple slaves in master mode. It is independent of the DUSART SPI function, and has further performance improvements and additional features.

The ESPI peripheral has the following main features.

- New, enhanced SPI peripheral independent of the DUSART.
- Supports both master and slave modes.
- Programmable single transfer size from 1 to 16 bits.
- Programmable serial clock polarity and phase.
- Four chip select signals, outputs in master mode and inputs in slave mode.
- Supports multiple data transfers (frames) in master mode.
- Programmable timer values for chip select delay times.

LCD Controller

The LCD controller provides the eCOG1X with hardware support for driving simple static or multiplexed LCDs.

The LCD controller peripheral has the following main features.

- For use with simple static and multiplexed LCDs.
- 32 segment and 4 backplane (common) driver outputs.
- Supports 1, 2, 3 or 4 way multiplexing.
- Provides continuous control of up to 128 display segments.
- Automatic display operation with static data.
- Programmable 8-bit input clock prescaler.
- The port multiplexer can enable subsets of the segment outputs.

Motor Control PWM

This peripheral module provides a flexible multi-channel PWM timer function, intended for motor control applications.

The MCPWM peripheral has the following main features.

- Suitable for 3-phase motor control.
- Six PWM timer outputs.
  - 16 bits resolution.
  - Sufficient to control a 3-phase full-bridge drive circuit.
- Two independent timebase period counters.
  - Use one timebase counter for 3-phase full bridge drive.
  - Use two timebase counters for two sets of 3-phase half bridge drive.
- Double buffered transition value registers.
- Programmable output sense.
- Programmable 16-bit input clock prescaler.
- Asymmetrical and symmetrical period counter modes.
  - In asymmetrical mode, the period counter runs from zero to max, and resets to zero after one period.
  - In symmetrical mode, the period counter runs from zero to max and back to zero over two periods.
- Output toggle and return-to-zero modes.
  - In output toggle mode, the outputs change state at each transition match time.
  - In return-to-zero mode, the outputs are set at the start of each period and cleared at their transition match times.
- Supports edge-aligned, centre-aligned and user-defined PWM operating schemes.
- Guard time or dead time mode.

Dual Smart Card Interface

The Dual Smart Card Interface (DSCI) module provides two complete smart card interface peripherals, independent of the single SCI function available within the DUSART peripheral.

The DSCI peripheral has the following main features.

- Two independent smart card interface blocks. The only shared resources are the common peripheral clock and reset (from the SSM), and the interrupt vector.
- Flexible smart card clock generation with support for clock stop. The smart card clock is derived from the DSCI peripheral clock. Its frequency can be changed while running, either by changing the DSCI peripheral clock in the SSM, or by changing the smart card clock prescaler in the DSCI.
- Dedicated serial port for each smart card.
  - Programmable bit polarity and character endianness.
  - Programmable guard time insertion from 1 to 256 etus.
  - Programmable baud rate derived from the DSCI peripheral clock.
  - Parity generation and checking (even or odd parity).
  - Double buffered receive and transmit data registers.
  - Programmable receive character timeout. This feature can be used for the EMV Work Waiting Time function in the T=0 protocol, or for the Character Waiting Time and/or Block Waiting Time functions in the T=1 protocol.
  - Programmable error detection and retransmission support for the T=0 protocol.
- Card activation and deactivation sequences, with manual or automatic start on card insertion and removal.
  - Programmable delay times for activation and deactivation sequences.
  - Programmable polarity for card detect, reset and power enable signals.
  - The DSCI can be deactivated to reduce power consumption until a card is inserted.
- Flexible software interface with interrupt support.
  - Card insertion and removal.
  - Card activation and deactivation sequence complete.
  - Received data available.
  - Transmitter ready.
  - Error conditions

Ethernet MAC

The eCOG1X includes an Ethernet MAC peripheral which can be used with a suitable external PHY device.

The main features of the EMAC peripheral include:

- Supports both 10Mbits/s and 100Mbits/s operation with the appropriate external PHY device fitted.
- Media Independent Interface (MII) for PHY device configuration.
- Complies with IEEE 802.3 CSMA/CD standard.
- Single address filtering.
- Buffer descriptors may be arranged as a ring or a chain.

The EMAC peripheral contains four main functional blocks.

- Control/status registers.
- DMA controller.
- Transmit data path.
- Receive data path.

Both the transmit and receive data paths have their own separate 128 byte FIFO to provide data flow buffering. Data packets are stored in internal SRAM, accessed via the DMA controller. The DMA controller is managed through registers in the eCOG1X internal peripheral register space.

The EMAC peripheral is controlled through a set of control/status registers (CSRs), located at an address defined by the MMU. Access to these registers is possible only when the MMU has been configured to set the base address for these registers in data space, and the SSM has been configured to provide a suitable clock signal to the EMAC.

USB Interface

The eCOG1X includes a USB 2.0 compatible peripheral module. It operates in USB host and peripheral modes, with support for On-The-Go functions. It supports low speed (1.5Mb/s), full speed (12Mb/s), and high speed (480Mb/s) modes.

An internal PHY supports low speed and full speed modes. High speed mode is supported with an external PHY, using a ULPI bus connection.

The USB core in the eCOG1X offers the following features:

- Low speed (LS), Full Speed (FS) and High Speed (HS) operation
- USB host, peripheral and On-The-Go (OTG) use
- Internal PHY for LS, FS and OTG operation.
- ULPI interface for use with external HS PHY.

The USB core requires 4Kbytes of working memory, used for the endpoint data buffers. This is taken from the top of the internal memory and cannot then be accessed directly by the processor. Reading and writing to this memory is always done either through the USB core FIFO registers or with the DMA peripheral and the slave FIFO.

The USB core is controlled through a set of memory mapped registers, located at an address defined by the MMU. The USB DMA channel is controlled through the eCOG1X internal peripheral registers.

Port Select Options

The eCOG1X device pins are connected to 19 I/O ports labelled A to T. Different peripheral functions can be mapped to these ports to define the operation of each pin. This section contains tables listing the peripheral signals available for each of the configurable ports. For further details, refer to the eCOG1X User Manual.

Port A

Port A is available on all eCOG1X device variants and packages.

port.sel1.a	1	2	3	4	5
A_0	EMAC_TXD0	LCD_COM0	EMI_D0	SCA_CLK	USRA_RX_CLK_OUT
A_1	EMAC_TXD1	LCD_COM1	EMI_D1	SCA_RESET	USRA_TX_CLK_OUT
A_2	EMAC_TXD2	LCD_COM2	EMI_D2	SCA_PWR_EN	USRA_DATA_OUT
A_3	EMAC_TXD3	LCD_COM3	EMI_D3	SCA_CARD_IN	USRA_DATA0_IN
A_4	EMAC_RXD0	LCD_SEG4	EMI_D4	SCA_DATA	USRA_DATA1_IN
A_5	EMAC_RXD1	LCD_SEG5	EMI_D5	LCD_COM0	USRA_DATA2_IN
A_6	EMAC_RXD2	LCD_SEG6	EMI_D6	UART2A_TX	USRA_RX_CLK_IN
A_7	EMAC_RXD3	LCD_SEG7	EMI_D7	UART2A_RX	USRA_TX_CLK_IN

port.sel1.a	6	7	8	9
A_0	USRA_RX_CLK_OUT	UART1A_TX	LCD_SEG0	LCD_COM0
A_1	USRA_TX_CLK_OUT	UART1A_RX	LCD_SEG1	LCD_SEG1
A_2	USRA_DATA_OUT	UART1B_TX	LCD_SEG2	LCD_SEG2
A_3	USRA_DATA0_IN	UART1B_RX	LCD_SEG3	LCD_SEG3
A_4	USRB_RX_CLK_OUT	UART2A_TX	LCD_SEG4	LCD_SEG4
A_5	USRB_TX_CLK_OUT	UART2A_RX	LCD_SEG5	LCD_SEG5
A_6	USRB_DATA_OUT	UART2B_TX	LCD_SEG6	LCD_SEG6
A_7	USRB_DATA0_IN	UART2B_RX	LCD_SEG7	LCD_SEG7

Port B

Port B is available on all eCOG1X device variants and packages.

port.sel1.b	1	2	3	4	5	6
B_0	EMAC_CLKT	LCD_COM0	SPI_SCLK	SCB_CLK	ESPI_SCLK	I2S_SCLK
B_1	EMAC_CLKR	LCD_COM1	SPI_MOSI	SCB_RESET	ESPI_MOSI	I2S_WS
B_2	EMAC_RXER	LCD_COM2	SPI_MISO	SCB_PWR_EN	ESPI_MISO	I2S_SD_OUT
B_3	EMAC_RXDV	LCD_COM3	SPI_CS0	SCB_CARD_IN	ESPI_CS0	I2S_SD_IN
B_4	EMAC_COL	LCD_SEG12	SPI_CS1	SCB_DATA	ESPI_CS1	I2S_ALT_CLK_IN
B_5	EMAC_CRS	LCD_SEG13	SPI_CS2	CAP_TRIG1	ESPI_CS2	I2S_MCLK
B_6	EMAC_TXEN	LCD_SEG14	SPI_CS3	PWM1	ESPI_CS3	PWM1
B_7	EMAC_TXER	LCD_SEG15	PWM1	PWM2	PWM1	PWM2

port.sel1.b	7	8	9	10	11
B_0	USRB_RX_CLK_OUT	USRA_RX_CLK_OUT	CAP_TRIG1	CAP_TRIG1	MCPWM1
B_1	USRB_TX_CLK_OUT	USRA_TX_CLK_OUT	CAP_TRIG2	CAP_TRIG2	MCPWM2
B_2	USRB_DATA_OUT	USRA_DATA_OUT	CAP_TRIG3	CAP_TRIG3	MCPWM3
B_3	USRB_DATA0_IN	USRA_DATA0_IN	CAP_TRIG4	CAP_TRIG4	MCPWM4
B_4	USRB_DATA1_IN	USRB_RX_CLK_OUT	CAP_TRIG5	CNT1_TRIG	MCPWM5
B_5	USRB_DATA2_IN	USRB_TX_CLK_OUT	CAP_TRIG6	CNT2_TRIG	MCPWM6
B_6	USRB_RX_CLK_IN	USRB_DATA_OUT	CNT1_TRIG	PWM1	PWM1
B_7	USRB_TX_CLK_IN	USRB_DATA0_IN	PWM2	PWM2	PWM2

port.sel1.b	12	13	14
B_0	LCD_SEG8	LCD_COM0	USB_OTG_VBUSVALID
B_1	LCD_SEG9	LCD_SEG9	USB_OTG_AVALID
B_2	LCD_SEG10	LCD_SEG10	USB_OTG_BVALID
B_3	LCD_SEG11	LCD_SEG11	USB_OTG_SESSEND
B_4	LCD_SEG12	LCD_SEG12	USB_OTG_IDDIG
B_5	LCD_SEG13	LCD_SEG13	USB_OTG_IDPULLUP
B_6	LCD_SEG14	LCD_SEG14	USB_OTG_DRVVBUS
B_7	LCD_SEG15	LCD_SEG15	USB_OTG_CHRGVBUS

Port C

Port C is available on all eCOG1X device variants and packages.

port.sel1.c	1	2	3	4	5	6	7
C_0	USB_ULPI_RST	SPI_SCLK	I2C_SCL	I2C_SCL	IR_RX	I2S_SCLK	UART1A_TX
C_1	USB_ULPI_DIR	SPI_MOSI	I2C_SDA	I2C_SDA	IR_TX	I2S_WS	UART1A_RX
C_2	USB_ULPI_NXT	SPI_MISO	UART_TX	IR_RX	UART_TX	I2S_SD_OUT	UART1B_TX
C_3	USB_ULPI_STOP	SPI_CS0	UART_RX	IR_TX	UART_RX	I2S_SD_IN	UART1B_RX

port.sel1.c	8	9	10	12	13
C_0	CNT1_TRIG	CAP1_TRIG	CNT1_TRIG	MCPWM1	USB_OTG_VBUSVALID
C_1	CNT2_TRIG	CAP2_TRIG	CNT2_TRIG	MCPWM2	USB_OTG_AVALID
C_2	PWM1	PWM1	CAP1_TRIG	MCPWM3	USB_OTG_SESSEND
C_3	PWM2	PWM2	CAP2_TRIG	PWM1	USB_OTG_DRVVBUS

Port D

Port D is available on all eCOG1X device variants and packages.

port.sel1.d	1	2	3	4
D_0	EMI_CS0	EHI_REQ	I2C_SCL	I2C_SCL
D_1	EMI_CS1	EHI_ACK	I2C_SDA	I2C_SDA
D_2	EMI_RW_RS_WEN	EHI_RW	UART_TX	IR_RX
D_3	EMI_DS0_WS0_CAS	EHI_CS	UART_RX	IR_TX

port.sel1.d	5	6	7	8
D_0	IR_RX	SPI_CS0	SPI_SCLK	USB_OTG_BVALID
D_1	IR_TX	SPI_CS1	SPI_MOSI	USB_OTG_SESSEND
D_2	UART_TX	SPI_CS2	SPI_MISO	USB_OTG_CHRGVBUS
D_3	UART_RX	SPI_CS3	SPI_CS0	USB_OTG_DISCHRGVBUS

Port E

Port E is available on all eCOG1X device variants and packages.

port.sel2.e	1	2	3	4	5
E_0	EMI_A0	EHI_D0	LCD_SEG16	SCB_CLK	ESPI_SCLK
E_1	EMI_A1	EHI_D1	LCD_SEG17	SCB_RESET	ESPI_MOSI
E_2	EMI_A2	EHI_D2	LCD_SEG18	SCB_PWR_EN	ESPI_MISO
E_3	EMI_A3	EHI_D3	LCD_SEG19	SCB_CARD_IN	ESPI_CS0
E_4	EMI_A4	EHI_D4	LCD_SEG20	SCB_DATA	ESPI_CS1
E_5	EMI_A5	EHI_D5	LCD_SEG21	PWM1	ESPI_CS2
E_6	EMI_A6	EHI_D6	LCD_SEG22	UART2B_TX	ESPI_CS3
E_7	EMI_A7	EHI_D7	LCD_SEG23	UART2B_RX	PWM1

port.sel2.e	6	7	8	9	10
E_0	USRA_RX_CLK_OUT	USRA_RX_CLK_OUT	UART1A_TX	CAP_TRIG1	CAP_TRIG1
E_1	USRA_TX_CLK_OUT	USRA_TX_CLK_OUT	UART1A_RX	CAP_TRIG2	CAP_TRIG2
E_2	USRA_DATA_OUT	USRA_DATA_OUT	UART1B_TX	CAP_TRIG3	CAP_TRIG3
E_3	USRA_DATA0_IN	USRA_DATA0_IN	UART1B_RX	CAP_TRIG4	CAP_TRIG4
E_4	USRA_DATA1_IN	USRB_RX_CLK_OUT	UART2A_TX	CAP_TRIG5	CNT1_TRIG
E_5	USRA_DATA2_IN	USRB_TX_CLK_OUT	UART2A_RX	CAP_TRIG6	CNT2_TRIG
E_6	USRA_RX_CLK_IN	USRB_DATA_OUT	UART2B_TX	CNT1_TRIG	PWM1
E_7	USRA_TX_CLK_IN	USRB_DATA0_IN	UART2B_RX	PWM2	PWM2

port.sel2.e	11	12	13	14
E_0	MCPWM1	SC_CLK_EN	SCA_CLK	USB_OTG_VBUSVALID
E_1	MCPWM2	SC_RESET	SCA_RESET	USB_OTG_AVALID
E_2	MCPWM3	SC_PWR_EN	SCA_PWR_EN	USB_OTG_BVALID
E_3	MCPWM4	SC_CARD_IN	SCA_CARD_IN	USB_OTG_SESSEND
E_4	MCPWM5	SC_DATA	SCA_DATA_IN	USB_OTG_IDDIG
E_5	MCPWM6	PWM2	SCA_DATA_OUT	USB_OTG_IDPULLUP
E_6	PWM1	UART2B_TX	UART2B_TX	USB_OTG_DRVVBUS
E_7	PWM2	UART2B_RX	UART2B_RX	USB_OTG_CHRGVBUS

Port F

Port F is available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel2.f	1	2	3	4	5
F_0	EMI_A8	EHI_D8	I2C_SCL	I2C_SCL	IR_RX
F_1	EMI_A9	EHI_D9	I2C_SDA	I2C_SDA	IR_TX
F_2	EMI_A10	EHI_D10	UART_TX	IR_RX	UART_TX
F_3	EMI_A11	EHI_D11	UART_RX	IR_TX	UART_RX

Port G

Port G is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel2.g	1	2
G_0	EMI_A12	EHI_D12
G_1	EMI_A13	EHI_D13
G_2	EMI_A14_DQML	EHI_D14
G_3	EMI_A15_DQMH	EHI_D15

Port H

Port H is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel2.h	1	2
H_0	EMI_D0	EHI_D16
H_1	EMI_D1	EHI_D17
H_2	EMI_D2	EHI_D18
H_3	EMI_D3	EHI_D19
H_4	EMI_D4	EHI_D20
H_5	EMI_D5	EHI_D21
H_6	EMI_D6	EHI_D22
H_7	EMI_D7	EHI_D23

Port I

Port I is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel3.i	1	2
I_0	EMI_D8_A16	EHI_D24
I_1	EMI_D9_A17	EHI_D25
I_2	EMI_D10_A18	EHI_D26
I_3	EMI_D11_A19	EHI_D27_A3
I_4	EMI_D12_A20	EHI_D28_A4
I_5	EMI_D13_A21	EHI_D29_A5
I_6	EMI_D14_A22	EHI_D30_A6
I_7	EMI_D15_A23	EHI_D31_A7

Port J

Port J is available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel3.j	1	2	3	4	5
J_0	EMI_DS1_WS1_RAS	EHI_WAIT	I2C_SCL	I2C_SCL	IR_RX
J_1	EMI_CKE	EHI_A0	I2C_SDA	I2C_SDA	IR_TX
J_2	EMI_WAIT	EHI_A1	UART_TX	IR_RX	UART_TX
J_3	EMI_CLK	EHI_A2	UART_RX	IR_TX	UART_RX

Port K

Port K is available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel3.k	1	2	3	4
K_0	LCD_COM0	LCD_SEG0	I2C_SCL	I2C_SCL
K_1	LCD_COM1	LCD_SEG1	I2C_SDA	I2C_SDA
K_2	LCD_COM2	LCD_SEG2	UART_TX	IR_RX
K_3	LCD_COM3	LCD_SEG3	UART_RX	IR_TX

port.sel3.k	5	6	7	8
K_0	IR_RX	SPI_SCLK	SCA_CLK	SPI_CS1
K_1	IR_TX	SPI_MOSI	SCA_RESET	USB_OTG_DISCHRGVBUS
K_2	UART_TX	SPI_MISO	SCA_PWR_EN	UART_TX
K_3	UART_RX	SPI_CS0	SCA_CARD_IN	UART_RX

Port L

Port L is available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel3.l	1	2	3	4
L_0	LCD_SEG24	LCD_COM0	I2C_SCL	I2C_SCL
L_1	LCD_SEG25	LCD_COM1	I2C_SDA	I2C_SDA
L_2	LCD_SEG26	LCD_COM2	UART_TX	IR_RX
L_3	LCD_SEG27	LCD_COM3	UART_RX	IR_TX

port.sel3.l	5	6	7
L_0	IR_RX	UART1A_TX	SCA_DATA
L_1	IR_TX	UART1A_RX	SCA_CARD_IN
L_2	UART_TX	UART1B_TX	SCB_DATA
L_3	UART_RX	UART1B_RX	SCB_CARD_IN

Port M

Port M is available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel4.m	1	2	3	4
M_0	USB_ULPI_DATA0	PIOA_8	LCD_SEG24	SCA_CLK
M_1	USB_ULPI_DATA1	PIOA_9	LCD_SEG25	SCA_RESET
M_2	USB_ULPI_DATA2	PIOA_10	LCD_SEG26	SCA_PWR_EN
M_3	USB_ULPI_DATA3	PIOA_11	LCD_SEG27	SCA_CARD_IN
M_4	USB_ULPI_DATA4	PIOA_12	LCD_SEG28	SCA_DATA
M_5	USB_ULPI_DATA5	PIOA_13	LCD_SEG29	SCB_CLK
M_6	USB_ULPI_DATA6	PIOA_14	LCD_SEG30	SCB_RESET
M_7	USB_ULPI_DATA7	PIOA_15	LCD_SEG31	SCB_PWR_EN

port.sel4.m	5	6	7	8
M_0	USRA_RX_CLK_OUT	USRA_RX_CLK_OUT	UART1A_TX	USB_OTG_VBUSVALID
M_1	USRA_TX_CLK_OUT	USRA_TX_CLK_OUT	UART1A_RX	USB_OTG_AVALID
M_2	USRA_DATA_OUT	USRA_DATA_OUT	UART1B_TX	USB_OTG_BVALID
M_3	USRA_DATA0_IN	USRA_DATA0_IN	UART1B_RX	USB_OTG_SESSEND
M_4	USRA_DATA1_IN	USRB_RX_CLK_OUT	UART2A_TX	USB_OTG_IDDIG
M_5	USRA_DATA2_IN	USRB_TX_CLK_OUT	UART2A_RX	USB_OTG_IDPULLUP
M_6	USRA_RX_CLK_IN	USRB_DATA_OUT	UART2B_TX	USB_OTG_DRVVBUS
M_7	USRA_TX_CLK_IN	USRB_DATA0_IN	UART2B_RX	USB_OTG_CHRGVBUS

Port N

Port N is available on the following eCOG1X device variants:
eCOG1X0A, 4A and 8A in the 68QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel4.n	1	2	3	4
N_0	LCD_COM0	PIOA_0	SPI_SCLK_OUT	SCB_CLK
N_1	LCD_COM1	PIOA_1	SPI_SCLK_IN	SCB_RESET
N_2	LCD_COM2	PIOA_2	SPI_CS0_OUT	SCB_PWR_EN
N_3	LCD_COM3	PIOA_3	SPI_CS0_IN	SCB_CARD_IN
N_4	LCD_SEG28	PIOA_4	SPI_DATA_IN	SCB_DATA
N_5	LCD_SEG29	PIOA_5	SPI_DATA_OUT	SCA_CLK
N_6	LCD_SEG30	PIOA_6	I2C_SCL	SCA_RESET
N_7	LCD_SEG31	PIOA_7	I2C_SDA	SCA_PWR_EN

port.sel4.n	5	6	7	8
N_0	USRA_RX_CLK_OUT	USRA_RX_CLK_OUT	SC_CLK_EN	SCB_CLK
N_1	USRA_TX_CLK_OUT	USRA_TX_CLK_OUT	SC_RESET	SCB_RESET
N_2	USRA_DATA_OUT	USRA_DATA_OUT	SC_PWR_EN	SCB_PWR_EN
N_3	USRA_DATA0_IN	USRA_DATA0_IN	SC_CARD_IN	SCB_CARD_IN
N_4	USRA_DATA1_IN	USRB_RX_CLK_OUT	SC_DATA_IN	SCB_DATA_IN
N_5	USRA_DATA2_IN	USRB_TX_CLK_OUT	SC_DATA_OUT	SCB_DATA_OUT
N_6	USRA_RX_CLK_IN	USRB_DATA_OUT	I2C_SCL	I2C_SCL
N_7	USRA_TX_CLK_IN	USRB_DATA0_IN	I2C_SDA	I2C_SDA

Port P

Port P is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel4.p	1	2	3	4
P_0	PIOA_0	LCD_SEG0	LCD_COM0	LCD_COM0
P_1	PIOA_1	LCD_SEG1	LCD_SEG1	LCD_COM1
P_2	PIOA_2	LCD_SEG2	LCD_SEG2	LCD_SEG2
P_3	PIOA_3	LCD_SEG3	LCD_SEG3	LCD_SEG3
P_4	PIOA_4	LCD_SEG4	LCD_SEG4	LCD_SEG4
P_5	PIOA_5	LCD_SEG5	LCD_SEG5	LCD_SEG5
P_6	PIOA_6	LCD_SEG6	LCD_SEG6	LCD_SEG6
P_7	PIOA_7	LCD_SEG7	LCD_SEG7	LCD_SEG7

Port Q

Port Q is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel4.q	1	2
Q_0	PIOA_8	LCD_SEG8
Q_1	PIOA_9	LCD_SEG9
Q_2	PIOA_10	LCD_SEG10
Q_3	PIOA_11	LCD_SEG11
Q_4	PIOA_12	LCD_SEG12
Q_5	PIOA_13	LCD_SEG13
Q_6	PIOA_14	LCD_SEG14
Q_7	PIOA_15	LCD_SEG15

Port R

Port R is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel4.r	1	2	3	4
R_0	PIOB_0	LCD_SEG16	USRA_RX_CLK_OUT	USRA_RX_CLK_OUT
R_1	PIOB_1	LCD_SEG17	USRA_TX_CLK_OUT	USRA_TX_CLK_OUT
R_2	PIOB_2	LCD_SEG18	USRA_DATA_OUT	USRA_DATA_OUT
R_3	PIOB_3	LCD_SEG19	USRA_DATA0_IN	USRA_DATA0_IN
R_4	PIOB_4	LCD_SEG20	USRA_DATA1_IN	USRB_RX_CLK_OUT
R_5	PIOB_5	LCD_SEG21	USRA_DATA2_IN	USRB_TX_CLK_OUT
R_6	PIOB_6	LCD_SEG22	USRA_RX_CLK_IN	USRB_DATA_OUT
R_7	PIOB_7	LCD_SEG23	USRA_TX_CLK_IN	USRB_DATA0_IN

port.sel4.r	5	6	7
R_0	CAP_TRIG1	CAP_TRIG1	MCPWM1
R_1	CAP_TRIG2	CAP_TRIG2	MCPWM2
R_2	CAP_TRIG3	CAP_TRIG3	MCPWM3
R_3	CAP_TRIG4	CAP_TRIG4	MCPWM4
R_4	CAP_TRIG5	CNT1_TRIG	MCPWM5
R_5	CAP_TRIG6	CNT2_TRIG	MCPWM6
R_6	CNT1_TRIG	PWM1	PWM1
R_7	PWM1	PWM2	PWM2

Port S

Port S is available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

port.sel5.s	1	2	3	4
S_0	PIOB_8	LCD_SEG24	I2S_SCLK	USRB_RX_CLK_OUT
S_1	PIOB_9	LCD_SEG25	I2S_WS	USRB_TX_CLK_OUT
S_2	PIOB_10	LCD_SEG26	I2S_SD_OUT	USRB_DATA_OUT
S_3	PIOB_11	LCD_SEG27	I2S_SD_IN	USRB_DATA0_IN
S_4	PIOB_12	LCD_SEG28	I2S_ALT_CLK_IN	USRB_DATA1_IN
S_5	PIOB_13	LCD_SEG29	I2S_MCLK	USRB_DATA2_IN
S_6	PIOB_14	LCD_SEG30	UART1A_TX	USRB_RX_CLK_IN
S_7	PIOB_15	LCD_SEG31	UART1A_RX	USRB_TX_CLK_IN

port.sel5.s	5	6	7	8	9
S_0	USRA_RX_CLK_OUT	UART1A_TX	CAP_TRIG1	CAP_TRIG1	MCPWM1
S_1	USRA_TX_CLK_OUT	UART1A_RX	CAP_TRIG2	CAP_TRIG2	MCPWM2
S_2	USRA_DATA_OUT	UART1B_TX	CAP_TRIG3	CAP_TRIG3	MCPWM3
S_3	USRA_DATA0_IN	UART1B_RX	CAP_TRIG4	CAP_TRIG4	MCPWM4
S_4	USRB_RX_CLK_OUT	UART2A_TX	CAP_TRIG5	CNT1_TRIG	MCPWM5
S_5	USRB_TX_CLK_OUT	UART2A_RX	CAP_TRIG6	CNT2_TRIG	MCPWM6
S_6	USRB_DATA_OUT	UART2B_TX	CNT1_TRIG	PWM1	PWM1
S_7	USRB_DATA0_IN	UART2B_RX	CNT2_TRIG	PWM2	PWM2

Port T

Port T is available on the following eCOG1X device variants:
eCOG1X0A, 1A, 8A and 9A in the 68QFN package.
eCOG1X10B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

port.sel5.t	1	2	3	4	5	6	7
T_0	PWM1	I2C_SCL	I2C_SCL	IR_RX	ESPI_SCLK	I2S_SCLK	UART2A_TX
T_1	PWM2	I2C_SDA	I2C_SDA	IR_TX	ESPI_MOSI	I2S_WS	UART2A_RX
T_2	I2S_ALT_CLK_IN	UART_TX	IR_RX	UART_TX	ESPI_MISO	I2S_SD_OUT	UART2B_TX
T_3	I2S_MCLK	UART_RX	IR_TX	UART_RX	ESPI_CS0	I2S_SD_IN	UART2B_RX

port.sel5.t	8	9	10	11	12	13
T_0	CNT1_TRIG	CAP1_TRIG	CNT1_TRIG	CNT1_TRIG	MCPWM4	SPI_CS1
T_1	CNT2_TRIG	CAP2_TRIG	CNT2_TRIG	CAP1_TRIG	MCPWM5	USB_OTG_DISCHRGVBUS
T_2	PWM1	PWM1	CAP1_TRIG	PWM1	MCPWM6	I2S_ALT_CLK_IN
T_3	PWM2	PWM2	CAP2_TRIG	PWM2	PWM2	I2S_MCLK

Peripheral Routing Options

The eCOG1X device pins are connected to 19 I/O ports labelled A to T. Different peripheral functions can be mapped to these ports to define the operation of each pin. This section lists the available routing options for each peripheral function. For further information on configuring the I/O ports, see the eCOG1X User Manual.

GPIO

The GPIO signals are not routed through the port multiplexer. They are always assigned to their specific port pin.

PIO

PIOA_0-7 are available on the following eCOG1X device variants:
eCOG1X0A, 4A and 8A in the 68QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

PIOA_8-15 are available on the following eCOG1X device variants:
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

PIOB_0-7 and PIOB_8-15 are available on the following eCOG1X device variants:
eCOG1X10Z and 14Z in the 208BGA package.

Peripheral	Signals	Ports	
PIOA	PIOA_0-7	N_0-7	P_0-7
	PIOA_8-15	M_0-7	Q_0-7
PIOB	PIOB_0-7	R_0-7	
	PIOB_8-15	S_0-7	

DUART

Peripheral	Signals	Ports								
UART1A	UART1A_TX	A_0		C_0	E_0	L_0	M_0	S_0	S_6	
	UART1A_RX	A_1		C_1	E_1	L_1	M_1	S_1	S_7	
UART1B	UART1B_TX	A_2		C_2	E_2	L_2	M_2	S_2		
	UART1B_RX	A_3		C_3	E_3	L_3	M_3	S_3		
UART2A	UART2A_TX	A_4	A_6		E_4		M_4	S_4		T_0
	UART2A_RX	A_5	A_7		E_5		M_5	S_5		T_1
UART2B	UART2B_TX	A_6			E_6		M_6	S_6		T_2
	UART2B_RX	A_7			E_7		M_7	S_7		T_3

DUSART

The routing options for the DUSART peripheral functions are listed in the tables below.

UART

Peripheral	Signals	Ports						
UART	UART_TX	C_2	D_2	F_2	J_2	K_2	L_2	T_2
	UART_RX	C_3	D_3	F_3	J_3	K_3	L_3	T_3

SPI

Peripheral	Signals	Ports							
SPI	SPI_SCLK	B_0	C_0	D_0		K_0			
	SPI_MOSI	B_1	C_1	D_1		K_1			
	SPI_MISO	B_2	C_2	D_2		K_2			
	SPI_CS0	B_3	C_3	D_3	D_0	K_3			
	SPI_CS1	B_4			D_1		K_0		T_0
	SPI_CS2	B_5			D_2				
	SPI_CS3	B_6			D_3				
SPI (modified)	SPI_SCLK_OUT							N_0	
	SPI_SCLK_IN							N_1	
	SPI_CS0_OUT							N_2	
	SPI_CS0_IN							N_3	
	SPI_DATA_IN							N_4	
	SPI_DATA_OUT							N_5	

I^2C

Peripheral	Signals	Ports							
I^2C	I2C_SCL	C_0	D_0	F_0	J_0	K_0	L_0	N_6	T_0
	I2C_SDA	C_1	D_1	F_1	J_1	K_1	L_1	N_7	T_1

Smart Card Interface (SCI)

Peripheral	Signals	Ports	
SCI	SC_CLK_EN	E_0	N_0
	SC_RESET	E_1	N_1
	SC_PWR_EN	E_2	N_2
	SC_CARD_IN	E_3	N_3
	SC_DATA	E_4	
	SC_DATA_IN		N_4
	SC_DATA_OUT		N_5

Infra Red (IFR)

Peripheral	Signals	Ports						
IR	IR_IN	C_0	D_0	F_0	J_0	K_0	L_0	T_0
		C_2	D_2	F_2	J_2	K_2	L_2	T_2
	IR_OUT	C_1	D_1	F_1	J_1	K_1	L_1	T_1
		C_3	D_3	F_3	J_3	K_3	L_3	T_3

User Serial Port (USR)

Peripheral	Signals	Ports							
USRA	USRA_RX_CLK_OUT	A_0		B_0	E_0	M_0	N_0	R_0	S_0
	USRA_TX_CLK_OUT	A_1		B_1	E_1	M_1	N_1	R_1	S_1
	USRA_DATA_OUT	A_2		B_2	E_2	M_2	N_2	R_2	S_2
	USRA_DATA0_IN	A_3		B_3	E_3	M_3	N_3	R_3	S_3
	USRA_DATA1_IN	A_4			E_4	M_4	N_4	R_4	
	USRA_DATA2_IN	A_5			E_5	M_5	N_5	R_5	
	USRA_RX_CLK_IN	A_6			E_6	M_6	N_6	R_6	
	USRA_TX_CLK_IN	A_7			E_7	M_7	N_7	R_7	
USRB	USRB_RX_CLK_OUT	A_4	B_0	B_4	E_4	M_4	N_4	R_4	S_0
	USRB_TX_CLK_OUT	A_5	B_1	B_5	E_5	M_5	N_5	R_5	S_1
	USRB_DATA_OUT	A_6	B_2	B_6	E_6	M_6	N_6	R_6	S_2
	USRB_DATA0_IN	A_7	B_3	B_7	E_7	M_7	N_7	R_7	S_3
	USRB_DATA1_IN		B_4						S_4
	USRB_DATA2_IN		B_5						S_5
	USRB_RX_CLK_IN		B_6						S_6
	USRB_TX_CLK_IN		B_7						S_7

Timers

Peripheral	Signals	Ports									
CNT1	CNT1_TRIG	B_4	B_6	C_0	E_4	E_6	R_4	R_6	S_4	S_6	T_0
CNT2	CNT2_TRIG	B_5		C_1	E_5		R_5		S_5	S_7	T_1
PWM1	PWM1	B_6	C_2	E_5	E_7	R_6	S_6	T_0	T_2		
		B_7	C_3	E_6		R_7					
PWM2	PWM2	B_7	C_3	E_5	E_7	R_7	S_7	T_1	T_3		

Peripheral	Signals	Ports			
CAP	CAP_TRIG1	B_5	T_1		
	CAP_TRIG1-2	C_0-1	C_2-3	T_0-1	T_2-3
	CAP_TRIG1-4	B_0-3	E_0-3	R_0-3	S_0-3
	CAP_TRIG1-6	B_0-5	E_0-5	R_0-5	S_0-5

External Memory Interface (EMI)

EMI_D0-7, EMI_A0-7 and EMI_CS0, CS1, RW_RS and DS0_WS0 are available on all eCOG1X devices in all packages. This subset of the EMI signals supports an 8-bit data bus and an 8-bit address bus, sufficient for memory mapped external peripherals.

The full set of signals for the EMI peripheral is available only on eCOG1X devices in the 208BGA package.

Peripheral	Signals	Ports	
EMI	EMI_D0-D7	A_0-7	H_0-7
	EMI_D8-15/A16-A23		I_0-7
	EMI_A0-A7	E_0-7	E_0-7
	EMI_A8-11		F_0-3
	EMI_A12-13 EMI_A14_DQML EMI_A15_DQMH		G_0-1 G_2 G_3
	EMI_CS0	D_0	D_0
	EMI_CS1	D_1	D_1
	EMI_RW_RS_WEN	D_2	D_2
	EMI_DS0_WS0_CAS	D_3	D_3
	EMI_DS1_WS1_RAS		J_0
	EMI_CKE		J_1
	EMI_WAIT		J_2
	EMI_CLK		J_3

External Host Interface (EHI)

The EHI peripheral is available only on eCOG1X devices in the 208BGA package.

Peripheral	Signals	Ports
EHI	EHI_D0-7	E_0-7
	EHI_D8-11	F_0-3
	EHI_D12-15	G_0-3
	EHI_D16-23	H_0-7
	EHI_D24-26 EHI_D27-31/A3-7	I_0-7
	EHI_REQ	D_0
	EHI_ACK	D_1
	EHI_RW	D_2
	EHI_CS	D_3
	EHI_WAIT	J_0
	EHI_A0-2	J_1-3

USB Interface

The USB peripheral is available on the following eCOG1X device variants:
eCOG1X4A and 5A in the 68QFN package (no ULPI).
eCOG1X14B in the 100QFN package.
eCOG1X14Z in the 208BGA package.

The on-chip USB PHY connections are dedicated and not controlled by the port multiplexer.

On-The-Go

Peripheral	Signals	Ports						
USB_OTG	USB_OTG_VBUSVALID	B_0	C_0		E_0		M_0	
	USB_OTG_AVALID	B_1	C_1		E_1		M_1	
	USB_OTG_BVALID	B_2		D_0	E_2		M_2	
	USB_OTG_SESSEND	B_3	C_2	D_1	E_3		M_3	
	USB_OTG_IDDIG	B_4			E_4		M_4	
	USB_OTG_IDPULLUP	B_5			E_5		M_5	
	USB_OTG_DRVVBUS	B_6	C_3		E_6		M_6	
	USB_OTG_CHRGVBUS	B_7		D_2	E_7		M_7	
	USB_OTG_DISCHRGVBUS			D_3		K_1		T_1

ULPI

Peripheral	Signals	Ports
USB_ULPI	USB_ULPI_RST	C_0
	USB_ULPI_DIR	C_1
	USB_ULPI_NXT	C_2
	USB_ULPI_STOP	C_3
	USB_ULPI_DATA0-7	M_0-7

Ethernet MAC

The Ethernet MAC peripheral is available on the following eCOG1X device variants:
eCOG1X8A and 9A in the 68QFN package.
eCOG1X10B and 14B in the 100QFN package.
eCOG1X10Z and 14Z in the 208BGA package.

Peripheral	Signals	Ports
EMAC	EMAC_TXD0-3	A_0-3
	EMAC_RXD0-3	A_4-7
	EMAC_CLKT	B_0
	EMAC_CLKR	B_1
	EMAC_RXER	B_2
	EMAC_RXDV	B_3
	EMAC_COL	B_4
	EMAC_CRS	B_5
	EMAC_TXEN	B_6
	EMAC_TXER	B_7

ESPI

Peripheral	Signals	Ports		
ESPI	ESPI_SCLK	B_0	E_0	T_0
	ESPI_MOSI	B_1	E_1	T_1
	ESPI_MISO	B_2	E_2	T_2
	ESPI_CS0	B_3	E_3	T_3
	ESPI_CS1	B_4	E_4	
	ESPI_CS2	B_5	E_5	
	ESPI_CS3	B_6	E_6	

I^2S

Peripheral	Signals	Ports			
I^2S	I2S_SCLK	B_0	C_0	S_0	T_0
	I2S_WS	B_1	C_1	S_1	T_1
	I2S_SD_OUT	B_2	C_2	S_2	T_2
	I2S_SD_IN	B_3	C_3	S_3	T_3
	I2S_ALT_CLK_IN	B_4	T_2	S_4	
	I2S_MCLK	B_5	T_3	S_5	

LCD Controller

Signals	Ports										
SEG0-3				K_0-3							
SEG0-7	A_0-7							P_0-7			
COM0 SEG1-7	A_0 A_1-7							P_0 P_1-7			
COM0-1 SEG2-7								P_0-1 P_2-7			
COM0-3 SEG4-7	A_0-3 A_4-7										
COM0	A_5										
COM0-3				K_0-3	L_0-3						
SEG8-15		B_0-7							Q_0-7		
COM0 SEG9-15		B_0 B_1-7									
COM0-3 SEG12-15		B_0-3 B_4-7									
SEG16-23			E_0-7							R_0-7	
SEG24-27					L_0-3						
SEG24-31						M_0-7					S_0-7
COM0-3 SEG28-31							N_0-3 N_4-7				

Motor Control PWM

Peripheral	Signals	Ports					
MCPWM	MCPWM1-6	B_0-5		E_0-5	R_0-5	S_0-5	
	MCPWM1-3		C_0-2				
	MCPWM4-6						T_0-2

Dual Smart Card Interface (DSCI)

Peripheral	Signals	Ports					
SCA	SCA_CLK	A_0	E_0	K_0		M_0	N_5
	SCA_RESET	A_1	E_1	K_1		M_1	N_6
	SCA_PWR_EN	A_2	E_2	K_2		M_2	N_7
	SCA_CARD_IN	A_3	E_3	K_3	L_1	M_3	
	SCA_DATA	A_4			L_0	M_4	
	SCA_DATA_IN		E_4				
	SCA_DATA_OUT		E_5				

Peripheral	Signals	Ports					
SCB	SCB_CLK	B_0	E_0		M_5	N_0	N_0
	SCB_RESET	B_1	E_1		M_6	N_1	N_1
	SCB_PWR_EN	B_2	E_2		M_7	N_2	N_2
	SCB_CARD_IN	B_3	E_3	L_3		N_3	N_3
	SCB_DATA	B_4	E_4	L_2		N_4	
	SCB_DATA_IN						N_4
	SCB_DATA_OUT						N_5

Analogue I/O

The ADC and DAC peripheral signals are dedicated and are not controlled by the port multiplexer. Different subsets of the analogue signals are available on different device variants and packages, as shown in the table below.

Peripheral	Signals	Device variants			
		0A, 4A, 8A	1A, 5A, 9A	10B, 14B	10Z, 14Z
ADC1	ADC1_Vin1				Yes
	ADC1_Vin2		Yes	Yes	Yes
	ADC1_Vin3		Yes	Yes	Yes
	ADC1_Vin4			Yes	Yes
	ADC1_Vin5			Yes	Yes
	ADC1_Vin6			Yes	Yes
	ADC1_Vin7			Yes	Yes
ADC2	ADC2_Vin1				Yes
	ADC2_Vin2		Yes	Yes	Yes
	ADC2_Vin3		Yes	Yes	Yes
	ADC2_Vin4			Yes	Yes
	ADC2_Vin5			Yes	Yes
	ADC2_Vin6			Yes	Yes
	ADC2_Vin7				Yes
DAC	DAC1		Yes	Yes	Yes
	DAC2		Yes	Yes	Yes

Applications Information

Connections

For normal operation, the following recommendations should be observed in the hardware design.

- The external quartz crystal used with the 8MHz high reference oscillator requires two load capacitors. The maximum load capacitance value for the high reference oscillator is 32pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 22pF. Higher load capacitor values increase slightly the power consumption of the oscillator circuit.

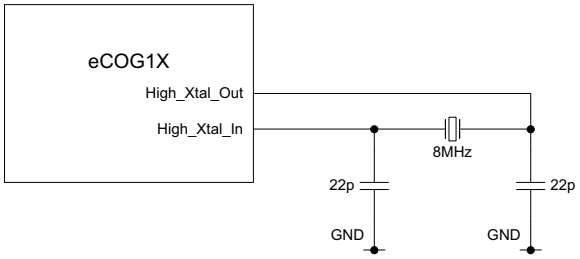


Figure 2: High reference oscillator external components

- If an external clock source is used instead of the 8MHz quartz crystal oscillator, then High_XTAL_Out is not connected and the external clock signal is connected to High_XTAL_In. If the high reference clock is not required, then High_XTAL_Out is not connected and High_XTAL_In is connected to AGND via a 10kΩ resistor.
- The external quartz crystal used with the 32.768kHz low reference oscillator requires two load capacitors. The maximum load capacitance value for the low reference oscillator is 25pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 10pF. Higher load capacitor values increase slightly the power consumption of the oscillator circuit.

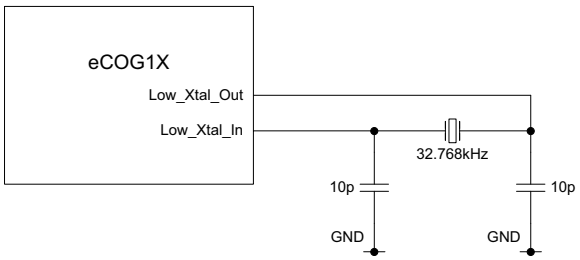


Figure 3: Low reference oscillator external components

- If an external clock source is used instead of the 32.768kHz quartz crystal oscillator, then Low_XTAL_Out is not connected and the external clock signal is connected to Low_XTAL_In. If the low reference clock is not required, then Low_XTAL_Out is not connected and Low_XTAL_In is connected to AGND via a 10kΩ resistor.
- On smaller package variants (68QFN, 100QFN), the nReset pin is bidirectional. It is driven low internally as an open-collector output by the on-chip power-on reset supply voltage sense circuit, and is also connected as an input to the device from the pin. This allows the use of an external reset circuit if required. The nReset input has a Schmitt trigger input circuit.
- On larger package variants (208BGA), the nReset_Out and nReset_In pins are not connected internally. This allows the use of an external reset circuit if required. A power-on reset signal must be connected to nReset_In (active low) for correct operation of the device, either from the internal reset circuit or from an external power-on reset circuit. To use the internal power-on reset circuit, connect nReset_Out to nReset_In, either directly or via external logic for any additional external reset source such as a pushbutton switch. The nReset_In input has a Schmitt trigger input circuit and an internal pull-up resistor. The nReset_Out output is open-drain with an internal pull-up resistor, and can be used in a wired-OR connection with an external power-on reset if the external device also has an active-low open-drain output.

- Applications using the analogue inputs or outputs with the internal reference voltage must have external decoupling capacitors connected to the Vref pin. The recommended decoupling on this pin is a 100nF ceramic capacitor in parallel with a 4.7µF low ESR electrolytic capacitor.

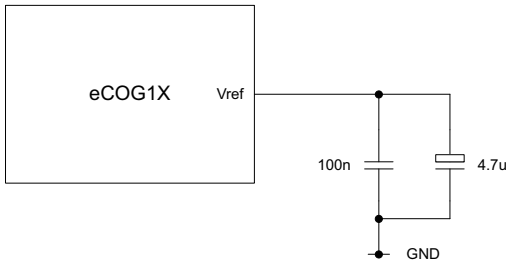


Figure 4: Vref decoupling

- The low frequency PLL requires external low pass filter components connected to the FIL pin, as shown. The filter consists of a 2.2nF capacitor from FIL to AGND, in parallel with a 68nF capacitor and an 8.2kΩ resistor in series.

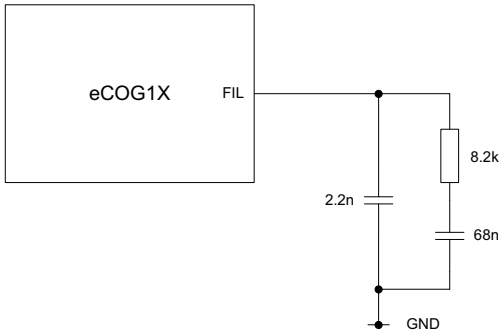


Figure 5: Low PLL filter external components

- The Rext pin for the external resistor to set the frequency of the relaxation oscillator is available only on the 208BGA package. On devices in this package, the relaxation oscillator frequency can be adjusted over a range from 1MHz to 11MHz by changing the value of an external resistor connected from the Rext pin to GND. In the smaller 68QFN and 100QFN packages, the relaxation oscillator runs at the frequency corresponding to an open circuit at the Rext pin with the external resistor not fitted, nominally 1MHz.
- The ULPI_CLK input should be pulled low or tied to GND if the ULPI high-speed USB connection is not used.
- The nTest pin is not used in normal applications and should be connected to VDD, either directly or via a 100kΩ pull-up resistor.

- The eICE_LOADB pin must be connected to VDD via a 100kΩ pull-up resistor for normal operation when the eICE debug port is not in use or disconnected. When the eICE port is used for debugging, a 4.7kΩ pull-up resistor is required. If the system is used with an external eICE programming adaptor, then the external adaptor has the 4.7kΩ pull-up resistor fitted, and the target system only needs a 100kΩ pull-up resistor connected to this signal.
  It is also recommended that the eICE input signals (eICE_CLK, eICE_MOSI) are connected to GND via 100kΩ pull-down resistors as a precaution against noise.

  The target system circuit board must make the eICE debug port connections available for software development, debugging and downloading into flash memory. Usually these signals are brought to a connector or pin header. A 10-way boxed header is preferred, as this provides mechanical polarisation and is compatible with the Cyan USB eICE debug adaptor. Suggested connections for this 10-way header on an eCOG1X target system are shown in the diagram below.

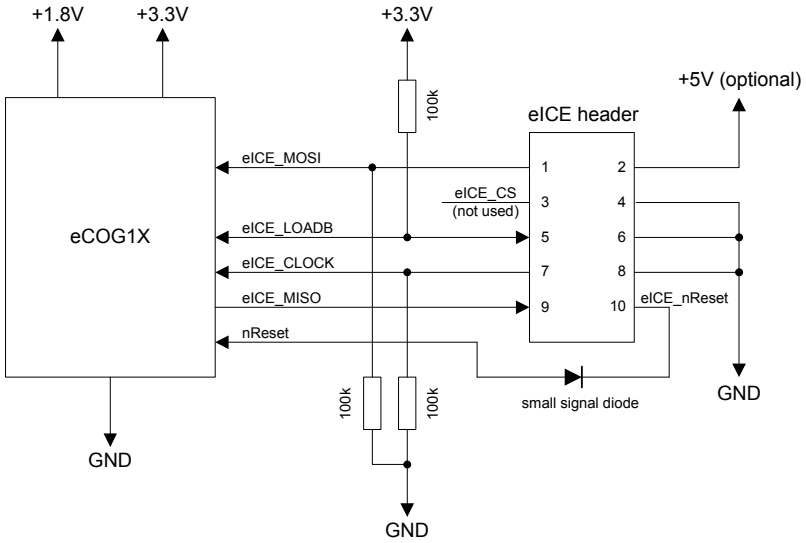


Figure 6: eICE debug header connections

- The VPP pin is used with a higher voltage supply to support faster programming of the internal flash memory via JTAG. If this function is not required, then the VPP pin should be connected to GND to minimise power consumption in normal operation. If this function is required, then connect VPP to GND via a pull-down resistor or jumper link so that the fast programming supply can be connected.
- NC indicates a No Connect. Any pins labelled as NC should not be connected in circuit.
- All digital input pins and bidirectional port pins have Schmitt trigger input circuits.

For low power operation, note the following additional recommendations.

- The EMI data bus pins float as inputs in the sleep state and can cause higher than expected power consumption. If minimum power consumption in the sleep state is required, connect all the EMI data bus pins to GND or to VDD via 100kΩ resistors.
- Similarly, all unused port input pins should be connected to GND or to VDD via 100kΩ resistors to prevent them floating.

Power Supplies and Decoupling

It is recommended that VDD, IVDD and GND are implemented as power and ground planes in the printed circuit board. The analogue power supply connections to the AVDD and AGND pins should be routed directly to separate power and ground connections, they should not share circuit tracks with any of the digital power supply connections. An ideal board layout should provide split power and ground plane areas to separate the digital 3.3V, 1.8V and analogue power supplies.

Decoupling capacitors must be fitted on both the digital and analogue power supplies. The digital power supply connections should have at least one 100nF capacitor for every two power pins, located close to these pins. Ideally there should be one 100nF decoupling capacitor for each power pin. The analogue power supplies should be decoupled separately with two 100nF capacitors in parallel, located as close as possible to the AVDD and AGND pins. All these decoupling capacitors should be low ESR ceramic types.

Additional bulk decoupling is required somewhere on the hardware design. At least one 10uF low ESR tantalum or aluminium electrolytic capacitor is required on each power supply, usually located at the power supply input connections or at the output of any power supply regulator. For larger designs it is recommended that multiple capacitors are fitted; these should be distributed around the circuit board.

For further filtering on the analogue power supply AVDD, connect a ferrite bead in series with the analogue supply input, between the 1.8V digital power supply and the analogue supply decoupling capacitors. A suitable surface mount ferrite bead is the EPCOS B82496C3100J (inductance 10nH, 500mA, 0.3Ω DC resistance, 0603 package) available from Farnell Electronic Components (order number 387-7024). Similarly, the USBVDD power supply pin should be decoupled separately with a 100nF capacitor and should have a series ferrite bead for filtering.

If the cost of a multilayer circuit board is too high for the target system and the layout is implemented without power and ground planes, then care must be taken to minimise the series impedance in the power and ground connections. Keep the power and ground tracks as short and as wide as possible, and locate the decoupling capacitors as close as possible to the package power pins. Route separate power and ground tracks from the power supply input connection to the ferrite beads and then to the decoupling capacitors for the analogue power and ground pins AVDD and AGND, and make sure that the decoupling capacitors are located as close as possible to these pins.

Electrical Characteristics

Recommended Operating Conditions

Except where otherwise specified, eCOG1X meets all operating specifications when operated within these limits.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Operating temperature		–40		+85	°C
IV_{DD}	Core supply voltage	Relative to GND	1.65	1.8	1.95	V
V_{DD}	I/O supply voltage	Relative to GND	3.0	3.3	3.6	V
AV_{DD}	Analogue supply voltage	Relative to AGND	1.62	1.8	1.98	V
V_{PP}	Fast programming voltage	Relative to GND	0		10.5	V
V_{IN}	Voltage on any digital I/O pin	3.3V pins	–0.5		V_{DD} + 0.3	V
		5V tolerant pins	–0.5		V_{DD} + 1.9	V
AV_{IN}	Voltage on any analogue pin		AGND – 0.3		AV_{DD} + 0.3	V

Table 18: Recommended operating conditions

Absolute Maximum Ratings

The eCOG1X device is not guaranteed to meet specification if it is operated outside the recommended operating conditions. In addition, exceeding these maximum operating parameters may cause permanent damage to the device.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Operating temperature		–40		+105	°C
IV_{DD}	Core supply voltage	Relative to GND	–0.5		2.0	V
V_{DD}	I/O supply voltage	Relative to GND	–0.5		3.7	V
AV_{DD}	Analogue supply voltage	Relative to AGND	–0.5		2.0	V
V_{IN}	Voltage on any digital I/O pin relative to GND	3.3V pins	–0.5		3.7	V
		5V tolerant pins	–0.5		5.5	V
AV_{IN}	Voltage on any analogue pin		–0.3		2.1	V
V_{ESD}	ESD protection	Human Body Model			2	kV
		Charge Device Model			500	V

Table 19: Absolute maximum ratings

Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	CPU Core	CPU clock frequency				
I_{CPU}	Supply current IV_{DD}	64MHz		33		mA
		48MHz		24		mA
		24MHz		12		mA
I_{SL}	Sleep Mode Current IV_{DD}	16kHz, clock source = low osc.		10		µA
I_{DS}	Deep Sleep	IV_{DD} (1.8V)		6		µA
		V_{DD} (3.3V)		3		µA
	High PLL					
I_{HP}	Supply current AV_{DD}	F_{IN} = 8.33MHz F_{OUT} = 16.66MHz		1.0		mA
		F_{IN} = 8.33MHz F_{OUT} = 416.66MHz	1.6	1.9	2.2	mA
		Disabled		0.013	5.0	µA
	High Reference Oscillator					
I_{HR}	Supply current AV_{DD}	Enabled, external clock		140		µA
		Enabled, 10MHz crystal, 32pF load capacitors			170	µA
		Disabled		0.5	65	nA
C_L	Load capacitor value			22	32	pF
	Relaxation Oscillator					
I_{RO}	Supply current AV_{DD}	R_{EXT} not fitted	1.15	2.51	6.24	µA
		R_{EXT} = 2.2MΩ	1.61	3.15	5.66	µA
		R_{EXT} = 150kΩ	13.0	20.5	35.6	µA
	Low PLL					
I_{LP}	Supply current AV_{DD}	F_{IN} = 32.768kHz F_{OUT} = 9.99MHz		104		µA
		Disabled		0.012	4.6	µA
	Low Reference Oscillator					
I_{LR}	Supply current AV_{DD}	Enabled, external clock	0.37	0.62	2.2	µA
		Enabled, 32kHz crystal, 25pF load capacitors			2.0	µA
		Disabled		0.2	43	nA
C_L	Load capacitor value			10	25	pF
	V_{REF}					
I_{REF}	Supply current AV_{DD}	Enabled	186	333	560	µA
		Disabled		2	340	nA
	ADC					
I_{ADC}	Supply current AV_{DD} (including V_{REF})	Enabled	368	598	1120	µA
		Disabled		0.013	6	µA
	DAC					
I_{DAC}	Supply current AV_{DD}	Enabled	62	85	103	µA
		Disabled		0.015	8	µA
	Power-On Reset					
I_{POR}	Supply current	AV_{DD} (1.8V)	0.81	1.27	2.22	µA
		V_{DD} (3.3V)	0.56	0.75	1.08	µA

Table 20: Supply current

DC Electrical Characteristics

Digital Inputs and Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Inputs					
V_{IL}	Input low voltage		–0.3		+0.8	V
V_{IH}	Input high voltage		2.0		V_{DD}+0.3	V
I_{OZ}	Input leakage current	GND–0.3V ≤ V_{IN} ≤ V_{DD}+0.3V			±5	µA
C_{IN}	Input capacitance				4.5	pF
	5V Tolerant Inputs [3]					
V_{IL}	Input low voltage		–0.3		+0.8	V
V_{IH}	Input high voltage		2.0		V_{DD}+1.9	V
I_{OZ}	Input leakage current	GND–0.3V ≤ V_{IN} ≤ V_{DD}+1.9V			±5	µA
C_{IN}	Input capacitance				4.5	pF
	2mA Outputs [1,2]					
V_{OL}	Output low voltage	I_{OL} = 2mA			0.2	V
V_{OH}	Output high voltage	I_{OH} = –2mA	V_{DD}–0.2			V
I_{OL}	Logic low output current	V_{OL} < 0.2V	2			mA
		V_{OL} = V_{DD}–0.45V	3	6	8	
I_{OH}	Logic high output current	V_{OH} > V_{DD}–0.2V	–2			mA
		V_{OH} = 0.45V	–5	–9	–10	
R_{PU}	Internal pull-up resistor		32	45	75	kΩ
	2mA 5V Tolerant Outputs [3]					
V_{OL}	Output low voltage	I_{OL} = 2mA			0.2	V
V_{OH}	Output high voltage	I_{OH} = –2mA	V_{DD}–0.2			V
I_{OL}	Logic low output current	V_{OL} < 0.2V	2			mA
		V_{OL} = V_{DD}–0.45V	3	6	8	
I_{OH}	Logic high output current	V_{OH} > V_{DD}–0.2V	–2			mA
		V_{OH} = 0.45V	–5	–9	–10	
R_{PU}	Internal pull-up resistor		29	40	68	kΩ
	4mA Outputs [4]					
V_{OL}	Output low voltage	I_{OL} = 4mA			0.2	V
V_{OH}	Output high voltage	I_{OH} = –4mA	V_{DD}–0.2			V
I_{OL}	Logic low output current	V_{OL} < 0.2V	4			mA
		V_{OL} = V_{DD}–0.45V	6	13	16	
I_{OH}	Logic high output current	V_{OH} > V_{DD}–0.2V	–4			mA
		V_{OH} = 0.45V	–10	–18	–23	
	Schmitt Trigger Inputs [5]					
V_{TH+}	Input threshold voltage (rising)		1.28	1.56	1.42	V
$V_{TH–}$	Input threshold voltage (falling)		0.91	1.12	1.26	V
ΔV	Hysteresis		160	360	430	mV

Table 21: DC characteristics - digital I/O

1 The following pins have 2mA output drive capability:
eICE_LOADB/JTMS, eICE_MISO/JTDO, nReset_Out.

2 The following pins have 2mA output drive capability and selectable internal pull-up resistors:
PortA_0-7, PortB_5-7, PortR_0-7, PortS_0-7, PortT_0-3.

3 The following pins have 2mA output drive capability, selectable internal pull-up resistors, and are 5V tolerant:
PortB_0-4, PortK_0-3, PortL_0-3, PortN_0-7, PortP_0-7, PortQ_0-7. The outputs must be disabled (tristated) or used in open-drain mode when signals above VDD are present on these pins.

4 The following pins have 4mA output drive capability:
PortC_0-3, PortD_0-3, PortE_0-7, PortF_0-3, PortG_0-3, PortH_0-7, PortI_0-7, PortJ_0-3, PortM_0-7.

5 The following input pins and bidirectional port pins have Schmitt trigger input circuits:
eICE_CLK/JTCLK, eICE_MOSI/JTDI, nReset_In, nReset, ULPI_CLK.

Analogue Inputs and Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{LIM}	Voltage on any analogue pin	Relative to AGND	–0.3		2.1	V
	ADC Inputs					
AV_{IN}	ADC input voltage range	Conversion data valid	0		V_{REF}	V
C_{IN}	Input capacitance	Sample/hold capacitor		30		pF
	DAC Outputs					
AV_{OL}	DAC output voltage	Data = 0x000			0.003	V
AV_{OH}	DAC output voltage	Data = 0xFFF	AV_{DD} – 0.003			V
Z_{OUT}	Output impedance	$V_{OUT} = V_{REF}$			500	Ω

Table 22: DC characteristics - analogue I/O

USB PHY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Input Levels					
V_{DI}	Differential input sensitivity	$\|(V_P – V_M)\|$	200			mV
V_{CM}	Common-mode voltage		0.8		2.5	V
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{HY}	Input hysteresis					mV
	Output Levels					
V_{OL}	Output low voltage	R_L = 1.5kΩ to USBVDD			0.3	V
V_{OH}	Output high voltage	R_L = 15kΩ to USBGND	2.8		3.6	V
	Termination					
Z_{OUT}	Output impedance [1]	Steady state drive	10		26	Ω
Z_{IN}	Input impedance		300			kΩ
	Leakage Current					
I_{OZ}	Off-state leakage current				±20	µA
	Pin Capacitance					
C_{IN}	Input capacitance				16	pF

Table 23: DC characteristics - USB PHY

1 To meet the USB specification requirements for the output impedance (28Ω to 44Ω), fit external 18Ω resistors in series with both the USB_p and USB_n data pins.

AC Electrical Characteristics

All signal timing information is given for output pin load capacitances of 30pF, unless specified otherwise.

Relaxation Oscillator

This table lists the performance characteristics of the relaxation oscillator over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{OSC}	Operating frequency	R_{EXT} not fitted	0.53	1.0	2.2	MHz
		R_{EXT} = 2.2MΩ	0.67	0.99	1.5	MHz
		R_{EXT} = 150kΩ	7.86	11.1	15.9	MHz
C_{OSC}	Duty cycle		45	50	55	%
T_{OSC}	Startup time	R_{EXT} not fitted	4.2	7.5	10.9	µs

Table 24: AC characteristics - relaxation oscillator

The Rext pin for the external resistor to set the frequency of the relaxation oscillator is available only on the 208BGA package. On devices in this package, the relaxation oscillator frequency can be adjusted over a range from 1MHz to 11MHz by changing the value of an external resistor connected from the Rext pin to GND. In the smaller 68QFN and 100QFN packages, the relaxation oscillator runs at the frequency corresponding to an open circuit at the Rext pin with the external resistor not fitted, nominally 1MHz.

Crystal Oscillators

This table lists the performance characteristics of the low and high frequency oscillators over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low Reference Oscillator					
F_{32k}	Operating frequency (32.768kHz crystal)	Combined crystal tolerance is ±150ppm worst case.	32.763	32.768	32.773	kHz
C_{32k}	Duty cycle	F_{32k} = 32.768kHz	45	50	55	%
T_{32k}	Startup time			500	600	ms
C_L	Load capacitor value			10	25	pF
	High Reference Oscillator					
F_{8M}	Operating frequency (8.0MHz crystal)	Combined crystal tolerance is ±50ppm worst case.	7.9996	8.000	8.0004	MHz
F_{HR}	Frequency range	With appropriate crystal.	5	8.0	10	MHz
C_{8M}	Duty cycle	F_{8M} = 8MHz	45	50	55	%
T_{8M}	Startup time			0.4	0.8	ms
C_L	Load capacitor value			22	32	pF

Table 25: AC characteristics - crystal oscillators

The crystal oscillator circuits require external load capacitors connected from both ends of the quartz crystal to GND, as shown in Applications Information. The recommended load capacitor values are 10pF for the low reference oscillator and 22pF for the high reference oscillator.

Phase Locked Loops (PLLs)

This table lists the performance characteristics of the low and high frequency phase locked loops over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low PLL					
F_{LK}	Lock range					kHz
T_{LK}	Lock time	Error < 1%		2	7	ms
	Duty cycle		45	50	55	%
T_J	Jitter			±170		ps
F_{VCO}	VCO frequency				50	MHz
F_{OUT}	PLL output frequency				9.99	MHz
	High PLL					
F_{LK}	Lock range					MHz
T_{LK}	Lock time	Error < 1%		10	19	µs
	Duty cycle		45	50	55	%
T_J	Jitter			±150		ps
F_{VCO}	VCO frequency				400	MHz
F_{OUT}	PLL output frequency				400	MHz

Table 26: AC characteristics - PLLs

The low frequency PLL requires external low pass filter components connected to the FIL pin, as shown in Applications Information. The filter consists of a 2.2nF capacitor from FIL to AGND, in parallel with a 68nF capacitor and an 8.2kΩ resistor in series.

External Clock Source

If an external clock source is used as the main system clock for the eCOG1X, the following parameters apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low reference clock input					
F_{LO}	Input frequency					MHz
	High reference clock input					
F_{HI}	Input frequency					MHz
	Input signal parameters					
t_{CKH}	Clock high time	Clock at 90% of V_{DD} or more	10			ns
t_{CKL}	Clock low time	Clock at 10% of V_{DD} or less	10			ns
t_R	Clock rise time	10% to 90%			100	ns
t_F	Clock fall time	90% to 10%			100	ns

Table 27: AC characteristics - external clock source

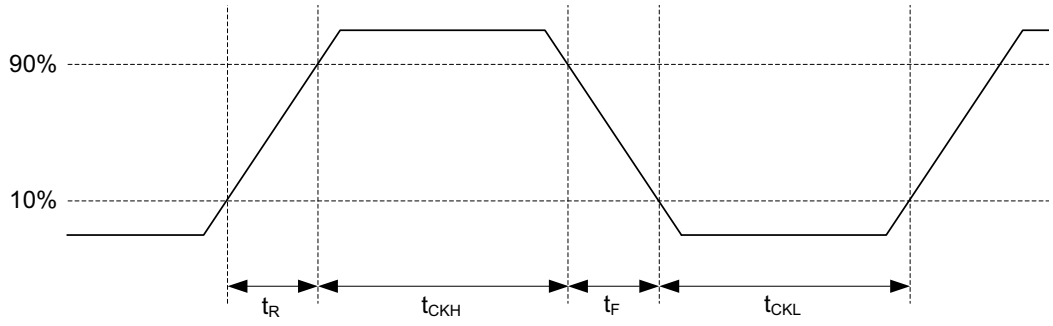


Figure 7: External clock source timing diagram

Digital Inputs and Outputs

The input pulse width specification applies to any input signal which is sampled by a peripheral of the chip. All inputs are clocked through synchroniser circuits to eliminate metastable data when reading input registers.

Output signal rise and fall times depend on the external load on each signal and the drive current capability of the output. Rise times are to 70% of VDD and fall times to 30% of VDD.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Inputs					
T_{Pmin}	Minimum pulse width	Peripheral sample clock period is T_S, determined by peripheral clock and prescaler configuration.	$3T_S$			sec
	2mA Outputs [1,2]					
t_R	Output rise time	C_L = 8pF			1.4	ns
		C_L = 16pF			2.1	ns
		C_L = 32pF			3.5	ns
		C_L = 64pF			6.4	ns
t_F	Output fall time	C_L = 8pF			1.1	ns
		C_L = 16pF			1.7	ns
		C_L = 32pF			2.7	ns
		C_L = 64pF			4.9	ns
t_{OE}	Output enable time			0.6	0.9	ns
t_{OD}	Output disable time			0.6	0.9	ns
	2mA 5V Tolerant Outputs [3]					
t_R	Output rise time	C_L = 8pF			1.7	ns
		C_L = 16pF			2.6	ns
		C_L = 32pF			4.5	ns
		C_L = 64pF			8.2	ns
t_F	Output fall time	C_L = 8pF			1.3	ns
		C_L = 16pF			2.0	ns
		C_L = 32pF			3.5	ns
		C_L = 64pF			6.4	ns
t_{OE}	Output enable time			0.6	0.9	ns
t_{OD}	Output disable time			0.6	0.9	ns
	4mA Outputs [4]					
t_R	Output rise time	C_L = 8pF			1.1	ns
		C_L = 16pF			1.5	ns
		C_L = 32pF			2.2	ns
		C_L = 64pF			3.6	ns
t_F	Output fall time	C_L = 8pF			1.0	ns
		C_L = 16pF			1.3	ns
		C_L = 32pF			1.8	ns
		C_L = 64pF			2.9	ns
t_{OE}	Output enable time			1.0	1.5	ns
t_{OD}	Output disable time			1.0	1.5	ns

Table 28: AC characteristics - digital I/O

1 The following pins have 2mA output drive capability:
eICE_LOADB/JTMS, eICE_MISO/JTDO, nReset_Out.

2 The following pins have 2mA output drive capability and selectable internal pull-up resistors:
PortA_0-7, PortB_5-7, PortR_0-7, PortS_0-7, PortT_0-3.

3 The following pins have 2mA output drive capability, selectable internal pull-up resistors, and are 5V tolerant:
PortB_0-4, PortK_0-3, PortL_0-3, PortN_0-7, PortP_0-7, PortQ_0-7. The outputs must be disabled (tristated) or used in open-drain mode when signals above VDD are present on these pins.

4 The following pins have 4mA output drive capability:
PortC_0-3, PortD_0-3, PortE_0-7, PortF_0-3, PortG_0-3, PortH_0-7, PortI_0-7, PortJ_0-3, PortM_0-7.

External Memory Interface (EMI)

EMI Clock

Symbol	Parameter	Min	Typ	Max	Units
f_{CK}	EMI_CLK frequency			149.7	MHz
C_{CK}	EMI_CLK duty cycle	45		55	%
t_R, t_F	EMI_CLK output rise and fall time	See Table 28			

Table 29: AC characteristics - EMI clock

Bus Mode

Symbol	Parameter	Min	Typ	Max	Units
t_{DS}	Setup time input data valid to EMI_CLK falling edge	5.0			ns
t_{DH}	Hold time EMI_CLK falling edge to input data invalid	0			ns
t_{WS}	Setup time EMI_WAIT input valid to EMI_CLK falling edge	4.8			ns
t_{WH}	Hold time EMI_CLK falling edge to EMI_WAIT input invalid	0			ns
t_{AV}	Delay time EMI_CLK rising edge to address outputs valid			3.6	ns
t_{AZ}	Delay time EMI_CLK rising edge to address outputs tristate			1.4	ns
t_{DV}	Delay time EMI_CLK rising edge to data outputs valid			3.6	ns
t_{DZ}	Delay time EMI_CLK rising edge to data outputs tristate			1.4	ns
t_{CO}	Delay time EMI_CLK rising edge to control signal output			2.8	ns

Table 30: AC characteristics - EMI bus mode

SDRAM Mode

Symbol	Parameter	Min	Typ	Max	Units
t_{DS}	Setup time input data valid to EMI_CLK rising edge	5.7			ns
t_{DH}	Hold time EMI_CLK rising edge to input data invalid	0			ns
t_{AV}	Delay time EMI_CLK rising edge to address outputs valid			3.6	ns
t_{AZ}	Delay time EMI_CLK rising edge to address outputs tristate			1.4	ns
t_{DV}	Delay time EMI_CLK rising edge to data outputs valid			3.6	ns
t_{DZ}	Delay time EMI_CLK rising edge to data outputs tristate			1.4	ns
t_{CO}	Delay time EMI_CLK rising edge to control signal output			2.8	ns

Table 31: AC characteristics - EMI SDRAM mode

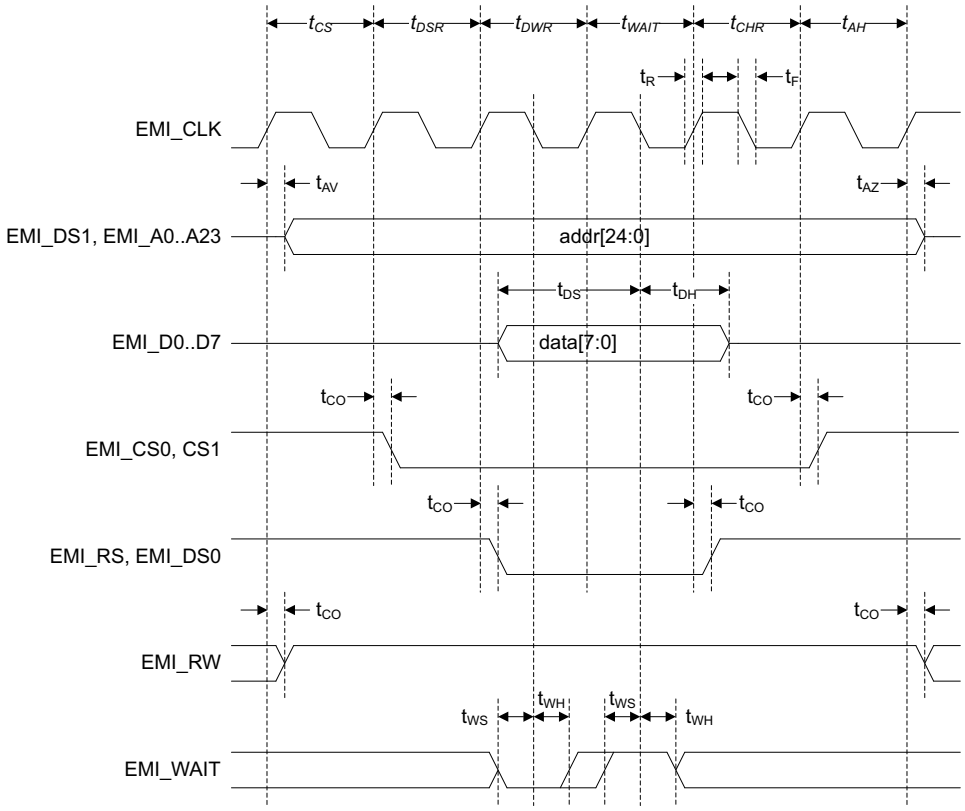


Figure 8: EMI bus mode 8-bit read cycle timing diagram

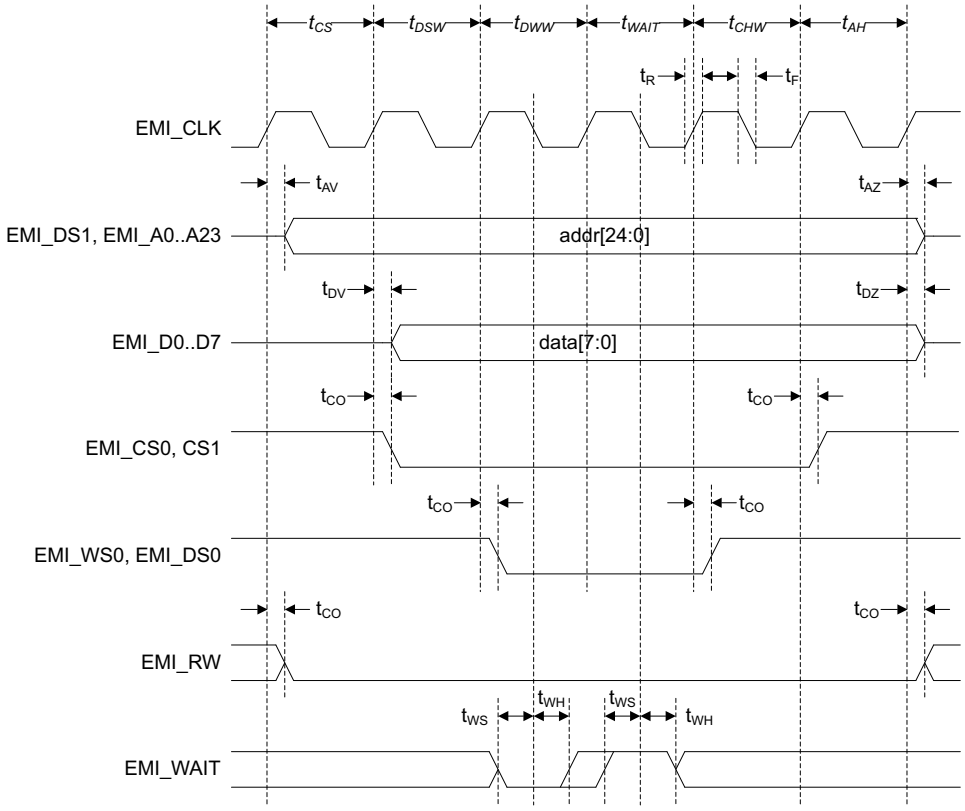


Figure 9: EMI bus mode 8-bit write cycle timing diagram

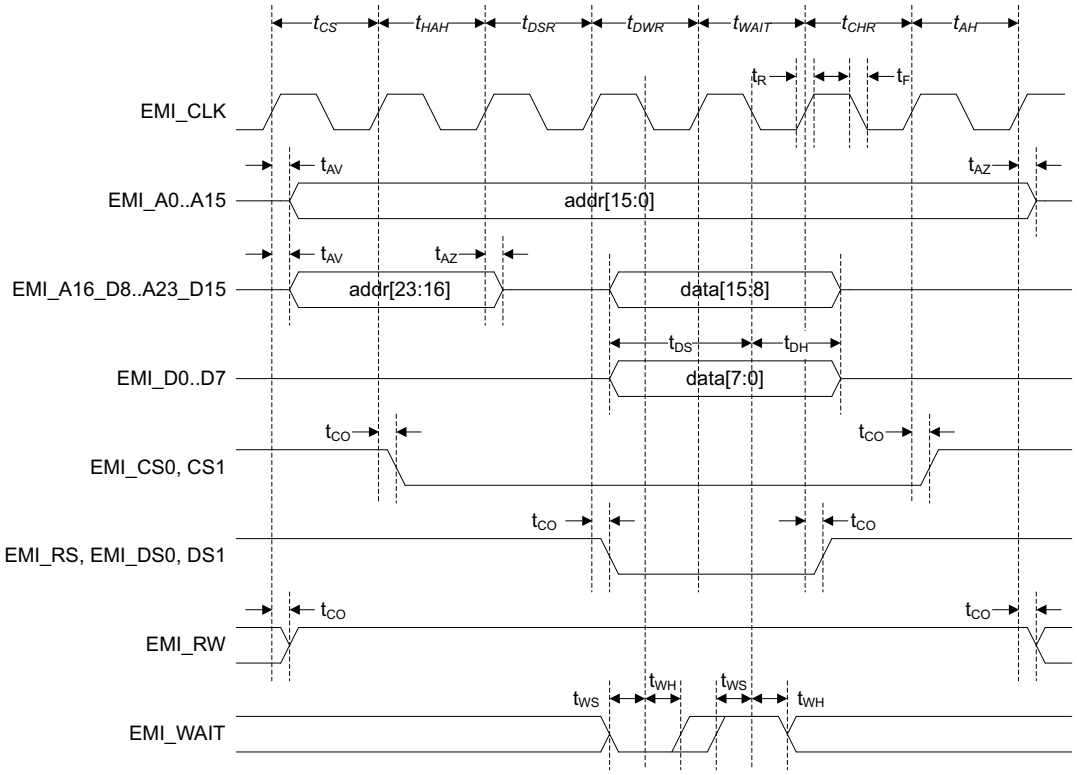


Figure 10: EMI bus mode 16-bit read cycle timing diagram

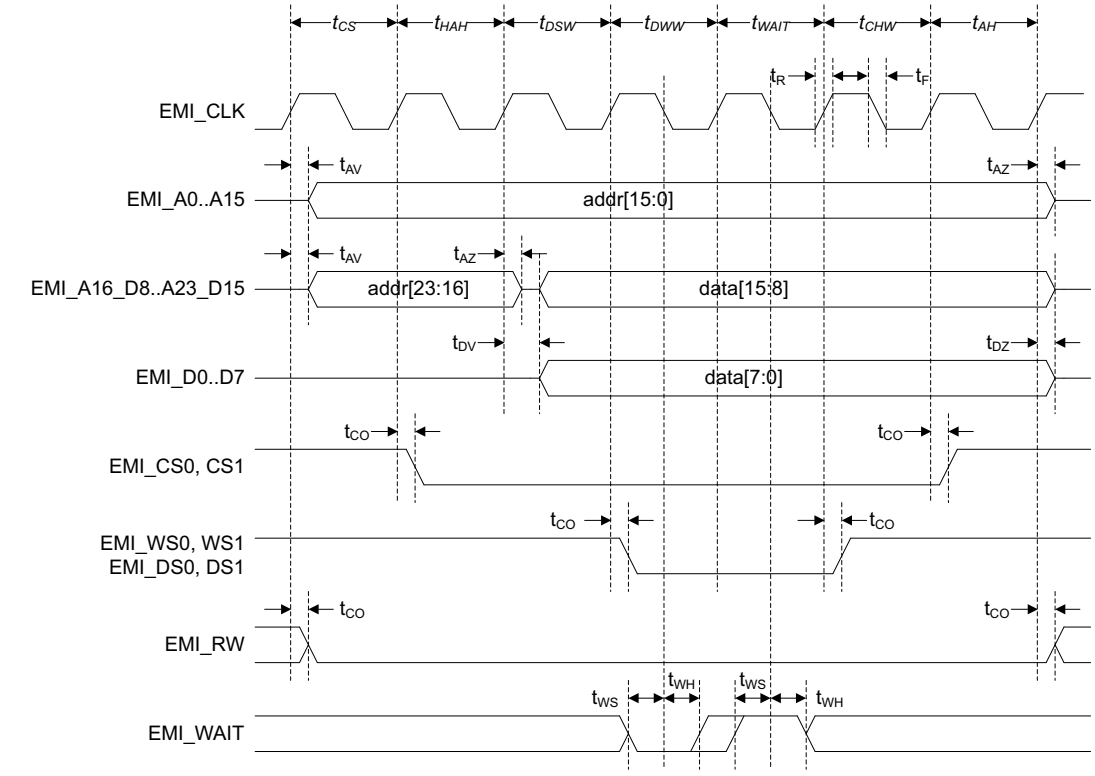


Figure 11: EMI bus mode 16-bit write cycle timing diagram

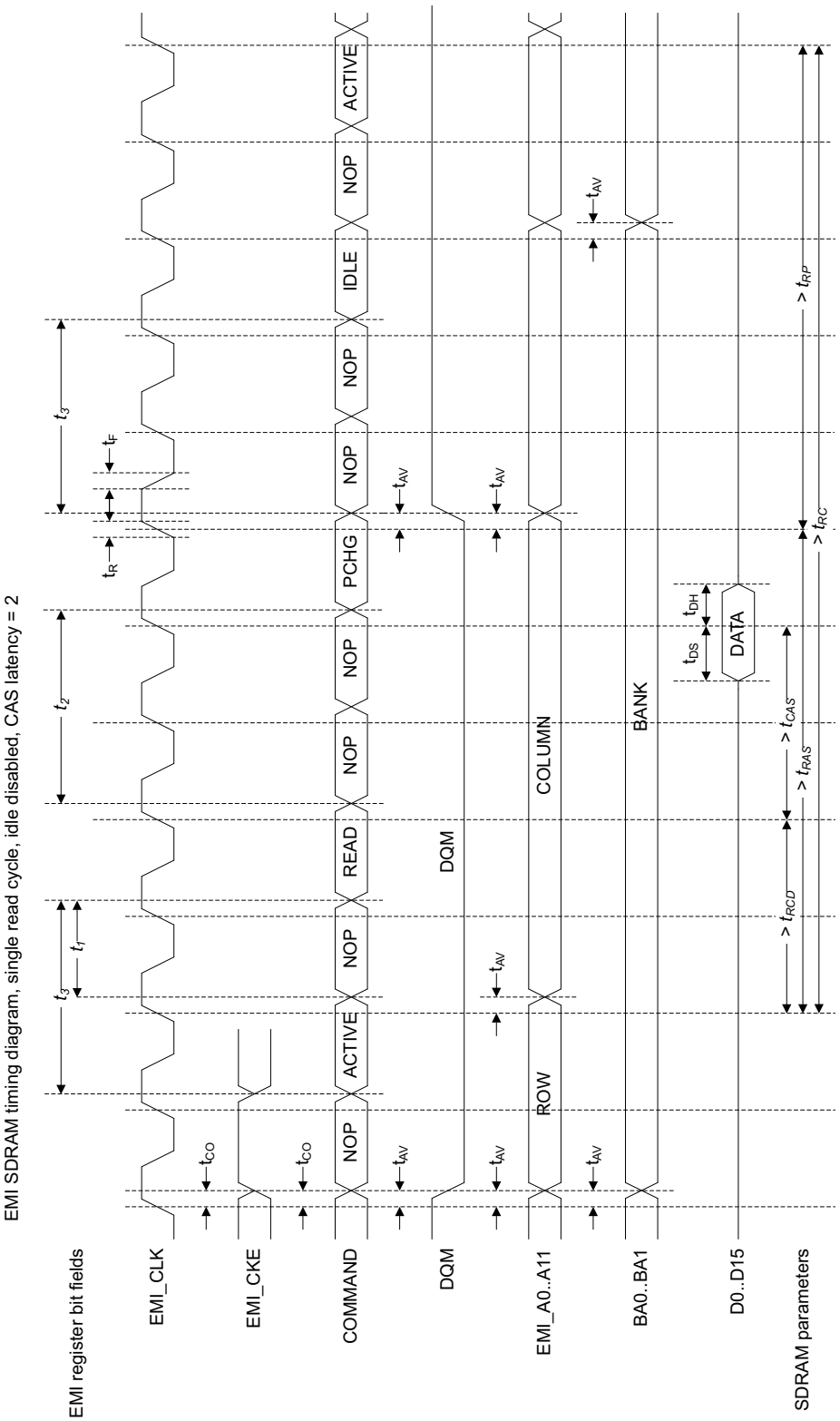


Figure 12: EMI SDRAM mode read cycle timing diagram

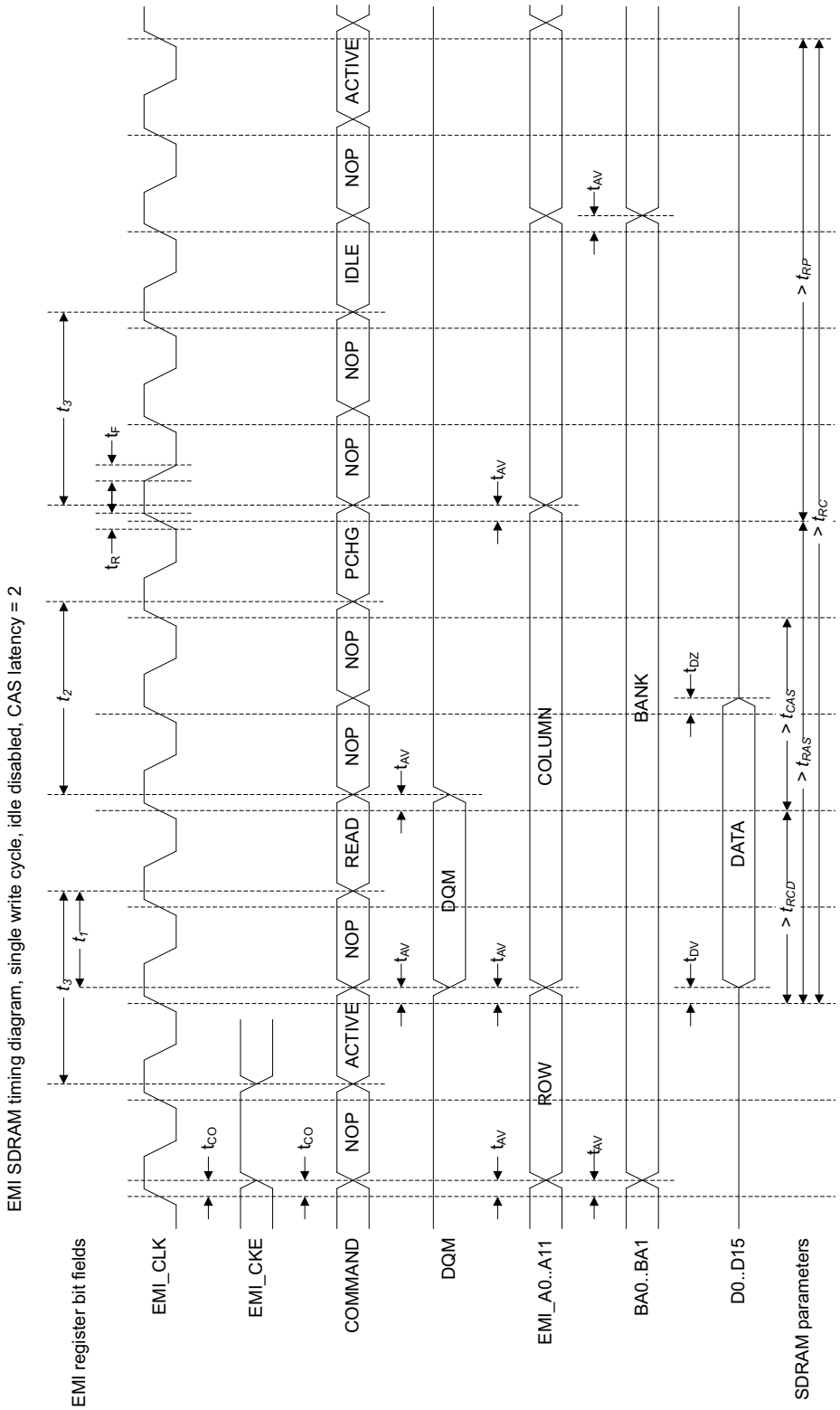


Figure 13: EMI SDRAM mode write cycle timing diagram

External Host Interface (EHI)

MMP mode

The table below for the eICE debug port uses the symbol T_{CPU} for the CPU clock period.

Symbol	Parameter	Min	Max	Units
t_{AS}	Setup time host address valid to EHI_CS active	0		ns
t_{AH}	Hold time EHI_CS inactive to host address invalid	0		ns
t_{CW}	Delay time EHI_CS active to EHI_WAIT active		12	ns
t_{WW}	Minimum EHI_WAIT active width	3 x T_{CPU}		ns
t_{WC}	Delay time EHI_WAIT inactive to EHI_CS inactive	0		ns
t_{DV}	Minimum time data output valid before EHI_WAIT inactive	T_{CPU} – 5		ns
t_{DZ}	Delay time EHI_CS inactive to data output invalid	13		ns
t_{DS}	Setup time data input valid to EHI_CS inactive	5		ns
t_{DH}	Hold time EHI_CS inactive to data input invalid	3		ns
t_{CI}	Minimum EHI_CS inactive time	3 x T_{CPU}		ns

Table 32: AC characteristics - EHI MMP mode

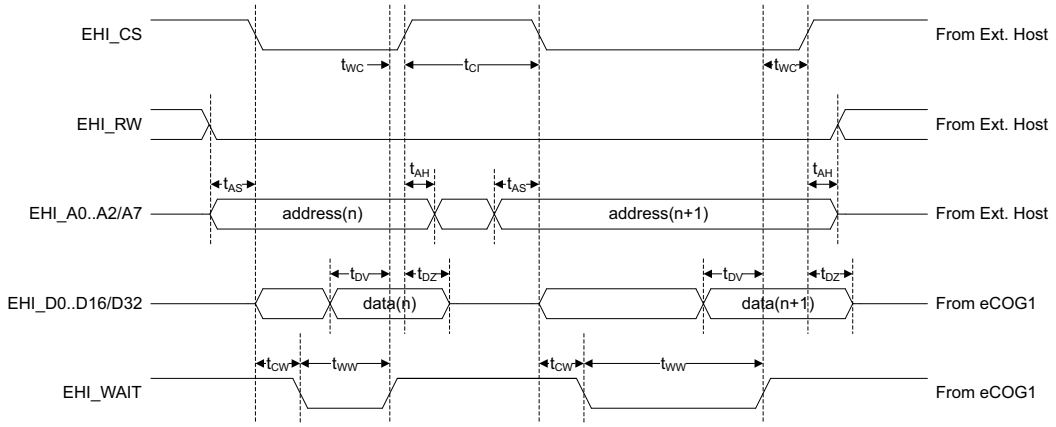


Figure 14: EHI MMP read cycle timing diagram

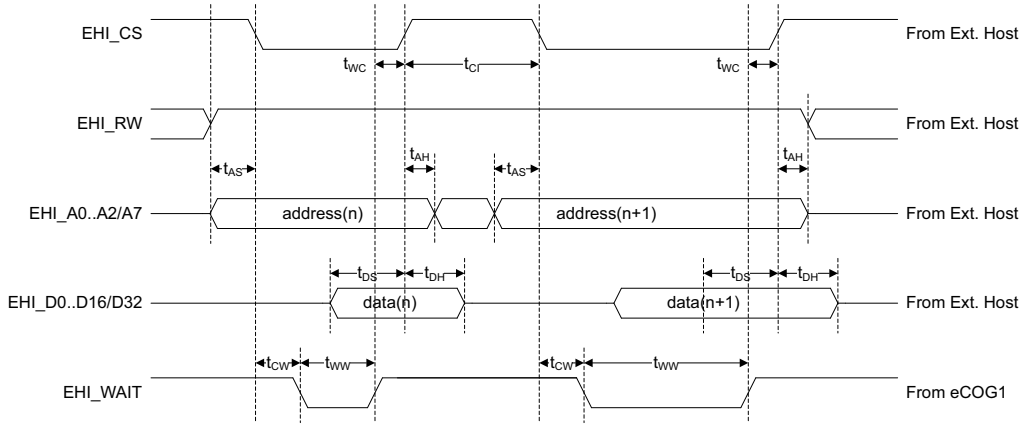


Figure 15: EHI MMP write cycle timing diagram

DMA Mode

The tables below for the EHI function in DMA mode use the following symbols for time periods defined by bit fields in the EHI registers.

Symbol	Description	Definition	Units
T_{CPU}	CPU clock period		ns
N_1	EHI_ACK output active period (0..3)	***fd.ehi.cfg.dma_ack_act_prd1***	
N_2	EHI_ACK output inactive period (0..3)	***fd.ehi.cfg.dma_ack_act_prd2***	

Table 33: EHI clock symbols

DMA Mode - eCOG1X as master

Symbol	Parameter		Min	Max	Units
t_{R1}	Delay time EHI_REQ active to EHI_ACK active		(2 x T_{CPU}) + 3		ns
t_{R2}	Delay time EHI_ACK active to EHI_REQ inactive	Continue next transfer (min)	0		ns
		Pause next transfer (max)	(T_{CPU} x (N_1 + N_2)) – 20		ns
t_{R3}	Minimum EHI_REQ input inactive width		0		ns
t_{A1}	Minimum EHI_ACK output active width		T_{CPU} x (N_1 + 1)		ns
t_{A2}	Minimum EHI_ACK output inactive width		T_{CPU} x (N_2 + 1)		ns
t_{DV}	Delay time data output valid to EHI_ACK output active		–3	+3	ns
t_{DS}	Setup time data input valid to EHI_ACK output inactive		13		ns
t_{DH}	Hold time EHI_ACK output inactive to data input invalid		0		ns

Table 34: AC characteristics - EHI DMA master mode

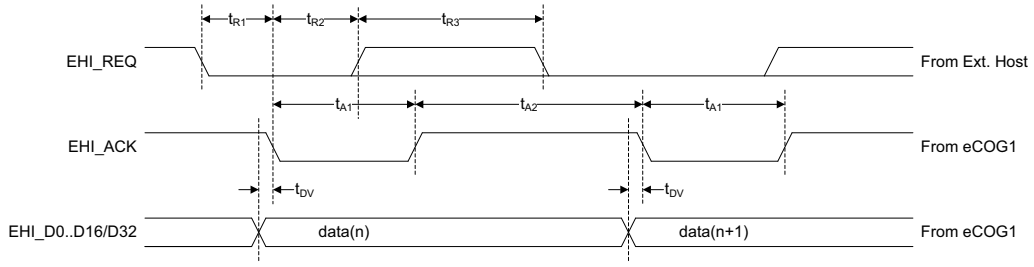


Figure 16: EHI DMA master read cycle timing diagram

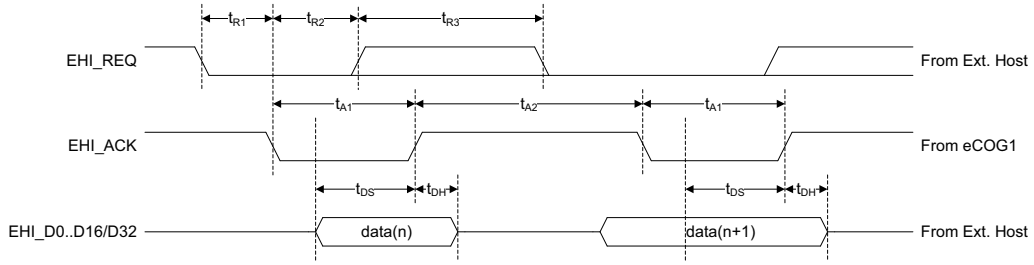


Figure 17: EHI DMA master write cycle timing diagram

DMA mode - eCOG1X as slave

Symbol	Parameter	Min	Max	Units
t_{R1}	Delay time EHI_REQ output active to EHI_ACK input active	0		ns
t_{R2}	Delay time EHI_ACK input active to EHI_REQ output inactive		(4 x T_{CPU}) + 22	ns
t_{R3}	Delay time EHI_ACK input inactive to EHI_REQ output active	2 x T_{CPU}		ns
t_{A1}	Minimum EHI_ACK input active width	T_{CPU} + 5		ns
t_{A2}	Minimum EHI_ACK input inactive width	T_{CPU} + 5		ns
t_{DV}	Delay time EHI_ACK input active to data output valid		13	ns
t_{DI}	Delay time EHI_ACK input inactive to data output invalid		13	ns
t_{DS}	Setup time data input valid to EHI_ACK input inactive	3		ns
t_{DH}	Hold time EHI_ACK input inactive to data input invalid	5		ns

Table 35: AC characteristics - EHI DMA slave mode

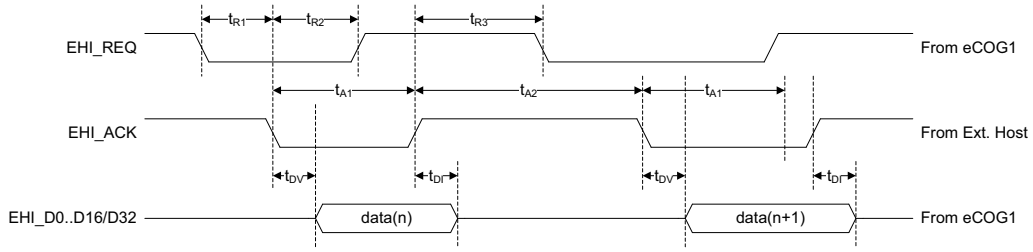


Figure 18: EHI DMA slave read cycle timing diagram

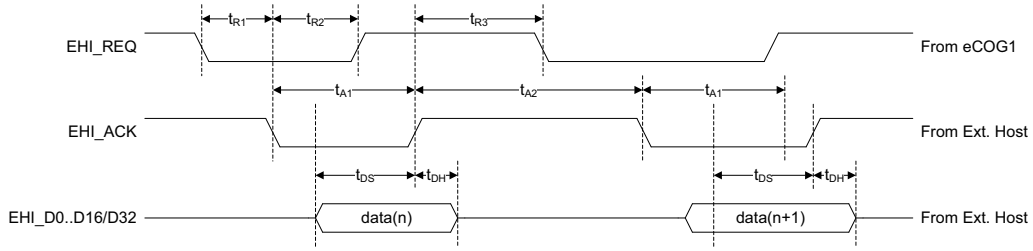


Figure 19: EHI DMA slave write cycle timing diagram

Serial Peripheral Interface (SPI)

The tables below for the SPI function use the following symbols for time periods defined by bit fields in the DUSART registers.

Symbol	Description	Definition	Units
T_{CLK}	DUSART peripheral input clock period		ns
N_S	DUSART sample period (0..255)	***fd.dusart.*_smpl_cfg.period***	
N_H	DUSART serial clock active period (0..255)	***fd.dusart.*_sym_cfg.clk_high***	
N_L	DUSART serial clock inactive period (0..255)	***fd.dusart.*_sym_cfg.clk_low***	
T_{BIT}	Serial data bit time (master mode)	T_{CLK} x (N_S+1) x ((N_H+1) + (N_L+1))	ns

Table 36: DUSART clock symbols

Master mode

Symbol	Parameter		Min	Typ	Max	Units
t_R, t_F	SCLK output rise and fall time		See Table 28			
t_{CKA}	SCLK output active time		T_{CLK} x (N_S+1) x (N_H+1)			ns
t_{CKI}	SCLK output inactive time		T_{CLK} x (N_S+1) x (N_L+1)			ns
t_{CSA}	Delay time from chip select active to first SCLK edge	***clk_pha*** = 0	(1 x T_{BIT}) + (1 x t_{CKI})			ns
		clk_pha = 1	1 x T_{BIT}			ns
t_{CSI}	Delay time from last SCLK edge to chip select inactive	***clk_pha*** = 0	1 x T_{BIT}			ns
		clk_pha = 1	(1 x T_{BIT}) + (1 x t_{CKI})			ns
t_{CSD}	Sequential transfer delay time		1 x T_{BIT}			ns
t_{DV}	Delay time from chip select active to MOSI output valid				5	ns
t_{CD}	Delay time SCLK to MOSI output				9	ns
t_{DI}	Delay time from chip select inactive to MOSI output invalid	***clk_pha*** = 0			5	ns
		clk_pha = 1	1 x t_{CKI}			ns
t_{DS}	Setup time MISO input valid to SCLK				26	ns
t_{DH}	Hold time SCLK to MISO input invalid		T_{CLK} x N_S			ns

Table 37: AC characteristics - SPI master mode

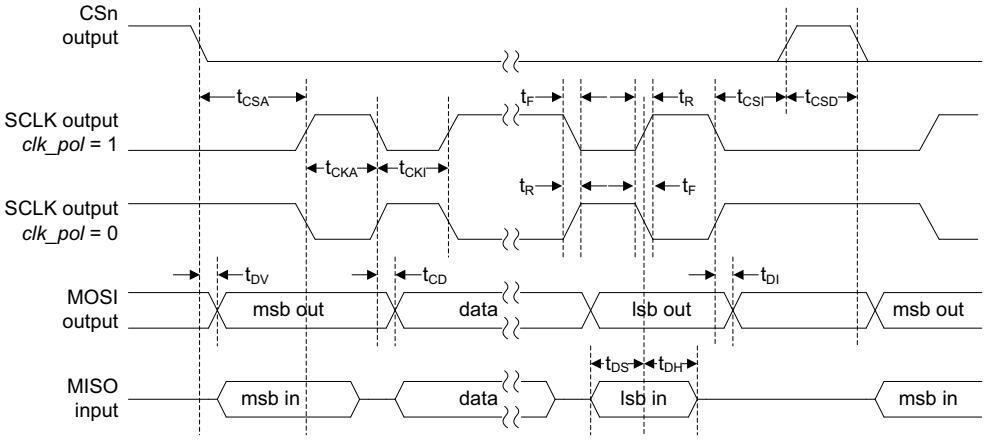


Figure 20: SPI timing diagram, master mode, *clk_pha* = 0

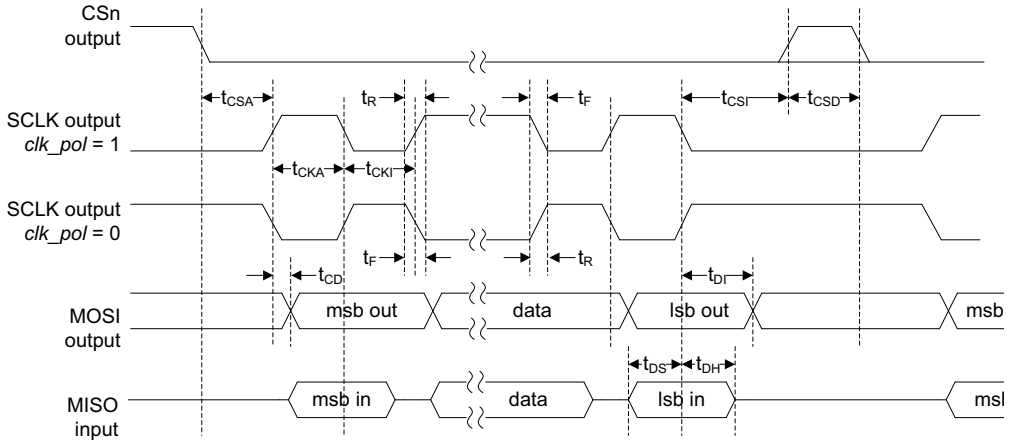


Figure 21: SPI timing diagram, master mode, *clk_pha* = 1

Slave mode

Note that all input signals are sampled at the DUSART symbol sample clock frequency, set by the ***period*** bit field in the ***dusart.a_smpl_cfg*** register. This clock must be fast enough to sample correctly the required input signals and detect input state changes within a suitable fraction of the serial bit time.

Symbol	Parameter	Typ	Units
t_{CKW}	SCLK input high or low time	T_{CLK} x (N_S+2)	ns
t_{CSA}	Delay time from chip select active to first SCLK edge	T_{CLK} x (N_S+1)	ns
t_{CSI}	Delay time from last SCLK edge to chip select inactive	T_{CLK} x (N_S+2)	ns
t_{CSD}	Sequential transfer delay time	T_{CLK} x (N_S+2)	ns
t_{DV}	Delay time from chip select active to MISO output valid	T_{CLK} x (N_S+3) + 18	ns
t_{CD}	Delay time SCLK to MISO output	T_{CLK} x (N_S+3) + 18	ns
t_{DI}	Delay time from chip select inactive to MISO output invalid	T_{CLK} x (N_S+3) + 18	ns
t_{DS}	Setup time MOSI input valid to SCLK	T_{CLK} x (N_S+1) + 8	ns
t_{DH}	Hold time SCLK to MOSI input invalid	T_{CLK} x N_S + 8	ns

Table 38: AC characteristics - SPI slave mode

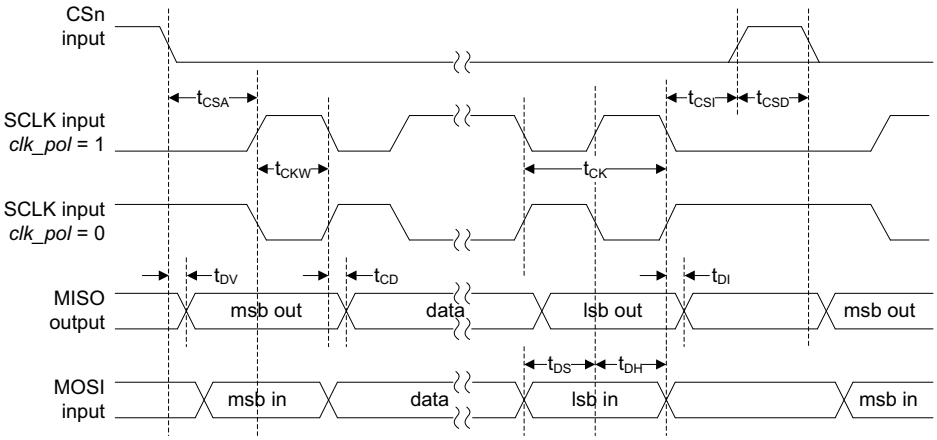


Figure 22: SPI timing diagram, slave mode, *clk_pha* = 0

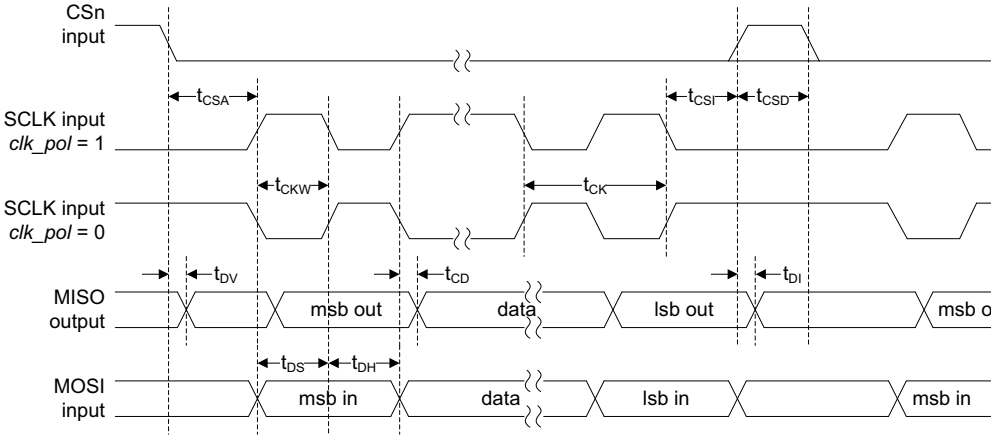


Figure 23: SPI timing diagram, slave mode, *clk_pha* = 1

Enhanced Serial Peripheral Interface (ESPI)

The tables below for the ESPI function use the following symbols for time periods defined by bit fields in the ESPI configuration registers.

Symbol	Description	Definition	Units
T_{CLK}	ESPI peripheral input clock period		ns
N_0	ESPI serial clock active period (0..65535)	***rg.espi.ph0_time***	
N_1	ESPI serial clock inactive period (0..65535)	***rg.espi.ph1_time***	
N_2	ESPI chip select to first clock delay (0..65535)	***rg.espi.cs_clk_time***	
N_3	ESPI last clock to chip select delay (0..65535)	***rg.espi.clk_cs_time***	
N_4	ESPI chip select inactive delay (0..65535)	***rg.espi.if_time***	
T_{BIT}	Serial data bit time (master mode)	T_{CLK} x ((N_0+1) + (N_1+1))	ns

Table 39: ESPI clock symbols

Master mode

Symbol	Parameter	Min	Typ	Max	Units
t_R, t_F	SCLK output rise and fall time	See Table 28			
t_{CKA}	SCLK output active time	T_{CLK} x (N_0+1)			ns
t_{CKI}	SCLK output inactive time	T_{CLK} x (N_1+1)			ns
t_{CSA}	Delay time from chip select active to first SCLK edge	T_{CLK} x (N_2+1)			ns
t_{CSI}	Delay time from last SCLK edge to chip select inactive	T_{CLK} x (N_3+1)			ns
t_{CSD}	Minimum chip select inactive time	T_{CLK} x (N_4+1)			ns
t_{DV}	Delay time from chip select active to MOSI output valid			3	ns
t_{CD}	Delay time SCLK to MOSI output			3	ns
t_{DI}	Delay time from chip select inactive to MOSI output invalid			3	ns
t_{DS}	Setup time MISO input valid to SCLK	22			ns
t_{DH}	Hold time SCLK to MISO input invalid	0			ns

Table 40: AC characteristics - ESPI master mode

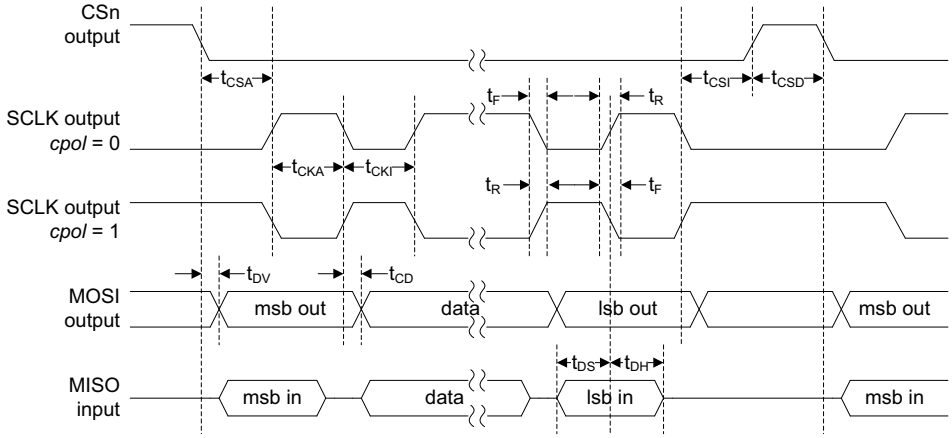


Figure 24: ESPI timing diagram, master mode, *cpha* = 0

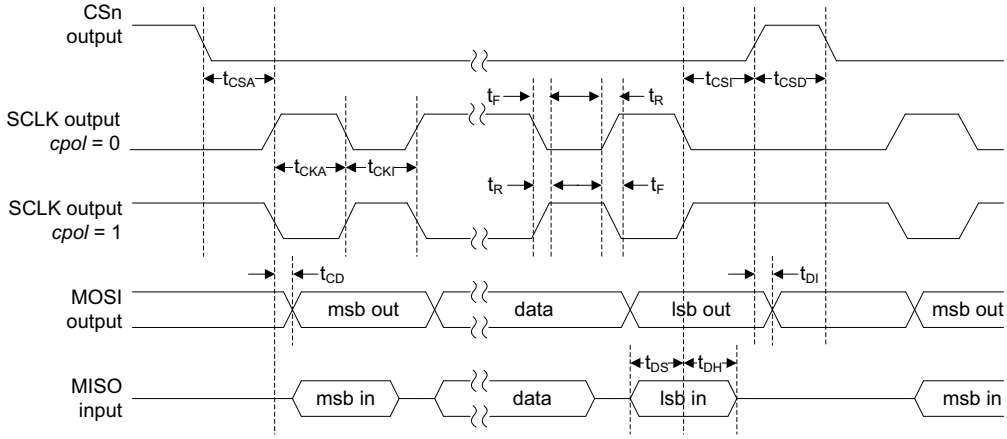


Figure 25: ESPI timing diagram, master mode, *cpha* = 1

Slave mode

Symbol	Parameter	Min	Typ	Max	Units
t_{CK}	SCLK input period	T_{CLK}			ns
t_{CKW}	SCLK input high or low time	10			ns
t_{CSA}	Delay time from chip select active to first SCLK edge	4			ns
t_{CSI}	Delay time from last SCLK edge to chip select inactive	2			ns
t_{CSD}	Sequential transfer delay time	0			ns
t_{DV}	Delay time from chip select active to MISO output valid			3	ns
t_{CD}	Delay time SCLK to MISO output			20	ns
t_{DI}	Delay time from chip select inactive to MISO output invalid			3	ns
t_{DS}	Setup time MOSI input valid to SCLK	4			ns
t_{DH}	Hold time SCLK to MOSI input invalid	2			ns

Table 41: AC characteristics - ESPI slave mode

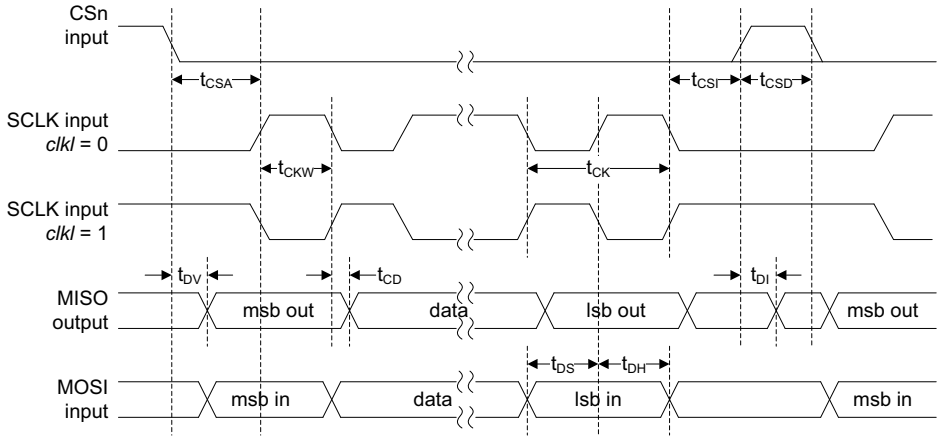


Figure 26: ESPI timing diagram, slave mode, *cpha* = 0

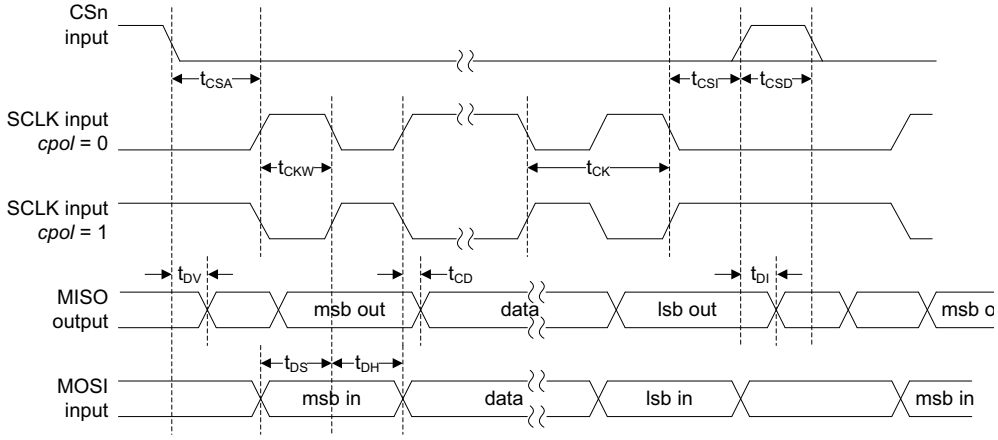


Figure 27: ESPI timing diagram, slave mode, *cpha* = 1

I2S

The tables below for the I2S function use the following symbols for time periods defined by bit fields in the I2S configuration registers.

Symbol	Description		Definition	Units
T_{CLK}	I2S peripheral input clock period		Set by SSM	ns
T_{ACLK}	I2S alternate clock input period		External input signal	ns
T_{MCLK}	I2S master clock period	***clk_sel*** = 00	T_{CLK}	ns
		clk_sel = 10	T_{ACLK}	ns
N_M	Master clock divisor		***fd.i2s.cfg2.div_ratio***	N_M

Table 42: I2S clock symbols

Master mode

Symbol	Parameter		Min	Typ	Max	Units
T_{SCLK}	I2S serial clock period	***mclk_en*** = 0	T_{MCLK}			ns
		mclk_en = 1	$T_{MCLK} \times N_M$			ns
C_{CK}	SCLK duty cycle (SCLK driven from an internal clock source)		45		55	%
t_R, t_F	SCLK output rise and fall time		See Table 28			
t_{CW}	Delay time SCLK falling edge to WS output valid		0		2	ns
t_{CD}	Delay time SCLK falling edge to data output valid		0		2	ns
t_{DS}	Setup time data input valid to SCLK rising edge	***mclk_en*** = 0	21			ns
		mclk_en = 1	$(T_{MCLK} / 2) + 26$			
t_{DH}	Hold time SCLK rising edge to data input invalid	***mclk_en*** = 0	0			ns
		mclk_en = 1	0			

Table 43: AC characteristics - I2S master mode

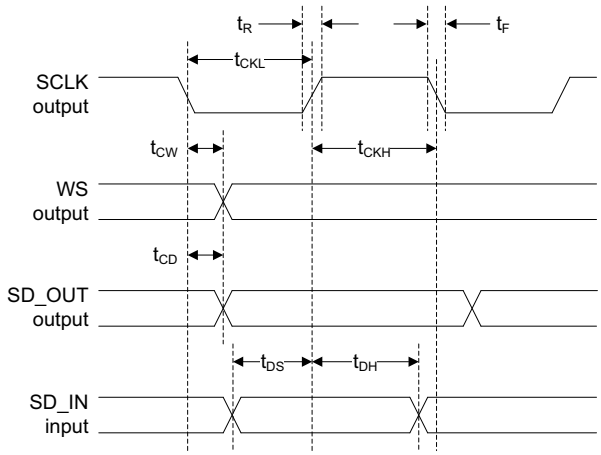


Figure 28: I2S master mode timing diagram

Slave mode

Symbol	Parameter	Min	Typ	Max	Units
t_{CK}	SCLK input period	100			ns
t_{CKL}	SCLK input low time	50			ns
t_{CKH}	SCLK input high time	50			ns
t_{WS}	Setup time WS input valid to SCLK rising edge	9			ns
t_{WH}	Hold time SCLK rising edge to WS input invalid	1			ns
t_{CD}	Delay time SCLK falling edge to data output valid			22	ns
t_{DS}	Setup time data input valid to SCLK rising edge	7			ns
t_{DH}	Hold time SCLK rising edge to data input invalid	2			ns

Table 44: AC characteristics - I2S slave mode

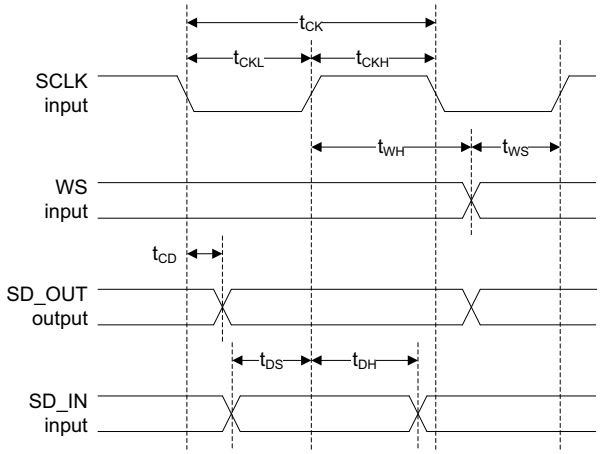


Figure 29: I2S slave mode timing diagram

Clock signals

Symbol	Parameter	Min	Typ	Max	Units
t_{CK}	ALT_CLK_IN input cycle time	40			ns
t_{CKL}	ALT_CLK_IN input low time	20			ns
t_{CKH}	ALT_CLK_IN input high time	20			ns
t_R, t_F	MCLK output rise and fall time	See Table 28			
t_1	Propagation delay ALT_CLK_IN to MCLK (falling edge)			13	ns
t_2	Propagation delay ALT_CLK_IN to MCLK (rising edge)			14	ns
t_3	Delay time MCLK falling edge to SCLK edge (master mode, ***mclk_en*** = 1)			3	ns
t_4	Propagation delay ALT_CLK_IN to SCLK (falling edge) (master mode, ***mclk_en*** = 0)			15	ns
t_5	Propagation delay ALT_CLK_IN to SCLK (rising edge) (master mode, ***mclk_en*** = 0)			16	ns

Table 45: AC characteristics - I2S clock signals

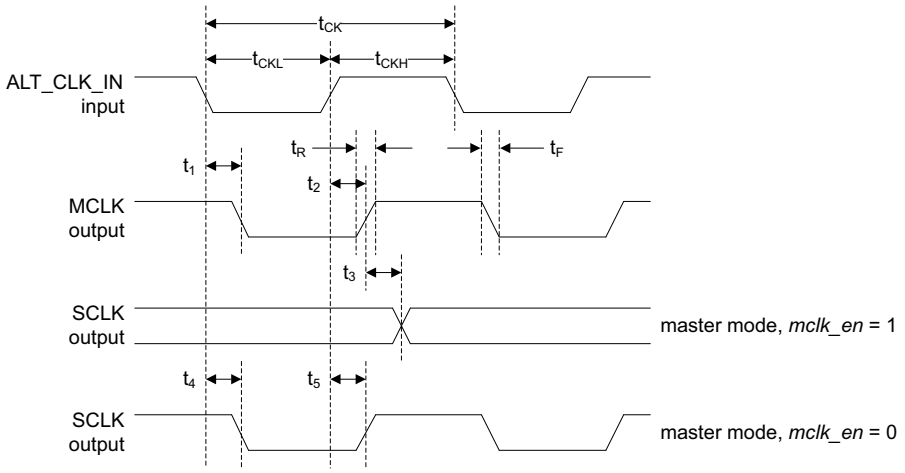


Figure 30: I2S clock signals timing diagram

Ethernet MAC

MII Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CT}	CLKT transmit clock input frequency (1 / t_{CT}) [1]	10Mb/s	2.5 ± 100ppm			MHz
		100Mb/s	25 ± 100ppm			MHz
f_{CR}	CLKR receive clock input frequency (1 / t_{CR}) [1]	10Mb/s	2.5 ± 100ppm			MHz
		100Mb/s	25 ± 100ppm			MHz
C_{CT}	CLKT input duty cycle		35		65	%
C_{CR}	CLKR input duty cycle		35		65	%
t_{CD}	Delay time CLKT rising edge to transmit data output valid		6		17	ns
t_{DS}	Setup time receive data input valid to CLKR rising edge		0			ns
t_{DH}	Hold time CLKR rising edge to receive data input invalid		9.3			ns

Table 46: AC characteristics - EMAC

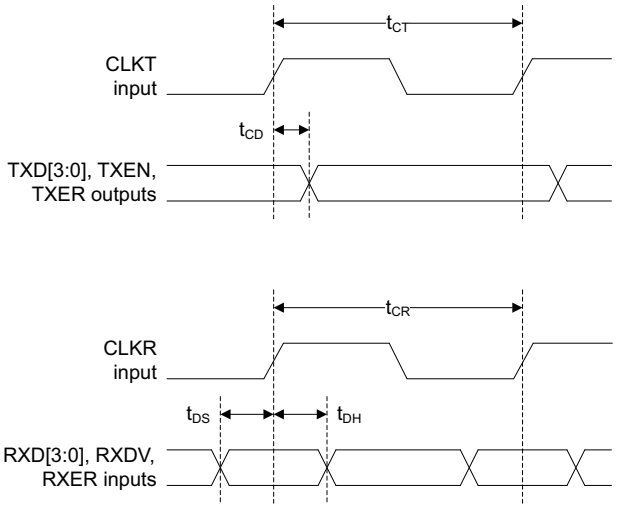


Figure 31: EMAC MII timing diagram

1 These are the limits for the transmit and receive input clock frequencies in order to meet the requirements of the IEEE802.3 standard.

USB

USB PHY Output Driver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RL}	Rise time (low speed)	C_L = 600pF 10 to 90% of $\|(V_{OH} - V_{OL})\|$	75		300	ns
t_{FL}	Fall time (low speed)		75		300	ns
t_{RF}	Rise time (full speed)	C_L = 50pF 10 to 90% of $\|(V_{OH} - V_{OL})\|$	4		20	ns
t_{FF}	Fall time (full speed)		4		20	ns
V_{CR}	Output crossover voltage	Excluding first transition from IDLE state	1.3		2.0	V
t_{RFM}	Rise and fall time matching		90		110	%

Table 47: AC characteristics - USB PHY

ULPI Port

Symbol	Parameter	Min	Typ	Max	Units
f_{CK}	ULPI_CLK input frequency	59.97	60.0	60.03	MHz
C_{CK}	ULPI_CLK input duty cycle	49.975	50	50.025	%
t_{CO}	Delay time ULPI_CLK rising edge to STP output valid	3.5		9.2	ns
t_{CD}	Delay time ULPI_CLK rising edge to data outputs valid	2.5		9.0	ns
t_{IS}	Setup time NXT, DIR input valid to ULPI_CLK rising edge	4.9			ns
t_{IH}	Hold time ULPI_CLK rising edge to NXT, DIR input invalid	0			ns
t_{DS}	Setup time data inputs valid to ULPI_CLK rising edge	3.1			ns
t_{DH}	Hold time ULPI_CLK rising edge to data inputs invalid	0.4			ns
t_{DZ}	Delay time DIR input rising edge to data outputs tristate			7.8	ns
t_{DE}	Delay time ULPI_CLK rising edge to data outputs enabled			8.3	ns

Table 48: AC characteristics - USB ULPI port

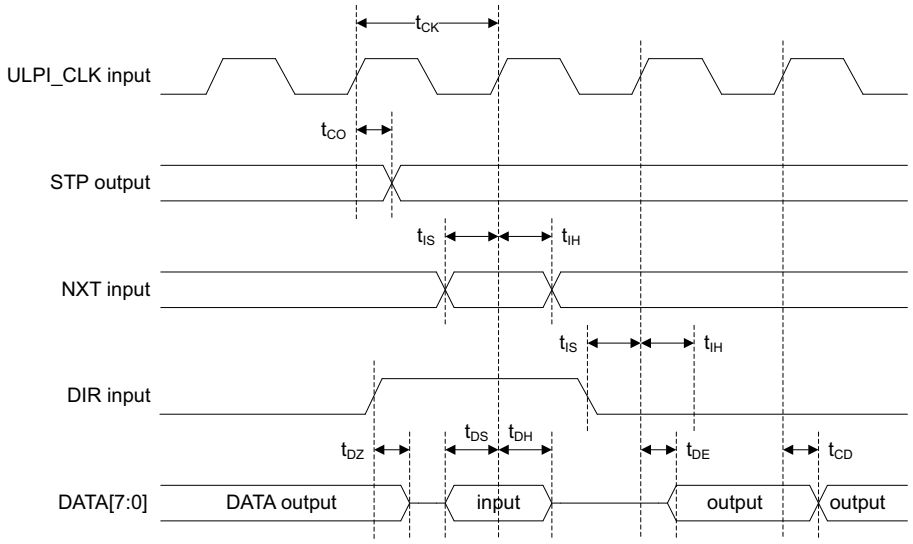


Figure 32: USB ULPI timing diagram

eICE Debug Port

The table below for the eICE debug port uses the symbol T_{CPU} for the CPU clock period.

Symbol	Parameter	Min	Typ	Max	Units
t_{CKH}	eICE_CLK input high time	10			ns
t_{CKL}	eICE_CLK input low high time	10			ns
t_{DS}	Setup time MOSI input valid to eICE_CLK falling edge	4			ns
t_{DH}	Hold time eICE_CLK falling edge to MOSI input invalid	1			ns
t_{CD}	Delay time eICE_CLK rising edge to MISO output valid			17	ns
t_1	Delay time eICE_CLK falling edge to master LOADB active	5			ns
t_2	Delay time LOADB active to MISO high			18	ns
t_3	Delay time MISO high to slave LOADB active	$(4 \times T_{CPU}) + 13$			ns
t_4	Delay time MISO high to MISO low	$(4 \times T_{CPU}) + 13$			ns
$(t_3 - t_4)$	Skew between slave LOADB active and MISO low			±3	ns
t_5	Delay time MISO low to master LOADB inactive	5			ns
t_6	Delay time MISO low to slave LOADB inactive	Min: $(3 \times T_{CPU}) + 13$ Max: command dependent			ns
t_7	Delay time LOADB inactive to eICE_CLK rising edge	5			ns

Table 49: AC characteristics - eICE debug port

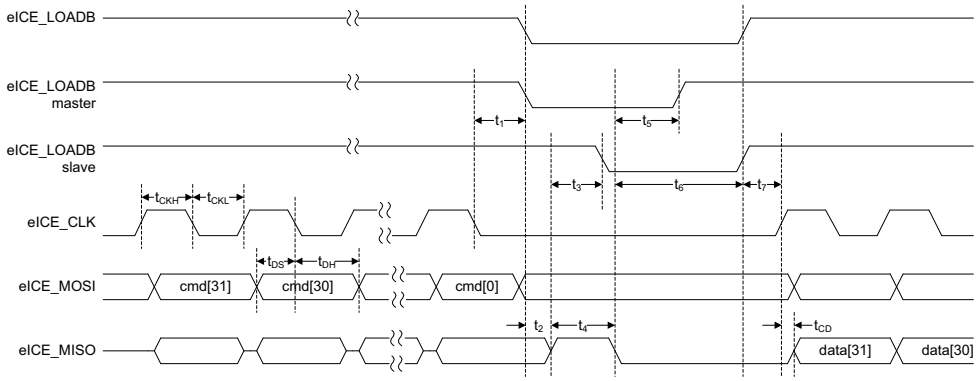


Figure 33: eICE read timing diagram

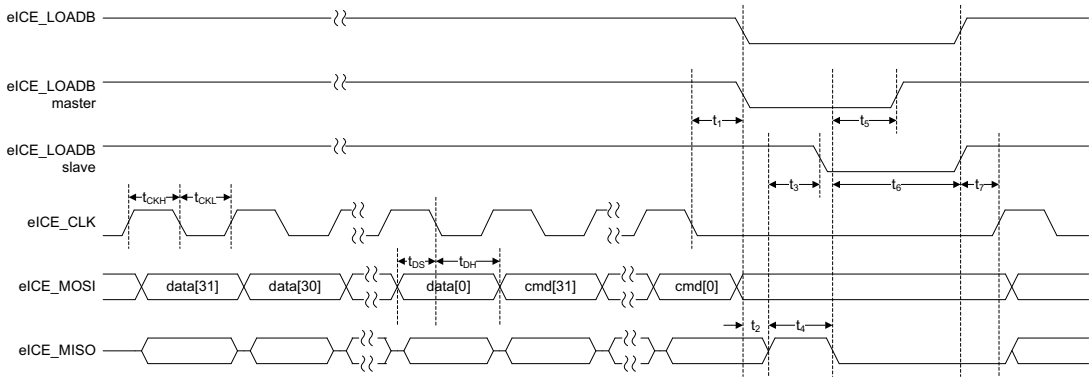


Figure 34: eICE write timing diagram

Peripheral Clock Frequency Limits

The clock sources, PLLs and SSM provide clock signals to the on-chip peripheral modules over a wide frequency range. There are maximum (and in some cases minimum) frequency limits on the clock signals provided by the SSM to the peripheral modules.

The following table lists any limits or constraints on input clock frequencies for the CPU and the on-chip peripherals, after the SSM clock dividers and prescalers. Note that each frequency listed here is the absolute maximum internal clock frequency for the peripheral. This means only that the internal peripheral hardware can be clocked at this maximum frequency, it does not mean that the complete peripheral function including external signals operates successfully at this frequency. Input and output delay times and pin loadings must be taken into account when determining the maximum operating frequency for any peripheral including external signals.

Module		Clock frequency (MHz)	
		Min.	Max.
CPU		0	71
EMI [1]		0	150
Timer	TMR	0	175
Counter/timers	CNT1	0	192
	CNT2	0	189
PWM timers	PWM1	0	206
	PWM2	0	194
Capture timer	CAP	0	203
Watchdog timer	WDOG	0	196
Long interval timer	LTMR	0	140
DUART	UART1A	0	195
	UART1B	0	215
	UART2A	0	202
	UART2B	0	202
DUSART		0	86
Flash memory timer		0	175
ADC	12 bits	0	3.2
	10 bits	0	4.9
	8 bits	0	6.0
	6 bits	0	8.0
DAC [2]		0	0.25
ESPI		0	209
I^2S		0	78
LCD		0	364
MCPWM		0	158
DSCI		0	172
EMAC [3]	10Mb/s	3.0	87
	100Mb/s	30	87
USB [4]		48 ± 0.05%	

Table 50: Internal clock frequency limits

1 If the high PLL is used as the memory clock source and the EMI peripheral is used, then the high PLL output frequency must be limited to a maximum of 385MHz. If the EMI peripheral is not used, the maximum high PLL output frequency of 400MHz can be used to generate the internal memory and CPU clocks.

2 The maximum useful DAC clock frequency is 250kHz since the DAC analogue output has a settling time of 4µs. The DAC interface logic can be clocked at much higher frequencies.

3 The EMAC peripheral is fully static and has a minimum clock frequency of zero. To support data communication at either 10Mb/s or 100Mb/s, higher minimum clock frequencies are required as shown.

4 The USB core is also fully static and has a minimum clock frequency of zero. However, in normal operation it requires a 48.0 MHz clock in order to meet the USB standard timing specifications.

Embedded Flash Memory Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Normal (fast) mode operation					
T_{RD}	Read access time				34	ns
T_{CY}	Read cycle time		49			ns
I_{FR}	Read current (20MHz)	IV_{DD} (1.8V)		18.5	27.2	mA
		V_{DD} (3.3V)		3.0	10.8	mA
I_{FS}	Read standby current	IV_{DD} (1.8V)		660	990	µA
		V_{DD} (3.3V)		40	68	µA
	Slow mode operation					
T_{RD2}	Slow read access time				2	µs
T_{CY2}	Slow read cycle time		60			µs
I_{FR2}	Slow read current (16kHz)	IV_{DD} (1.8V)		40	120	µA
		V_{DD} (3.3V)		60	90	µA
I_{FS2}	Slow read standby current	IV_{DD} (1.8V)		25	30	µA
		V_{DD} (3.3V)		30	50	µA
	Stop mode operation					
I_{FS3}	Stop mode current	IV_{DD} (1.8V)			5	µA
		V_{DD} (3.3V)				µA
	Program/erase operation					
T_{SE}	Sector erase time	From all ‘0’		217	658	ms
T_{CE}	Chip erase time	From all ‘0’		2.2	6.4	s
T_{WP}	Word programming time			102.4	315.2	µs
T_{BP}	Write buffer programming time			0.8	2.77	ms
N_{EP}	Maximum erase/program cycles		1000	10000		cycles
T_{DR}	Data retention time		10			years
I_{FP}	Active program current	IV_{DD} (1.8V)		8	18	mA
		V_{DD} (3.3V)		8	18	mA
I_{FE}	Active erase current	IV_{DD} (1.8V)		6	14	mA
		V_{DD} (3.3V)		8	22.8	mA
V_{LKO}	Program/erase lockout voltage	V_{DD} (3.3V)	2.4			V
I_{PP}	Fast programming supply current	V_{PP} (9V)				µA

Table 51: Embedded flash memory characteristics

The VPP pin is used with a higher voltage supply to support fast programming of the internal flash memory via JTAG. If this function is not required, then the VPP pin should be connected to GND to minimise power consumption in normal operation. If this function is required, then connect VPP to GND via a pull-down resistor or jumper link so that the higher voltage programming supply can be connected.

Analogue Characteristics

ADC

This table lists the performance characteristics of the analogue-to-digital converter over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{ADC}	Supply current AV_{DD} (including V_{REF})	Enabled	368	598	1120	µA
I_{ADCSB}	Standby current AV_{DD}	Disabled		0.013	6	µA
T_{PU1}	Power up time	V_{REF} stable			10	us
T_{PU2}	Power up time	Including V_{REF} startup			6	ms
C_{IN}	Input capacitance	Sample/hold capacitor		30		pF
AV_{IN}	Analogue input range	Conversion data valid	0		V_{REF}	V
	ADC Performance	Resolution:				
	Clock frequency	12 bits			3.2	MHz
		10 bits			4.9	
		8 bits			6.0	
		6 bits			8.0	
	Conversion time (continuous mode)	12 bits		16		Clocks
		10 bits		14		
		8 bits		12		
		6 bits		10		
	Conversion rate (continuous mode)	12 bits			200	ks/s
		10 bits			350	
		8 bits			500	
		6 bits			800	
	Conversion time (software or timer triggered mode)	12 bits		17		Clocks
		10 bits		15		
		8 bits		13		
		6 bits		11		
	Conversion rate (software or timer triggered mode)	12 bits			188	ks/s
		10 bits			326	
		8 bits			461	
		6 bits			727	
	Temperature sensor sampling time	12 bits	10			µs
		10 bits	9.0			
		8 bits	7.5			
		6 bits	6.0			
	Supply voltage sensor sampling time	12 bits	8.5			µs
		10 bits	7.5			
		8 bits	6.0			
		6 bits	5.0			

Table 52: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy					
	No missing codes		12			Bits
DNL	Differential linearity error			±0.5	±1	LSB
INL	Integral linearity error			±0.5	±1	LSB
	Gain error	Excluding V_{REF} error		0		LSB
	Offset error			±0.2	±1	LSB
	AC Accuracy	F_S = 50ks/s, –3dBFS				
SNR	Signal-to-noise ratio		66.6	66.8	67.1	dB
SFDR	Spurious-free dynamic range		81.0	82.9	85.2	dB
THD	Total harmonic distortion		-82.2	-80.7	-79.1	dB
SINAD	Signal-to-(Noise + Distortion)		66.4	66.6	66.9	dB
	Noise floor		-103.2	-103.0	-102.8	dB
ENOB	Effective number of bits		11.26	11.29	11.33	Bits
	AC Accuracy	F_S = 100ks/s, –3dBFS				
SNR	Signal-to-noise ratio		66.6	66.8	67.0	dB
SFDR	Spurious-free dynamic range		78.6	81.8	86.3	dB
THD	Total harmonic distortion		-83.8	-80.0	-77.3	dB
SINAD	Signal-to-(Noise + Distortion)		66.3	66.6	66.9	dB
	Noise floor		-103.2	-103.0	-102.8	dB
ENOB	Effective number of bits		11.23	11.29	11.33	Bits
	AC Accuracy	F_S = 200ks/s, –3dBFS				
SNR	Signal-to-noise ratio		65.3	66.6	67.0	dB
SFDR	Spurious-free dynamic range		74.0	79.7	84.8	dB
THD	Total harmonic distortion		-81.7	-78.1	-73.1	dB
SINAD	Signal-to-(Noise + Distortion)		64.8	66.3	66.9	dB
	Noise floor		-103.2	-102.8	-101.5	dB
ENOB	Effective number of bits		10.98	11.23	11.32	Bits

Table 52: ADC characteristics

DAC

This table lists the performance characteristics of the digital-to-analogue converter over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DAC}	Supply current AV_{DD}	Enabled	62	85	103	µA
I_{DACSB}	Standby current AV_{DD}	Disabled		0.015	8	µA
T_{PU1}	Power up time	V_{REF} stable			10	us
T_{PU2}	Power up time	Including V_{REF} startup			6	ms
	Output noise	1Hz to 20MHz, enabled, Data = 0xB84		33		µVrms
	Output voltage slew rate	C_{LOAD} = 50pF	1.0	1.8	3.0	V/µs
T_S	Output settling time	C_{LOAD} = 50pF Data 0x000 -> 0xB84	5	9	15	µs
AV_{OL}	Output voltage	Data = 0x000			0.003	V
AV_{OH}	Output voltage	Data = 0xFFF	V_{REF} – 0.003			V
Z_{OUT}	Output impedance	V_{OUT} = 1.2V			500	Ω
PSRR	Power supply rejection, ΔV_{DD} = 100mV	Data = 0x800 External V_{REF}		65		dB
	Accuracy					
	Resolution	Guaranteed monotonic	12			Bits
	Differential linearity error			±1	±2	LSB
	Integral linearity error			±5	±10	LSB
	Gain error	Excluding V_{REF} error		±0.25	±0.5	%
	Offset error		2.5	5	7	LSB

Table 53: DAC characteristics

Voltage Reference

This table lists the performance characteristics of the internal voltage reference over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	Internal reference voltage	Over process, voltage, and temperature ranges. Excluding device mismatch.	1.21	1.22	1.23	V
ΔV_{REF}	Tolerance	Device mismatch		±23.9		mV
V_{REFE}	External reference voltage		0		1.40	V
	V_{REF} output error (Internal V_{REF} enabled)	R_{LOAD} = 4kΩ			1	%
		R_{LOAD} = 6.8kΩ			0.1	%
		R_{LOAD} = 70kΩ			0.01	%
Z_{IN}	Input impedance	Internal V_{REF} disabled			20	MΩ
T_{EN}	Startup Time	-40°C		2.8	4.6	ms
		+25°C		3.2	5.3	
		+85°C		3.6	6.0	
	Temperature coefficient	Excluding device mismatch			132	ppm/°C
PSRR	Power Supply Rejection	100Hz		78		dB
		100kHz		50		dB

Table 54: Voltage reference characteristics

Applications which use the analogue inputs or outputs with the internal reference voltage must have external decoupling capacitors connected to the Vref pin. The recommended decoupling on this pin is a 100nF ceramic capacitor in parallel with a 4.7µF tantalum or aluminium electrolytic capacitor.

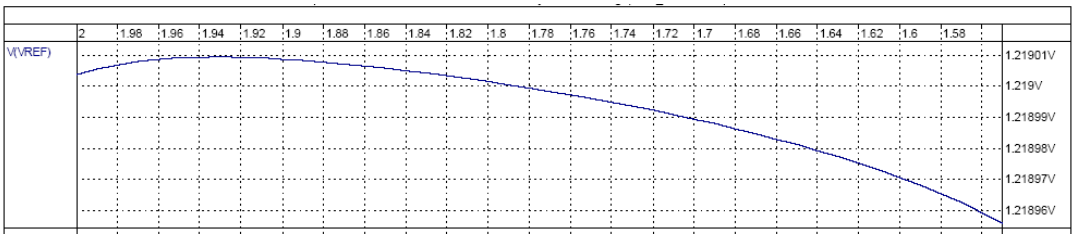


Figure 35: Vref variation with supply voltage (typical)

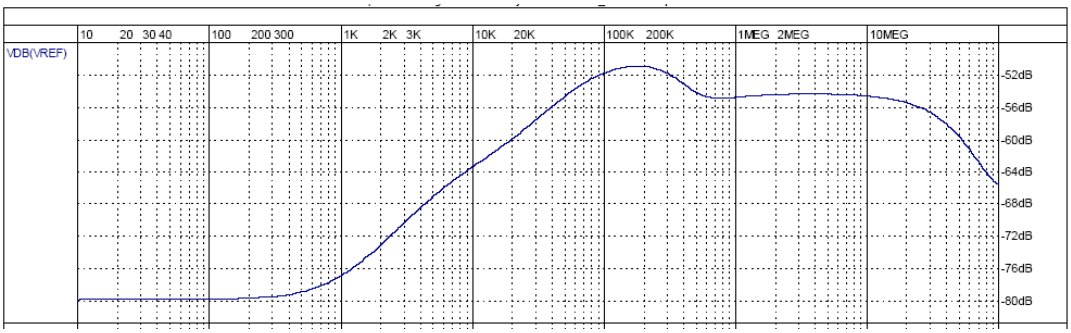


Figure 36: Vref supply noise rejection versus frequency (typical)

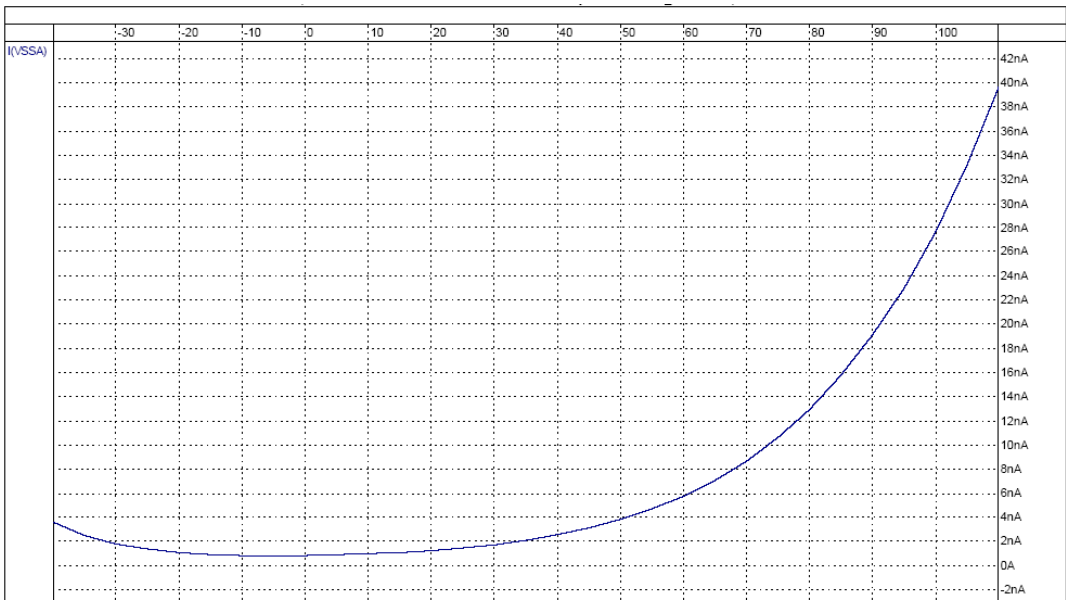


Figure 37: Voltage reference standby current with temperature (typical)

Supply Voltage Sensor

The supply voltage sensor transfer function is:

$$V_{OUT} = \frac{AV_{DD}}{K_V}$$

To calculate the AVDD supply voltage from the ADC result value:

$$AV_{DD} = \frac{R}{2066} = R \times 0.000484$$

$$AV_{DD} = \frac{R \times V_{REF} \times K_V}{4096}$$

where R is the ADC conversion result, V_{REF} is the reference voltage, nominally 1.22V, and K_V is the supply voltage sensor division factor, nominally 13/8 = 1.625.

Temperature Sensor

This table lists the performance characteristics of the on-chip temperature sensor over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.62V to 1.98V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TS}	Temperature sensor voltage	25°C	587	597	607	mV
ΔV_{TS}	Tolerance	Device mismatch		±26.7		mV
	Temperature coefficient	Excluding device mismatch	1.98	2.01	2.04	mV/°C
	Accuracy	without calibration		±18		°C

Table 55: Temperature sensor characteristics

The temperature sensor transfer function is:

$$V_{OUT} = 0.547 + (0.00201 \times T)$$

where V_{OUT} is in Volts and T is the device temperature in °C. The ADC transfer function for single-ended inputs is:

$$\text{ADCoutput } R = 4096 \times \left(\frac{V_{IN}}{V_{REF}}\right)$$

where V_{REF} is 1.22V nominally. To calculate the temperature from the ADC result value:

$$T = \frac{(R - 1836) \times V_{REF}}{4096 \times 0.00201}$$

$$T = (R - 1836) \times 0.1482$$

where R is the ADC conversion result.

Power-On Reset

This table lists the performance characteristics of the on-chip power-on reset circuit over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.45V to 1.98V.

Symbol	Parameter	Min	Typ	Max	Units
AV_{DD}	Supply voltage	1.45	1.8	1.98	V
V_{TH+}	AV_{DD} Threshold Voltage (Rising)	1.542	1.555	1.583	V
$V_{TH–}$	AV_{DD} Threshold Voltage (Falling)	1.511	1.525	1.553	V
ΔV	Hysteresis	29	30	31	mV
T_{POR}	Reset Output Time	25	44	74	µs

Table 56: Power-on reset characteristics

The eCOG1X has an internal supply voltage sense circuit used for the power-on reset function. It is designed for use with nominal power supply voltages between 1.62 and 1.98V and provides a reset indication when the supply voltage is below 1.55V.

The reset output is active low and has an open-drain driver. On the smaller QFN package variants, the power-on reset circuit output signal is available on the bidirectional nReset pin. On the larger 208BGA package, it is available on the Reset_Out pin, and in normal use this is connected externally to the Reset_In pin. External circuits to support additional reset input signals from a user pushbutton or hardware watchdog may be connected to the nReset or nReset_Out pin, provided they have an open-drain output.

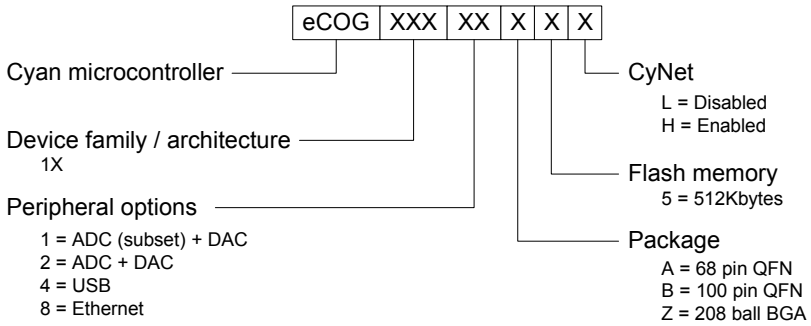
VDD Low Voltage Sensor

This table lists the performance characteristics of the VDD low voltage sensor over the full range of process variation, operating temperature and supply voltage.
T_j = –40°C to +85°C, AVDD = 1.45V to 1.98V.

Symbol	Parameter	Min	Typ	Max	Units
V_{TH+}	V_{DD} Threshold Voltage (Rising)	2.729	2.779	2.829	V
$V_{TH–}$	V_{DD} Threshold Voltage (Falling)	2.668	2.718	2.768	V
ΔV	Hysteresis		60		mV

Table 57: VDD low voltage sensor characteristics

Part Number Description



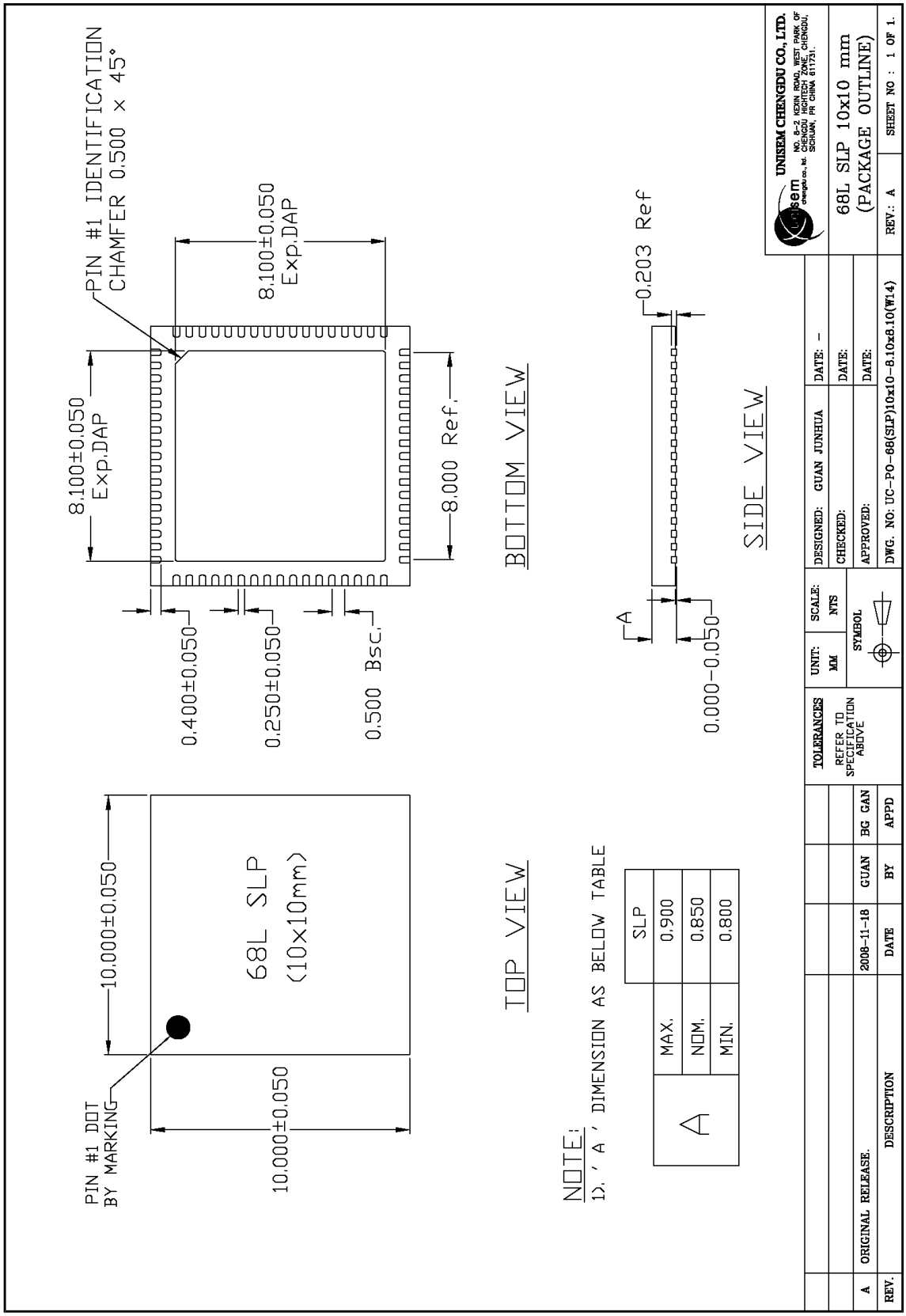
Ordering Information

Part number	Flash size	ETH	USB	ADC	DAC	I/Os	Package	CyNet
eCOG1X0A5L	512K					44	68QFN	Disabled
eCOG1X1A5L	512K			4	2	36	68QFN	
eCOG1X4A5L	512K		Y			40	68QFN	
eCOG1X5A5L	512K		Y	4	2	32	68QFN	
eCOG1X8A5L	512K	Y				44	68QFN	
eCOG1X9A5L	512K	Y		4	2	36	68QFN	
eCOG1X10B5L	512K	Y		11	2	60	100QFN	
eCOG1X14B5L	512K	Y	Y	11	2	56	100QFN	
eCOG1X10Z5L	512K	Y		14	2	120	208BGA	
eCOG1X14Z5L	512K	Y	Y	14	2	120	208BGA	
eCOG1X0A5H	512K					44	68QFN	Enabled
eCOG1X1A5H	512K			4	2	36	68QFN	
eCOG1X4A5H	512K		Y			40	68QFN	
eCOG1X5A5H	512K		Y	4	2	32	68QFN	
eCOG1X8A5H	512K	Y				44	68QFN	
eCOG1X9A5H	512K	Y		4	2	36	68QFN	
eCOG1X10B5H	512K	Y		11	2	60	100QFN	
eCOG1X14B5H	512K	Y	Y	11	2	56	100QFN	
eCOG1X10Z5H	512K	Y		14	2	120	208BGA	
eCOG1X14Z5H	512K	Y	Y	14	2	120	208BGA	

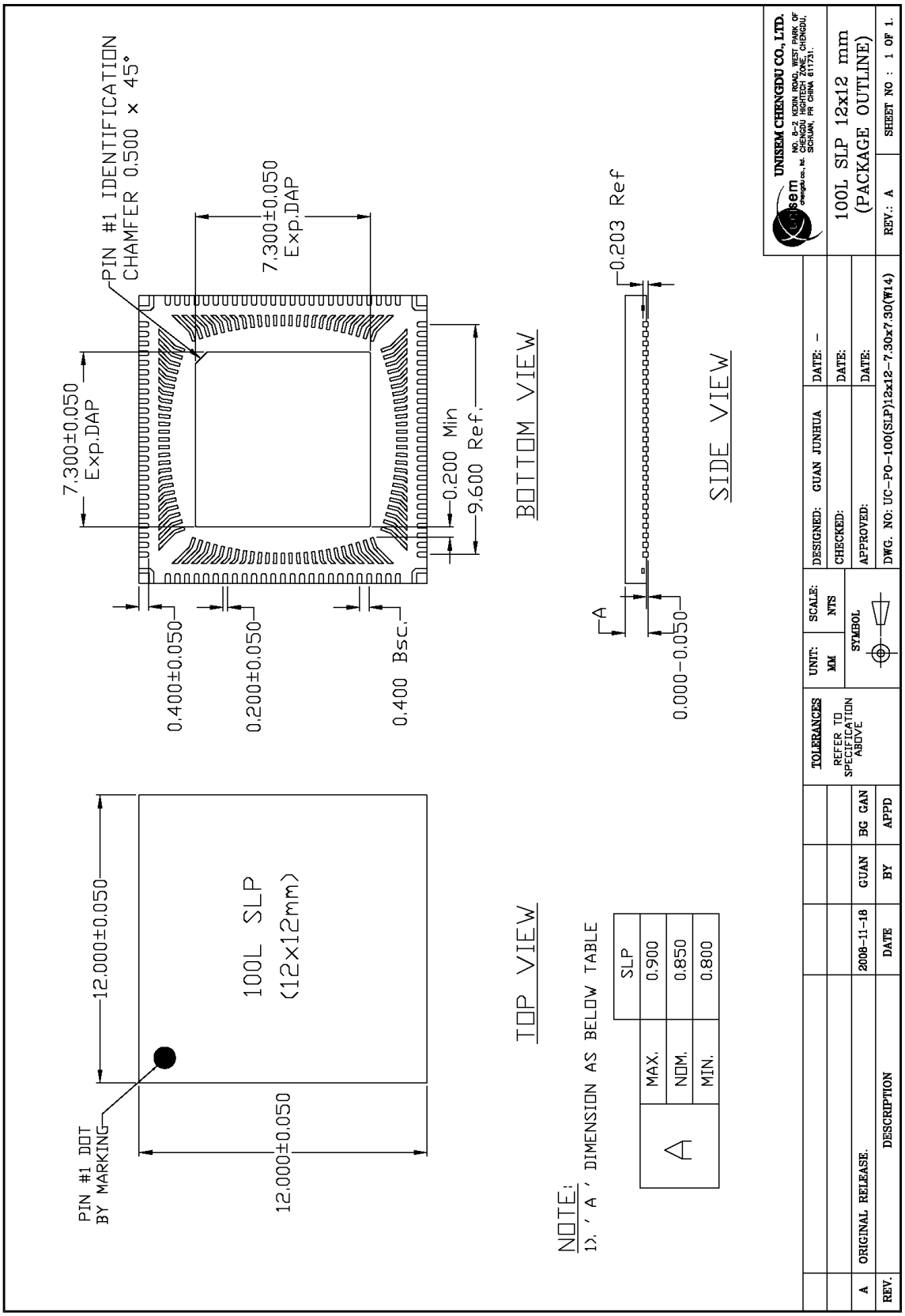
Table 58: eCOG1X Ordering Information

Mechanical Package Drawings

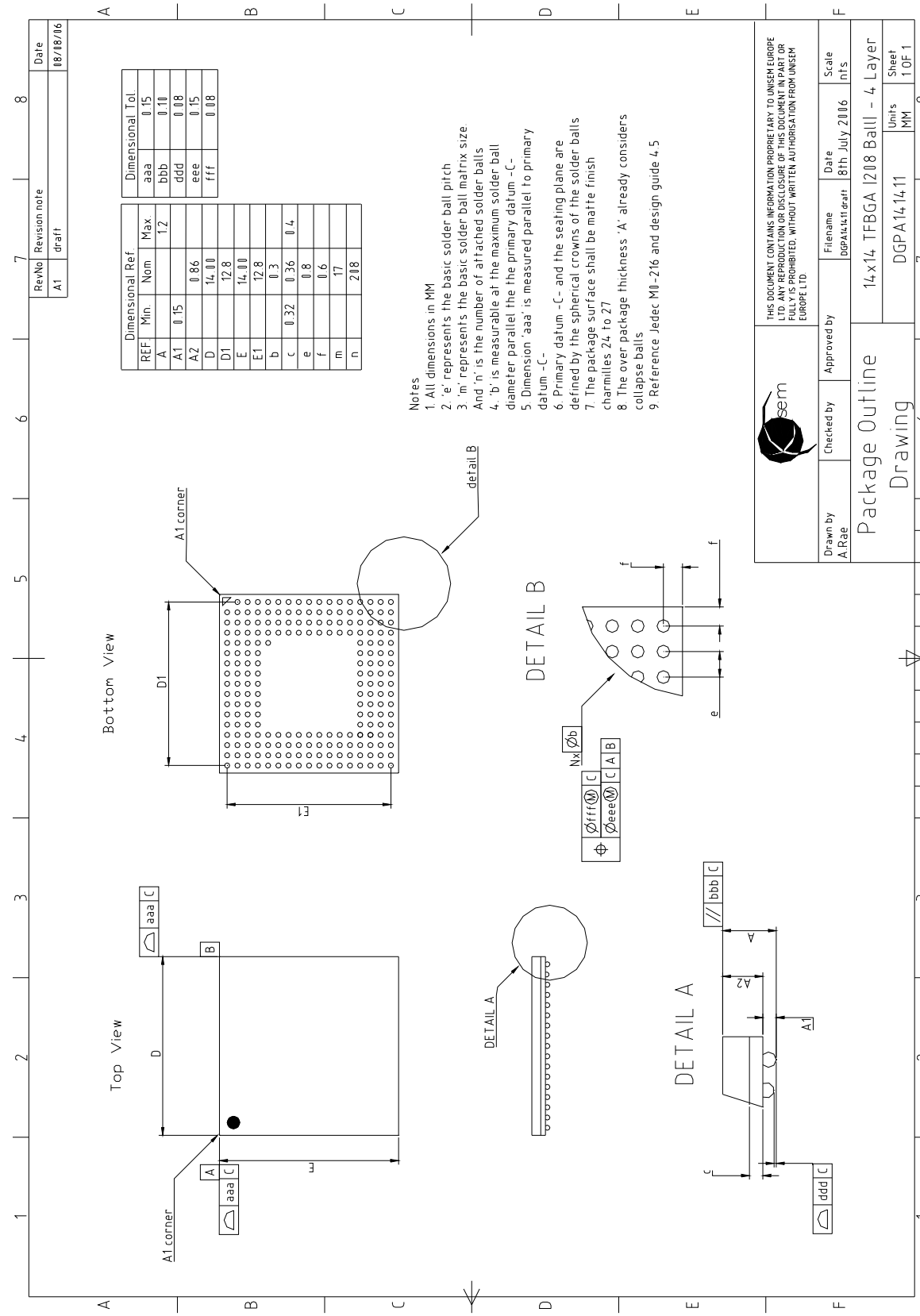
68QFN



100QFN



208BGA

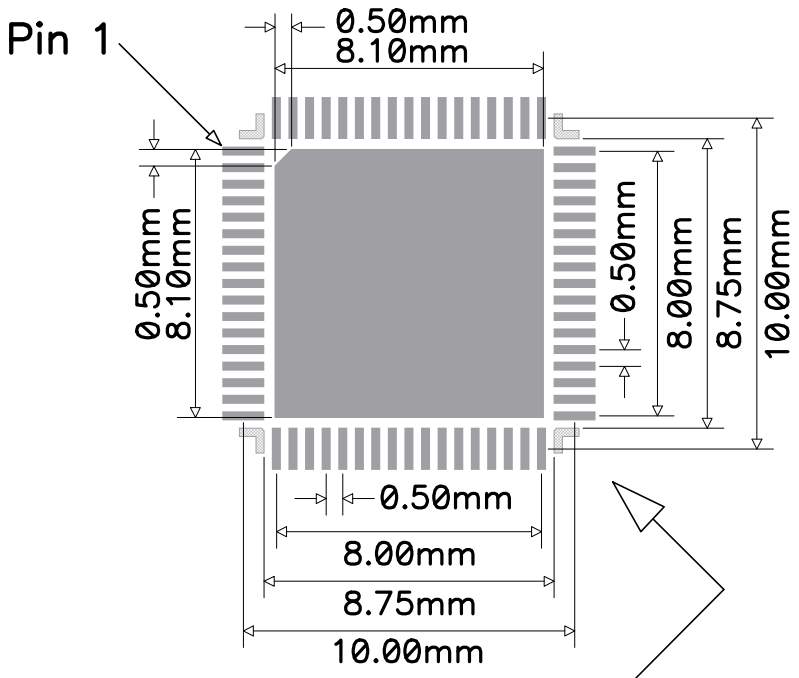


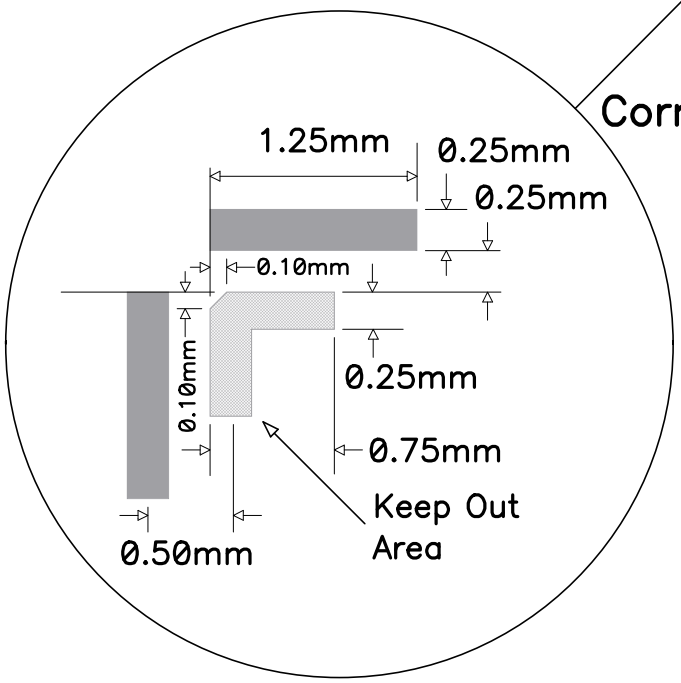
Circuit Board Pad Layout Drawings

68QFN

Rev.	Date	Comment
1.0	29/01/08	Initial Creation

Cyan Technology 68QFN Package Footprint Drawing





NOTES:

The corner Keep Out areas protect accidental connection to the corner L shaped pads on the package.

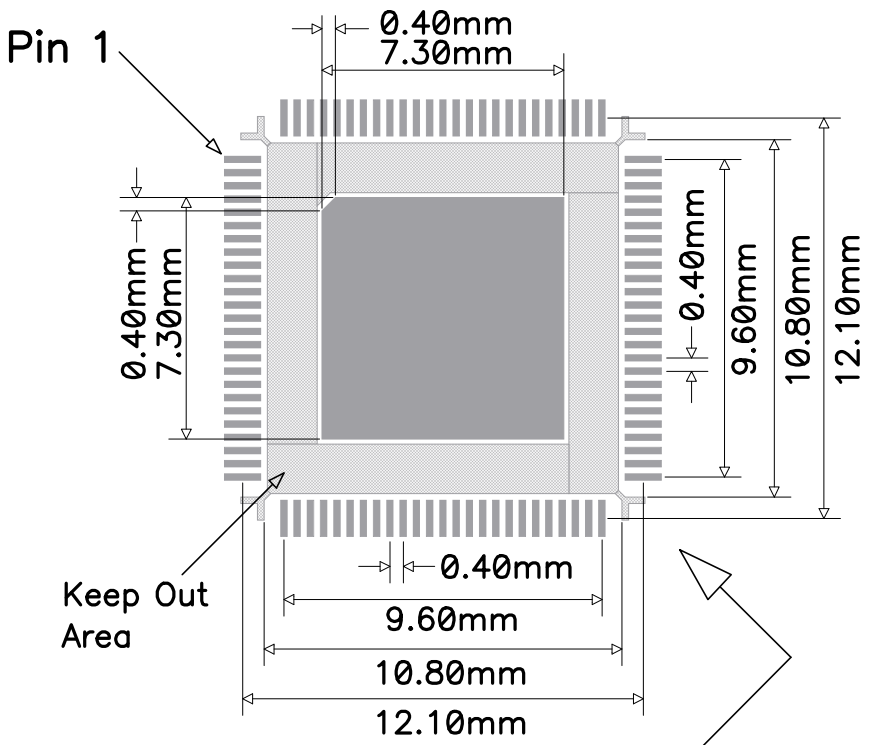
These corner pads are electrically connected to the central ground pad.

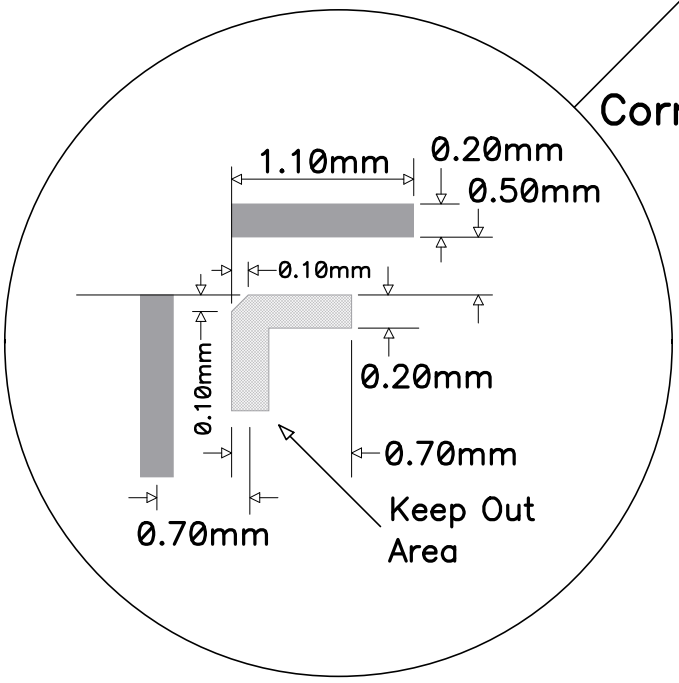
The paste mask for the central ground pad should limit the area pasted to approximatly 30% of the total pad area. Consult with your assembly house for details.

100QFN

Rev.	Date	Comment
1.0	29/01/08	Initial Creation

Cyan Technology 100QFN Package Footprint Drawing





Corner Detail

NOTES:

The corner Keep Out areas protect accidental connection to the corner L shaped pads on the package.

These corner pads are electrically connected to the central ground pad.

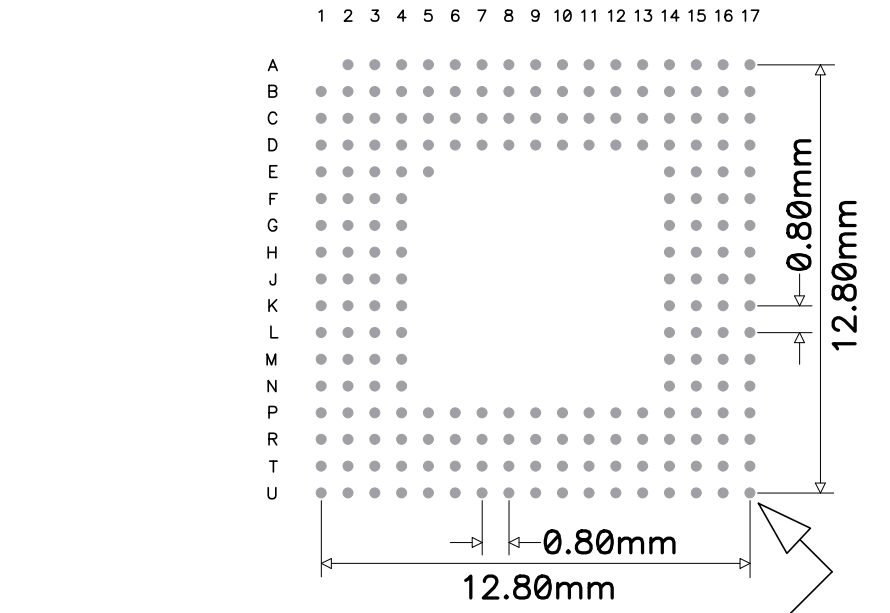
No tracking should be placed between the central pad and the outer pads.

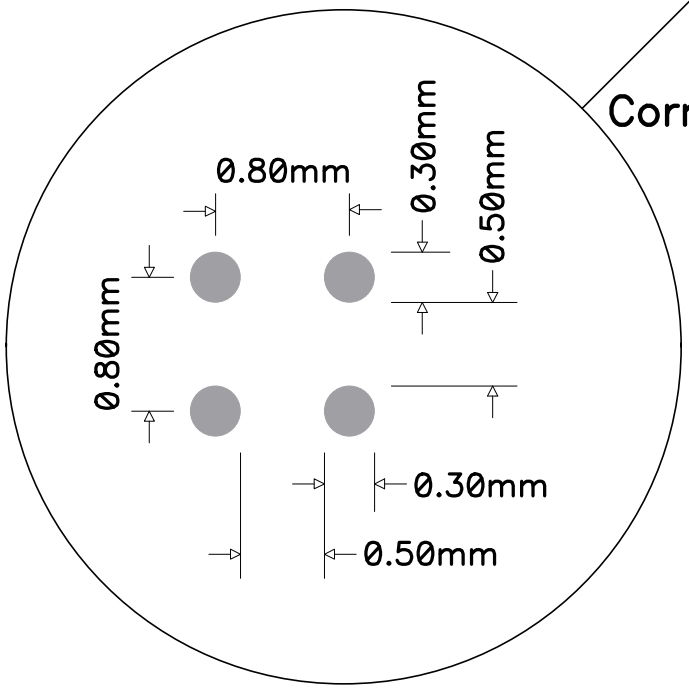
The paste mask for the central ground pad should limit the area pasted to approximatly 30% of the total pad area. Consult with your assembly house for details.

208BGA

Rev.	Date	Comment
1.0	29/01/08	Initial Creation

Cyan Technology 208BGA Package Footprint Drawing





NOTES:

The pad size is a suggestion only and your PCB Manufacturer should be consulted as to their preferences and specifications.

The selection of Solder Mask Defined (SMD) or Non Solder Mask Defined (NSMD) pads should be made in consultation with your PCB Assembler.

Notes

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I2C and the I2C interface are patented by Philips Semiconductor in certain territories.

Philips may demand a royalty or licence fee from designs using the I2C interface.

Declaration of RoHS Compliance

Cyan Technology Ltd hereby declares that the eCOG1X is in full compliance with the European Directive 2002/95/EC, The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS).

This declaration is made based on data provided by our material suppliers, and independent analysis of all homogenous materials used in the manufacture of the product.

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