Features

- Fast Read Access Time – 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum (Standard)
    2 ms Maximum (Option – Ref. AT28HC64BF Datasheet)
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5 V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- Green (Pb/Halide-free) Packaging Option

64K (8K x 8) High Speed Parallel EEPROM with Page Write and Software Data Protection

AT28HC64B

1. Description

The AT28HC64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

5. DC and AC Operating Range

	AT28HC64B-70	AT28HC64B-90	AT28HC64B-120
Operating Temperature (Case)	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply	5 V ±10%	5 V ±10%	5 V ±10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be VIL or VIH.
2. See “AC Write Waveforms” on page 8.
3. VH = 12.0 V ±0.5 V.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} + 0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

8. DC Characteristics

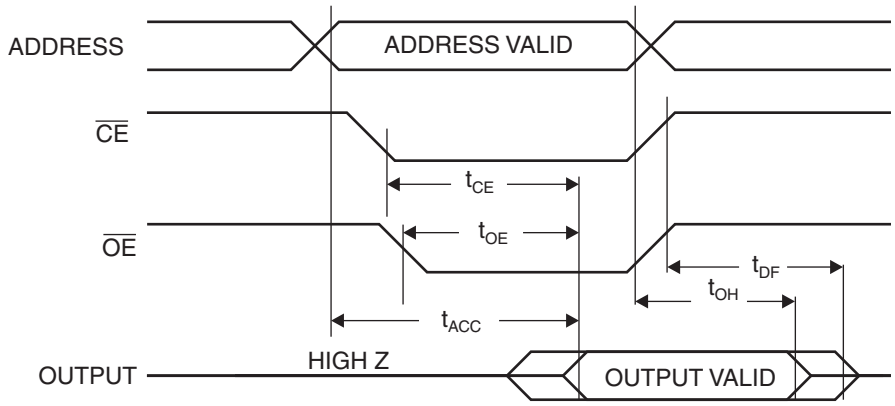
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC} + 1 V		100[1]	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		2[1]	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. I_{SB1} and I_{SB2} for the 55 ns part is 40 mA maximum.

9. AC Read Characteristics

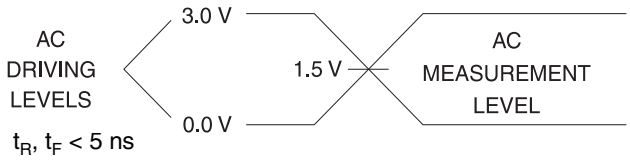
Symbol	Parameter	AT28HC64B-70		AT28HC64B-90		AT28HC64B-120		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF}[3][4]	$\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold	0		0		0		ns

10. AC Read Waveforms[1][2][3][4]

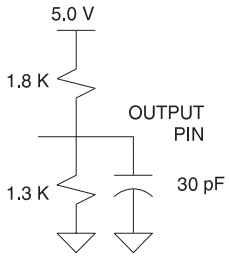


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

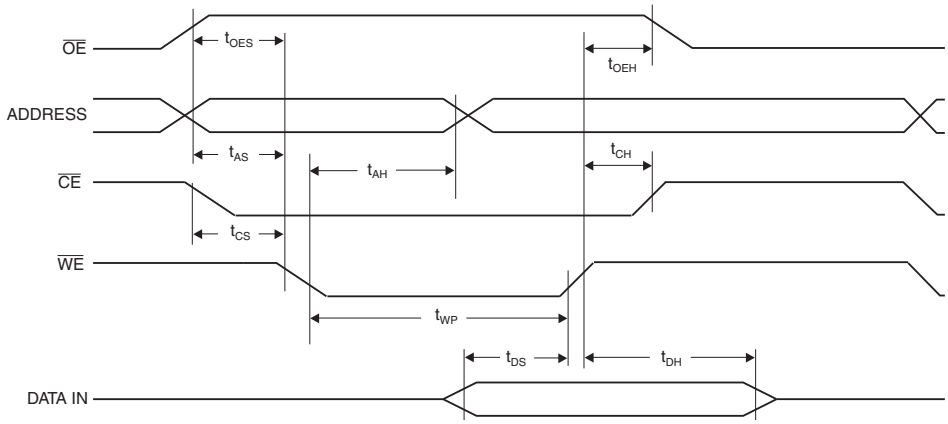
Note: 1. This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

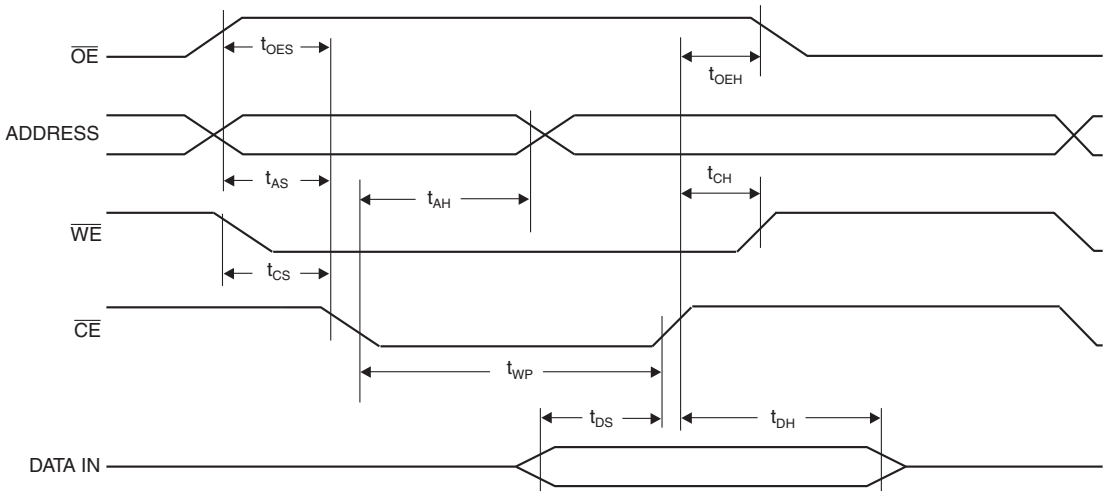
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled



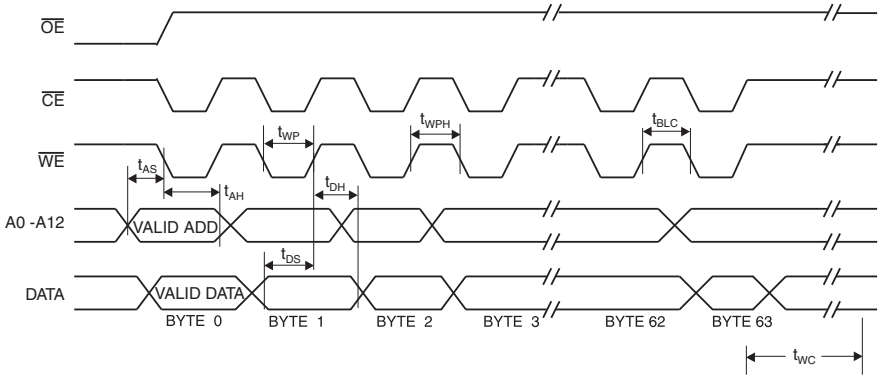
15.2 $\overline{CE}$ Controlled



16. Page Mode Characteristics

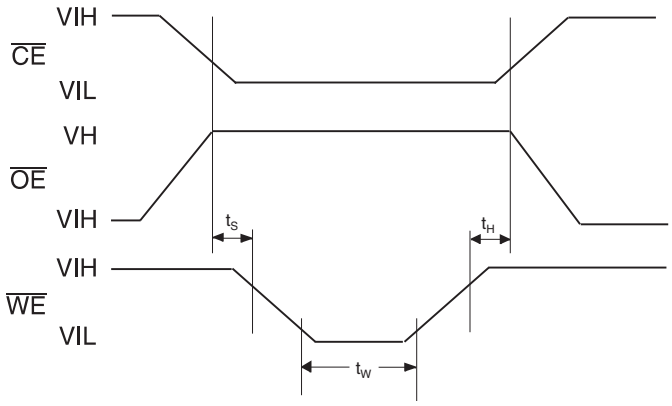
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{WC}	Write Cycle Time (Use AT28HC64BF))		2	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

17. Page Mode Write Waveforms(1)(2)



Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

18. Chip Erase Waveforms



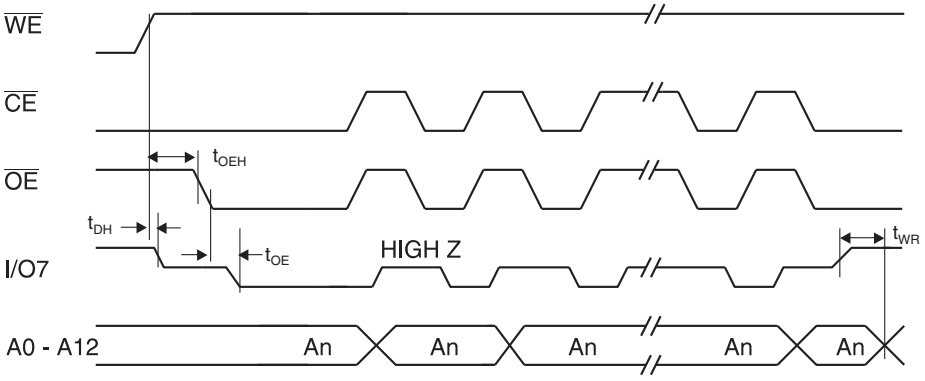
$t_S = t_H = 5$ µs (min.)
$t_W = 10$ ms (min.)
$V_H = 12.0$ V ±0.5 V

22. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[1]				ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested. See “AC Read Characteristics” on page 6.

23. $\overline{\text{Data}}$ Polling Waveforms

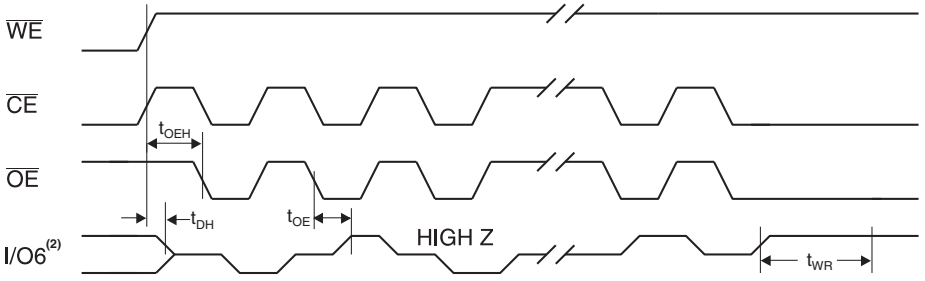


24. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See “AC Read Characteristics” on page 6.

25. Toggle Bit Waveforms[1][2][3]



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

27. Ordering Information[1]

27.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	40	0.1	AT28HC64B-70JI AT28HC64B-70PI AT28HC64B-70SI AT28HC64B-70TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
90	40	0.1	AT28HC64B-90JI AT28HC64B-90PI AT28HC64B-90SI AT28HC64B-90TI	32J 28P6 28S 28T	
120	40	0.1	AT28HC64B-12JI AT28HC64B-12PI AT28HC64B-12SI AT28HC64B-12TI	32J 28P6 28S 28T	

Note: 1. See “Valid Part Numbers” on page 13.

27.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	40	0.1	AT28HC64B-70TU AT28HC64B-70JU AT28HC64B-70SU	28T 32J 28S	Industrial (-40°C to 85°C)
90	40	0.1	AT28HC64B-90JU AT28HC64B-90PU AT28HC64B-90SU AT28HC64B-90TU	32J 28P6 28S 28T	
120	40	0.1	AT28HC64B-12JU AT28HC64B-12SU	32J 28S	

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

28. Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

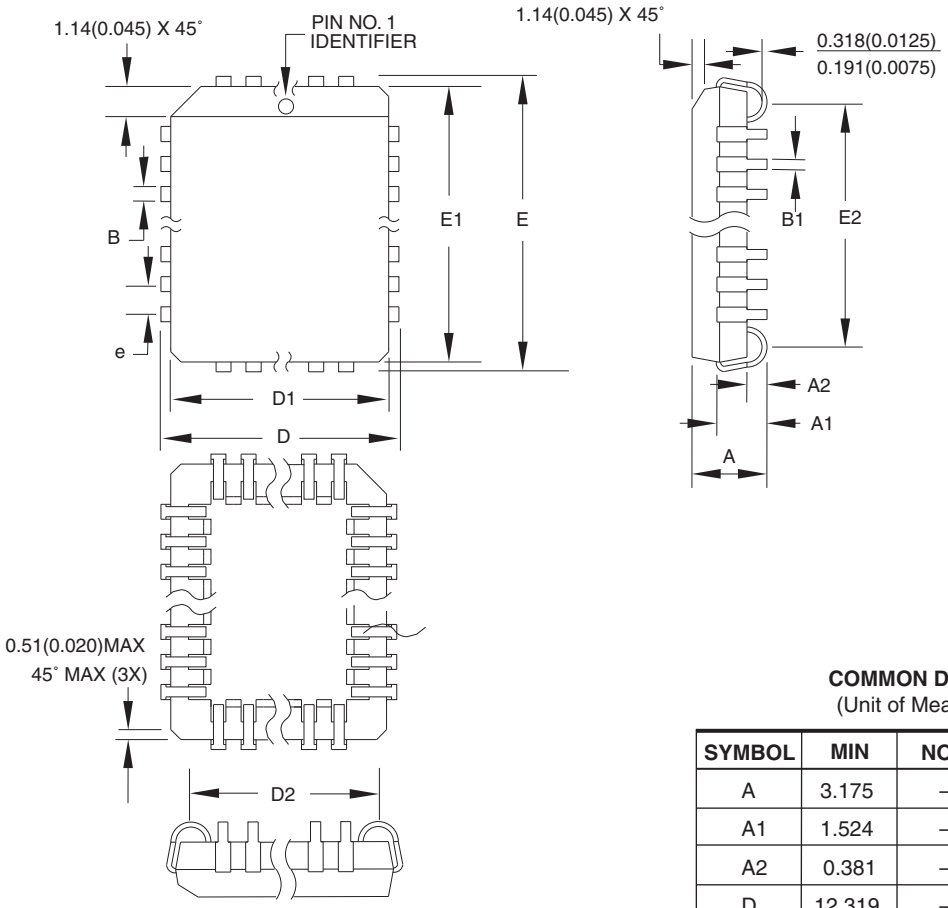
Device Numbers	Speed	Package and Temperature Combinations
AT28HC64B	70	JI, PI, SI, TI, TU, JU, SU
AT28HC64B	90	JI, JU, PI, PU, SI, SU, TI, TU
AT28HC64B	12	JI, JU, PI, PU, SI, SU, TI, TU

29. Die Products

Reference Section: Parallel EEPROM Die Products

30. Packaging Information

30.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B