Data Sheet FN2920.10

2MHz, Super Chopper-Stabilized Operational Amplifier

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering ***improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wider*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial temperature range.***

Intersil's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lockup.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14 lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

Features

- *Guaranteed* Max Input Offset Voltage for *All* Temperature Ranges
- Low Long-Term and Temperature Drifts of Input Offset Voltage
- *Guaranteed* Max Input Bias Current 10pA
- *Extremely Wide* Common Mode Voltage Range. . . . . +3.5V to -5V
- *Reduced* Supply Current 2mA
- *Guaranteed* Minimum Output Source/Sink Current
- Extremely High Gain 150dB
- Extremely High CMRR and PSRR 140dB
- High Slew Rate 2.5V/µs
- Wide Bandwidth 2MHz
- Unity-Gain Compensated
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output
- *Improved, Direct* Replacement for Industry-Standard ICL7650 and other Second-Source Parts
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7650SCBA-1	7650S CBA-1	0 to +70	8 Ld SOIC	M8.15
ICL7650SCBA-1T	7650S CBA-1	0 to +70	8 Ld SOIC (Tape and Reel)	M8.15
ICL7650SCBA-1Z (Note)	7650S CBA-1Z	0 to +70	8 Ld SOIC	M8.15
ICL7650SCBA-1ZT (Note)	7650S CBA-1Z	0 to +70	8 Ld SOIC (Tape and Reel)	M8.15
ICL7650SCPA-1	7650S CPA-1	0 to +70	8 Ld PDIP	E8.3
ICL7650SCPA-1Z (Note)	7650S CPA-1Z	0 to +70	8 Ld PDIP* (Pb-free)	E8.3
ICL7650SCPD	ICL7650SCPD	0 to +70	14 Ld PDIP	E14.3
ICL7650SCPDZ	7650SCPDZ	0 to +70	14 Ld PDIP* (Pb-free)	E14.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications. NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (V+ to V-). 18V
Input Voltage . . . . . (V+ +0.3) to (V- -0.3)
Voltage on Oscillator Control Pins . . . . . V+ to V-
Duration of Output Short Circuit. . . . . Indefinite
Current to Any Pin 10mA
While Operating (Note 1) 100µA

Operating Conditions

Temperature Range
ICL7650SC. . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead PDIP Package*	110	N/A
14 Lead PDIP Package	90	N/A
8 Lead SOIC Package	160	N/A

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . -55°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Limiting input current to 100µA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	***V_{OS}***		+25	-	***±0.7***	***±5***	µV
			0 to +70	-	***±1***	***±8***	µV
Average Temperature Coefficient of Input Offset Voltage (Note 3)	***$\Delta V_{OS}/\Delta T$***		0 to +70	-	***0.02***	-	µV/°C
Change in Input Offset with Time	$\Delta V_{OS}/\Delta T$		+25	-	100	-	$nV/\sqrt{month}$
Input Bias Current |I(+)|, |I(-)|	***I_{BIAS}***		+25	-	4	10	pA
			0 to +70	-	***5***	***20***	pA
Input Offset Current |I(-), |I(+)|	***I_{OS}***		+25	-	***8***	***20***	pA
			0 to +70	-	***10***	***40***	pA
Input Resistance	R_{IN}		+25	-	10^{12}	-	Ω
Large Signal Voltage Gain (Note 3)	***A_{VOL}***	R_L = 10kΩ, V_O = ±4V	+25	***135***	***150***	-	dB
			0 to +70	***130***	-	-	dB
Output Voltage Swing (Note 4)	V_{OUT}	R_L = 10kΩ	+25	±4.7	±4.85	-	V
		R_L = 100kΩ	+25	-	±4.95	-	V
Common Mode Voltage Range (Note 3)	***CMVR***		+25	-5	***-5.2 to +4***	***3.5***	V
			0 to +70	-5	-	***3.5***	V
Common Mode Rejection Ratio (Note 3)	***CMRR***	CMVR = -5V to +3.5V	+25	***120***	***140***	-	dB
			0 to +70	***120***	-	-	dB
Power Supply Rejection Ratio	***PSRR***	V_S = ±3V to ±8V	+25	120	***140***	-	dB
Input Noise Voltage	e_N	R_S = 100Ω, f = DC to 10Hz	+25	-	2	-	μV_{P-P}
Input Noise Current	i_N	f = 10Hz	+25	-	0.01	-	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP		+25	-	2	-	MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ	+25	-	2.5	-	V/µs
Rise Time	t_R		+25	-	0.2	-	µs
Overshoot	OS		+25	-	20	-	%
Operating Supply Range	V+ to V-		+25	4.5	-	16	V
Supply Current	***I_{SUPP}***	No Load	+25	-	2	***3***	mA
			0 to +70	-	-	***3.2***	mA

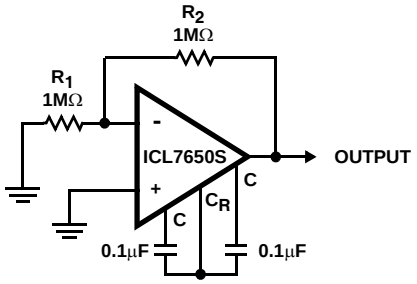
Electrical Specifications V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Output Source Current	$I_{O\ SOURCE}$		+25	2.9	4.5	-	mA
			0 to +70	2.3	-	-	mA
Output Sink Current	$I_{O\ SINK}$		+25	25	30	-	mA
			0 to +70	20	-	-	mA
Internal Chopping Frequency	f_{CH}	Pins 13 and 14 Open	+25	120	250	375	Hz
Clamp ON Current (Note 5)		R_L = 100kΩ	+25	25	70	-	µA
Clamp OFF Current (Note 5)		-4V ≤ V_{OUT} ≤ +4V	+25	-	***0.001***	***5***	nA
			0 to +70	-	-	***10***	nA

NOTES:

3. These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.
4. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
5. See OUTPUT CLAMP under detailed description.
6. All significant improvements over the industry-standard ICL7650 are highlighted in ***bold italics.***

Test Circuit



Application Information

Detailed Description

AMPLIFIER

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feed forward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

INTERMODULATION

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

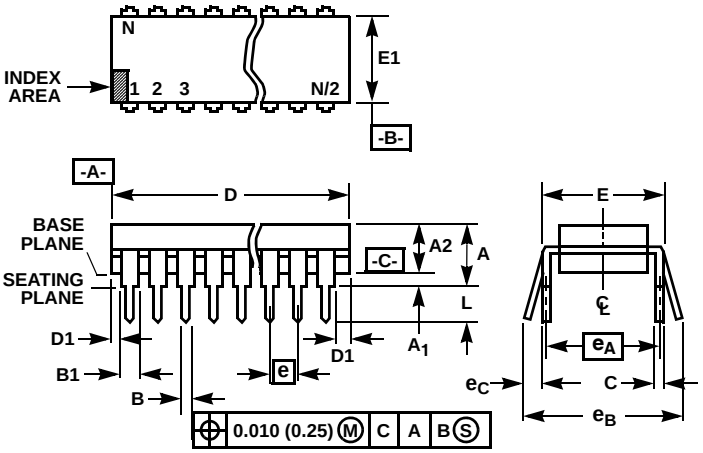
CAPACITOR CONNECTION

The null/storage capacitors should be connected to the CEXTA and CEXTB pins, with a common connection to the CRETN pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to CRETN.

OUTPUT CLAMP

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differentials are avoided, together with the consequent charge buildup on the correction-storage capacitors. The output swing is slightly reduced.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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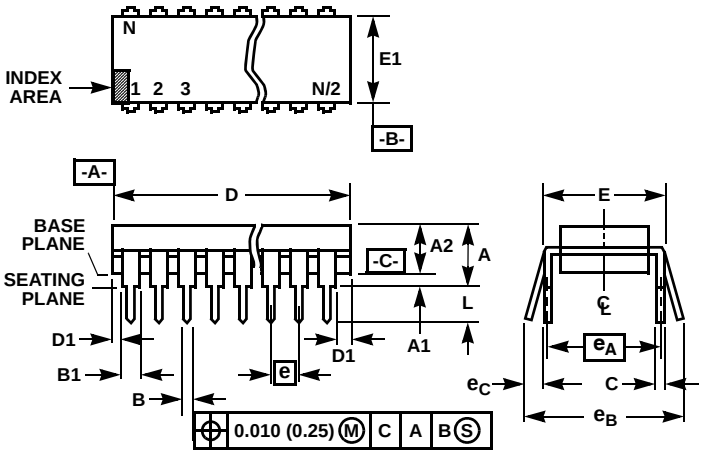
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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