500 MHz, G = +1 and +2 Triple Video Buffers with Disable

AD8074/AD8075

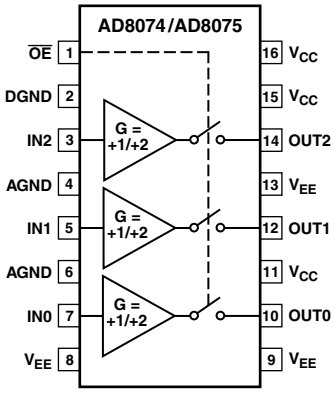
FEATURES

Dual Supply ±5 V
High-Speed Fully Buffered Inputs and Outputs
600 MHz Bandwidth (–3 dB) 200 mV p-p
500 MHz Bandwidth (–3 dB) 2 V p-p
1600 V/μs Slew Rate, G = +1
1350 V/μs Slew Rate, G = +2
Fast Settling Time: 4 ns
Low Supply Current: <30 mA
Excellent Video Specifications (R_L = 150 Ω):
Gain Flatness of 0.1 dB to 50 MHz
0.01% Differential Gain Error
0.01° Differential Phase Error
"All Hostile" Crosstalk
–80 dB @ 10 MHz
–50 dB @ 100 MHz
High "OFF" Isolation of 90 dB @ 10 MHz
Low Cost
Fast Output Disable Feature

APPLICATIONS

RGB Buffer in LCD and Plasma Displays
RGB Driver
Video Routers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8074/AD8075 are high-speed triple video buffers with G = +1 and +2 respectively. They have a –3 dB full signal bandwidth in excess of 450 MHz, along with slew rates in excess of 1400 V/μs. With better than –80 dB of all hostile crosstalk and 90 dB isolation, they are useful in many high-speed applications. The differential gain and differential phase error are 0.01% and 0.01°. Gain flatness of 0.1 dB up to 50 MHz makes the AD8074/AD8075 ideal for RGB buffering or driving. They consume less than 30 mA on a ±5 V supply.

Both devices offer a high-speed disable feature that allows the outputs to be put into a high impedance state. This allows the building of larger input arrays while minimizing "OFF" channel output loading. The AD8074/AD8075 are offered in a 16-lead TSSOP package.

Table I. Truth Table

$\overline{OE}$	OUT0, 1, 2
0	IN0, IN1, IN2
1	High Z

REV. A

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AD8074/AD8075–SPECIFICATIONS (T_A = 25°C, V_S = ±5 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth (Small Signal)	V_{IN} = 200 mV p-p, C_L = 5 pF	330/310	600/550		MHz
	V_{IN} = 200 mV p-p, R_L = 150 Ω	250/230	400/400		MHz
–3 dB Bandwidth (Large Signal)	V_{IN} = 2 V p-p, C_L = 5 pF	330/300	500/500		MHz
	V_{IN} = 2 V p-p, R_L = 150 Ω	250/230	350/350		MHz
0.1 dB Bandwidth	V_{IN} = 200 mV p-p, C_L = 5 pF		70/65		MHz
	V_{IN} = 200 mV p-p, R_L = 150 Ω		70/65		MHz
Slew Rate	2 V Step, R_L = 1 kΩ/150 Ω		1600/1350		V/µs
Settling Time to 0.1%	2 V Step, R_L = 1 kΩ/150 Ω		4/7.5		ns
NOISE/DISTORTION PERFORMANCE					
Differential Gain	V= 3.58 MHz, 150 Ω		0.01		%
Differential Phase	V= 3.58 MHz, 150 Ω		0.01		Degrees
All Hostile Crosstalk	V= 10 MHz, R_L = 1 kΩ		–80/–74		dB
	V= 100 MHz, R_L = 1 kΩ		–50/–44		dB
OFF Isolation	V= 10 MHz, R_L = 150 Ω		90		dB
Voltage Noise	V= 10 kHz to 100 MHz		19.5/22		nV/√Hz
DC PERFORMANCE					
Voltage Gain Error	No Load		±0.1/±0.2	±0.15/±0.65	%
Input Offset Voltage			2.5	27/40	mV
	T_{MIN} to T_{MAX}		3		mV
Input Offset Drift			10		µV/°C
Input Bias Current			5	9.5/10	µA
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance	Channel Enabled		1.5		pF
	Channel Disabled		1.5		pF
Input Voltage Range			±2.8/±1.4		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	$+V_S$ – 1.95	$+V_S$ – 1.8		V
		$–V_S$ + 2.1	$–V_S$ + 1.8		V
	R_L = 150 Ω	$+V_S$ – 2.35	$+V_S$ – 2.2		V
		$–V_S$ + 2.30	$–V_S$ + 2.2		V
Short Circuit Current (Protected)			70		mA
Output Resistance	Enabled		0.5		Ω
	Disabled	3.5	7.5		MΩ
Output Capacitance	Disabled		2.2		pF
POWER SUPPLY					
Operating Range		±4.5		±5.5	V
Power Supply Rejection Ratio	+PSRR: $+V_S$ = +4.5 V to +5.5 V, $–V_S$ = –5 V	60	74		dB
	–PSRR: $–V_S$ = –4.5 V to –5.5 V, $+V_S$ = +5 V	56	64		dB
Quiescent Current	All Channels "ON"		21.5/24	30	mA
	All Channels "OFF"		3/4	5.5	mA
	T_{MIN} to T_{MAX}		23/26		mA
DIGITAL INPUT					
Logic "1" Voltage	$\overline{OE}$ Input	2.0			V
Logic "0" Voltage	$\overline{OE}$ Input			0.8	V
Logic "1" Input Current	$\overline{OE}$ = 4 V		100		nA
Logic "0" Input Current	$\overline{OE}$ = 0.4 V		1		µA
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)	–40		+85	°C
θ_{JA}	Operating (Still Air)		150.4		°C/W
θ_{JC}	Operating		27.6		°C/W

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

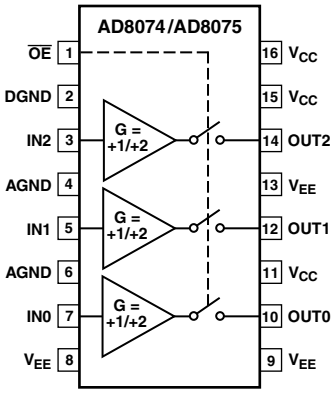
Supply Voltage . . . . . 12.0 V
Internal Power Dissipation[2, 3]
AD8074/AD8075 16-Lead TSSOP (RU) . . . . . 1 W
Input Voltage
IN0, IN1, IN2 . . . . . $V_{EE} \le V_{IN} \le V_{CC}$
$\overline{OE}$ . . . . . DGND $\le V_{IN} \le V_{CC}$
Output Short Circuit Duration . . . . . Indefinite[3]
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air (T_A = 25°C).
[3]16-lead plastic TSSOP; θ_{JA} = 150.4°C/W. Maximum internal power dissipation (P_D) should be derated for ambient temperature (T_A) such that $P_D < (150°C - T_A)/\theta_{JA}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8074ARU	–40°C to +85°C	16-Lead Plastic TSSOP	RU-16
AD8075ARU	–40°C to +85°C	16-Lead Plastic TSSOP	RU-16
AD8074-EVAL		Evaluation Board	
AD8075-EVAL		Evaluation Board	

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8074/AD8075 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8074/AD8075 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8074/AD8075 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 1.

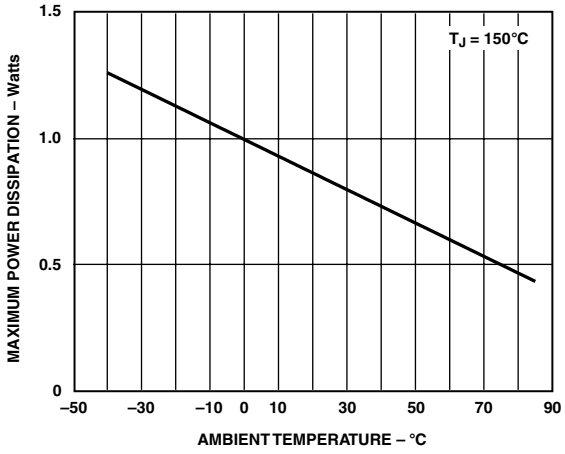


Figure 1. Maximum Power Dissipation vs. Temperature