

Features

- Single Voltage Read/Write Operation: 2.65V to 3.6V
- Access Time – 70 ns
- Sector Erase Architecture
 - Sixty-three 32K Word (64K Bytes) Sectors with Individual Write Lockout
 - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Word Program Time – 10 μ s
- Fast Sector Erase Time – 100 ms
- Suspend/Resume Feature for Erase and Program
 - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
 - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
 - 10 mA Active
 - 15 μ A Standby
- VPP Pin for Write Protection and Accelerated Program Operation
- \overline{WP} Pin for Sector Protection
- \overline{RESET} Input for Device Initialization
- Flexible Sector Protection
- TSOP and CBGA Package Options
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)
- Green (Pb/Halide-free) Packaging

1. Description

The AT49BV320D(T) is a 2.7-volt 32-megabit Flash memory organized as 2,097,152 words of 16 bits each. The memory is divided into 71 sectors for erase operations. The device is offered in a 48-lead TSOP package and a 47-ball CBGA package. The device has \overline{CE} and \overline{OE} control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “[Flexible Sector Protection](#)” on page 6).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory.

The VPP pin provides data protection. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 10.0V, the program (Dual-word Program command) operation is accelerated.



**32-megabit
(2M x 16)
3-volt Only
Flash Memory**

**AT49BV320D
AT49BV320DT**



21. Command Definition Table

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | |
|-------------------------------------|------------|---------------|-------|---------------------|---------------------------------|---------------|------------------|
| | | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | XX | FF | | | | |
| Sector Erase/Confirm | 2 | XX | 20 | SA ⁽²⁾ | D0 | | |
| Word Program | 2 | XX | 40/10 | Addr | D _{IN} | | |
| Dual-word Program ⁽³⁾ | 3 | XX | E0 | Addr0 | D _{IN0} | Addr1 | D _{IN1} |
| Erase/Program Suspend | 1 | XX | B0 | | | | |
| Erase/Program Resume | 1 | XX | D0 | | | | |
| Product ID Entry | 1 | XX | 90 | | | | |
| Sector Softlock | 2 | XX | 60 | SA ⁽²⁾ | 01 | | |
| Sector Hardlock | 2 | XX | 60 | SA ⁽²⁾ | 2F | | |
| Sector Unlock | 2 | XX | 60 | SA ⁽²⁾ | D0 | | |
| Read Status Register | 2 | XX | 70 | XX | D _{OUT} ⁽⁴⁾ | | |
| Clear Status Register | 1 | XX | 50 | | | | |
| Program Protection Register | 2 | XX | C0 | Addr ⁽⁵⁾ | D _{IN} | | |
| Lock Protection Register – Sector B | 2 | XX | C0 | 80 | FFFD | | |
| Status of Sector B Protection | 2 | XX | 90 | 80 | D _{OUT} ⁽⁶⁾ | | |
| CFI Query | 1 | XX | 98 | | | | |

- Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A7 - A0 (Hex). Address A20 through A8 are don't care.
 2. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 17 - 20 for details).
 3. This fast programming option enables the user to program two words in parallel only when V_{PP} = 9.5V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used during manufacturing purposes only.
 4. The status register bits are output on I/O7 - I/O0.
 5. Any addresses within the user programmable protection register region. Address locations are shown on "Protection Register Addressing Table" on page 16.
 6. If data bit D1 is "0", sector B is locked. If data bit D1 is "1", sector B can be reprogrammed.

22. Absolute Maximum Ratings*

| | |
|---|---------------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to V _{CC} + 0.6V |
| Voltage on V _{PP} with Respect to Ground | -0.6V to +10.0V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



26. DC and AC Operating Range

| | | AT49BV320D(T)-70 |
|------------------------------|------|------------------|
| Operating Temperature (Case) | Ind. | -40°C - 85°C |
| V _{CC} Power Supply | | 2.65V to 3.6V |

27. Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | \overline{RESET} | V _{PP} ⁽¹⁾ | Ai | I/O |
|---------------------------------|-----------------|------------------|-----------------|--------------------|----------------------------------|---|----------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X ⁽²⁾ | Ai | D _{OUT} |
| Program/Erase ⁽³⁾ | V _{IL} | V _{IH} | V _{IL} | V _{IH} | V _{IHPP} ⁽⁴⁾ | Ai | D _{IN} |
| Standby/Program Inhibit | V _{IH} | X ⁽²⁾ | X | V _{IH} | X | X | High-Z |
| Program Inhibit | X | X | V _{IH} | V _{IH} | X | | |
| | X | V _{IL} | X | V _{IH} | X | | |
| | X | X | X | V _{IH} | V _{ILPP} ⁽⁵⁾ | | |
| Output Disable | X | V _{IH} | X | V _{IH} | X | | High-Z |
| Reset | X | X | X | V _{IL} | X | X | High-Z |
| Product Identification Software | | | | V _{IH} | | A0 = V _{IL} , A1 - A20 = V _{IL} | Manufacturer Code ⁽⁶⁾ |
| | | | | | | A0 = V _{IH} , A1 - A20 = V _{IL} | Device Code ⁽⁶⁾ |

Notes: 1. The VPP pin can be tied to V_{CC}. For faster program operations, V_{PP} can be set to 9.5V ± 0.5V.

2. X can be V_{IL} or V_{IH}.

3. Refer to AC programming waveforms on [page 26](#).

4. V_{IHPP} (min) = 1.65V.

5. V_{ILPP} (max) = 0.4V.

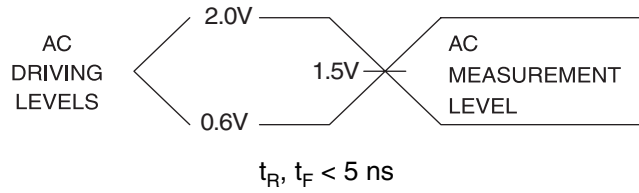
6. Manufacturer Code: 001FH, Device Code: 90C5H – AT49BV320D; 90C4H – AT49BV320DT

28. DC Characteristics

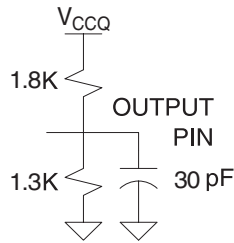
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|-------------------------------|---|-----------------|-----|------|---------|
| I_{LI} | Input Load Current | $V_{IN} = 0V$ to V_{CC} | | | 2 | μA |
| I_{LO} | Output Leakage Current | $V_{IO} = 0V$ to V_{CC} | | | 2 | μA |
| I_{SB} | V_{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V_{CC} | | 15 | 25 | μA |
| $I_{CC}^{(1)}$ | V_{CC} Active Read Current | $f = 5$ MHz; $I_{OUT} = 0$ mA | | 10 | 15 | mA |
| I_{CC1} | V_{CC} Programming Current | | | | 25 | mA |
| I_{PP1} | V_{PP} Input Load Current | | | | 10 | μA |
| V_{IL} | Input Low Voltage | | | | 0.6 | V |
| V_{IH} | Input High Voltage | | $V_{CCQ} - 0.6$ | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1$ mA | | | 0.45 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100$ μA | $V_{CCQ} - 0.1$ | | | V |

Note: 1. In the erase mode, I_{CC} is 25 mA.

29. Input Test Waveforms and Measurement Level



30. Output Test Load



31. Pin Capacitance

f = 1 MHz, T = 25°C⁽¹⁾

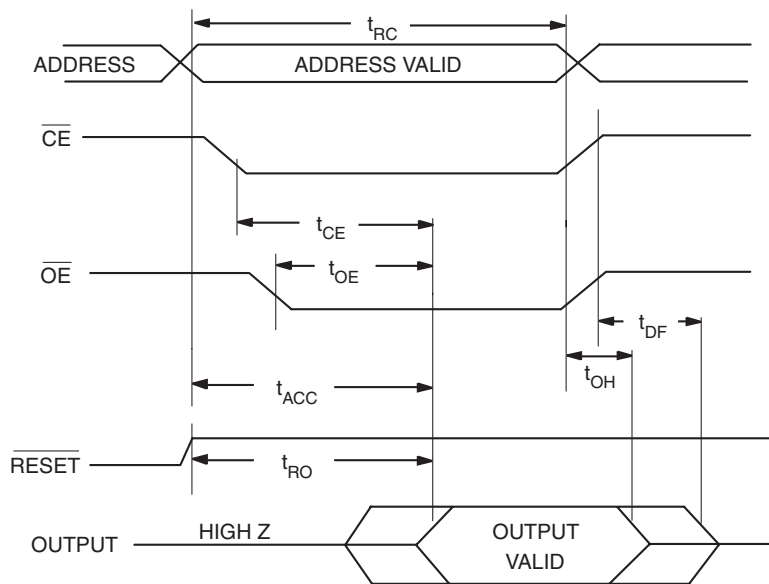
| Symbol | Typ | Max | Units | Conditions |
|------------------|-----|-----|-------|-----------------------|
| C _{IN} | 4 | 6 | pF | V _{IN} = 0V |
| C _{OUT} | 8 | 12 | pF | V _{OUT} = 0V |

Note: This parameter is characterized and is not 100% tested.

32. AC Read Characteristics

| Symbol | Parameter | AT49BV320D(T)-70 | | Units |
|-------------------|---|------------------|-----|-------|
| | | Min | Max | |
| t_{RC} | Read Cycle Time | 70 | | ns |
| t_{ACC} | Address to Output Delay | | 70 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 70 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 20 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 25 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |
| t_{RO} | \overline{RESET} to Output Delay | | 100 | ns |

33. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



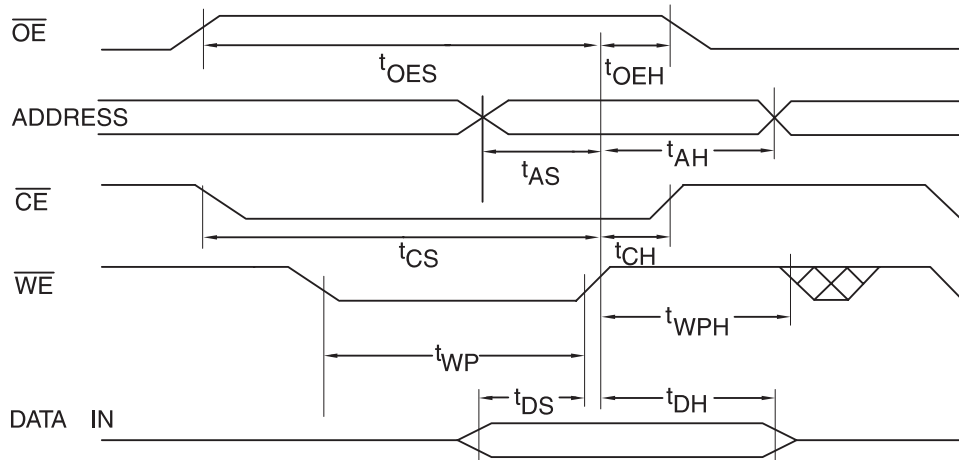
- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

34. AC Word Load Characteristics

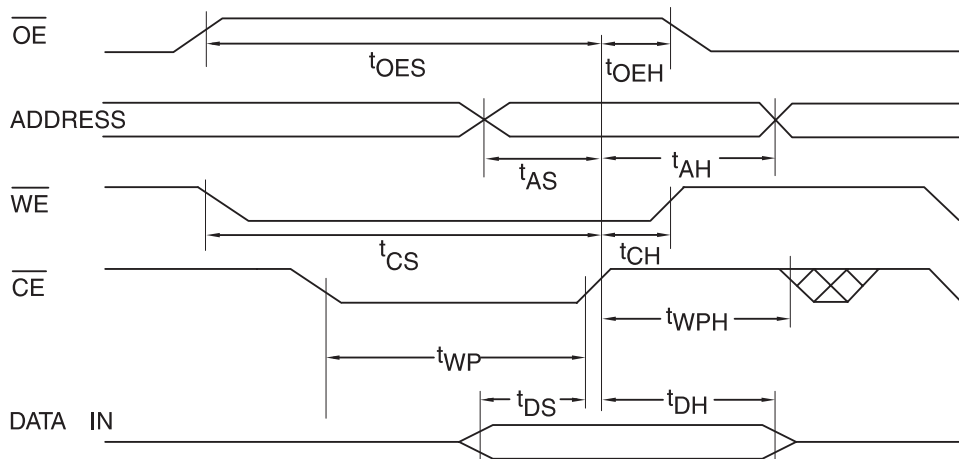
| Symbol | Parameter | Min | Max | Units |
|-------------------|--|-----|-----|-------|
| t_{AS}, t_{OES} | Address, \overline{OE} Setup Time | 20 | | ns |
| t_{AH} | Address Hold Time | 0 | | ns |
| t_{CS} | Chip Select Setup Time | 0 | | ns |
| t_{CH} | Chip Select Hold Time | 0 | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 25 | | ns |
| t_{WPH} | Write Pulse Width High | 15 | | ns |
| t_{DS} | Data Setup Time | 25 | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 0 | | ns |

35. AC Word Load Waveforms

35.1 \overline{WE} Controlled



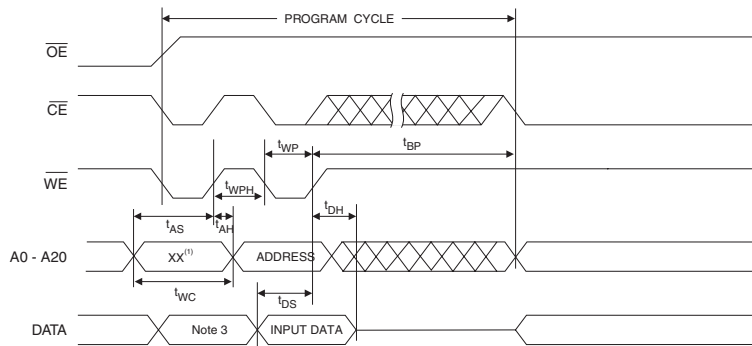
35.2 \overline{CE} Controlled



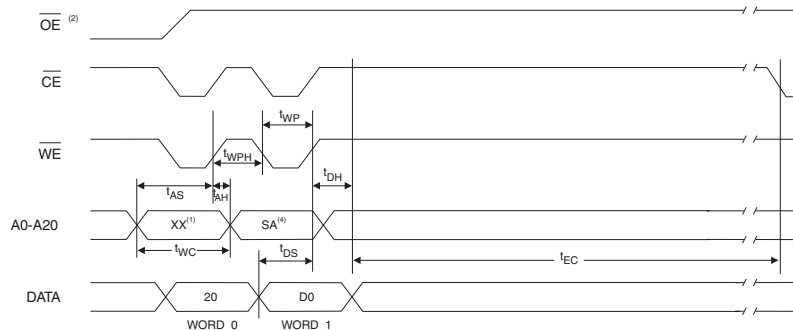
36. Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|------------|--|-----|-----|-----|---------------|
| t_{BP} | Word Programming Time | | 10 | 120 | μs |
| t_{BPD} | Word Programming Time in Dual Programming Mode | | 5 | 60 | μs |
| t_{AS} | Address Setup Time | 20 | | | ns |
| t_{AH} | Address Hold Time | 0 | | | ns |
| t_{DS} | Data Setup Time | 25 | | | ns |
| t_{DH} | Data Hold Time | 0 | | | ns |
| t_{WP} | Write Pulse Width | 25 | | | ns |
| t_{WPH} | Write Pulse Width High | 15 | | | ns |
| t_{WC} | Write Cycle Time | 70 | | | ns |
| t_{RP} | $\overline{\text{Reset}}$ Pulse Width | 500 | | | ns |
| t_{SEC1} | Sector Erase Cycle Time (4K Word Sectors) | | 0.1 | 2 | seconds |
| t_{SEC2} | Sector Erase Cycle Time (32K Word Sectors) | | 0.5 | 6.0 | seconds |
| t_{ES} | Erase Suspend Time | | | 15 | μs |
| t_{PS} | Program Suspend Time | | | 10 | μs |

37. Program Cycle Waveforms



38. Sector Erase Cycle Waveforms



- Notes:
1. Any address can be used to load the data.
 2. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
 3. The data can be 40H or 10H.
 4. The address depends on what sector is to be erased.

40. Ordering Information

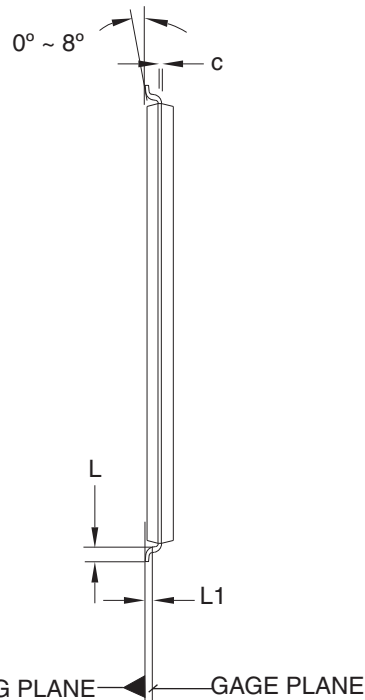
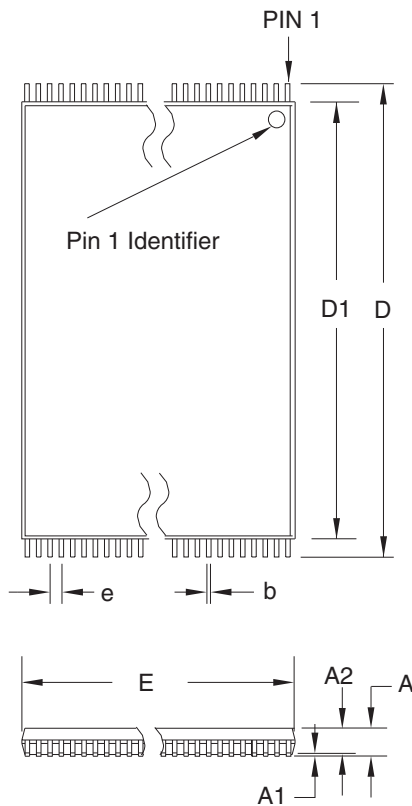
40.1 Green Package (Pb/Halide-free)

| t_{ACC} (ns) | I_{CC} (mA) | | Ordering Code | Package | Operation Range |
|-------------------|---------------|---------|--------------------------------------|-------------|-------------------------------|
| | Active | Standby | | | |
| 70 | 25 | 0.025 | AT49BV320D-70CU AT49BV320D-70TU | 47C1 48T | Industrial (-40° to 85° C) |
| | | | AT49BV320DT-70CU AT49BV320DT-70TU | 47C1 48T | |

| Package Type | |
|--------------|---|
| 47C1 | 47-ball, Plastic Chip-Size Ball Grid Array Package (CBGA) |
| 48T | 48-lead, Plastic Thin Small Outline Package (TSOP) |



41.2 48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 11.90 | 12.00 | 12.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.



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San Jose, CA 95131

TITLE

48T, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)

DRAWING NO.

48T

REV.

B

