

OP292/OP492

FEATURES

Single-Supply Operation: 4.5 V to 33 V
Input Common-Mode Includes Ground
Output Swings to Ground
High Slew Rate: 3 V/ μ s
High Gain Bandwidth: 4 MHz
Low Input Offset Voltage
High Open-Loop Gain
No Phase Inversion
Low Cost

APPLICATIONS

Disk Drives
Mobile Phones
Servo Controls
Modems and Fax Machines
Pagers
Power Supply Monitors and Controls
Battery-Operated Instrumentation

GENERAL DESCRIPTION

The OP292/OP492 are low cost, general purpose dual and quad operational amplifiers designed for single-supply applications and are ideal for 5 volt systems.

Fabricated on Analog Devices' CBCMOS process, the OP292/OP492 series has a PNP input stage that allows the input voltage range to include ground. A BiCMOS output stage enables the output to swing to ground while sinking current.

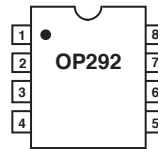
The OP292/OP492 series is unity-gain stable and features an outstanding combination of speed and performance for single- or dual-supply operation. The OP292/OP492 provide high slew rate, high bandwidth, with open-loop gain exceeding 40,000 and offset voltage under 800 Ω (OP292) and 1 mV (OP492). With these combinations of features and low supply current, the OP292/OP492 series is an excellent choice for battery-operated applications.

The OP292/OP492 series performance is specified for single- or dual-supply voltage operation over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$).

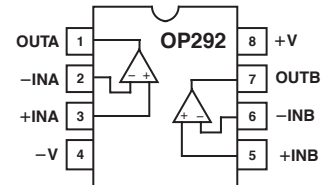
Package options for the OP292 and OP492 include plastic DIP, SO-8 (OP292) and SO-14.

PIN CONNECTIONS

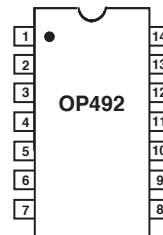
8-Lead Narrow-Body SOIC
(S-Suffix)



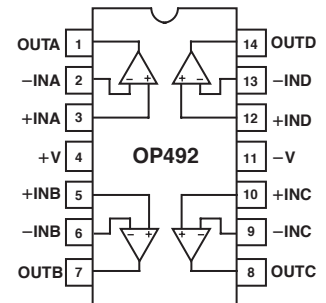
8-Lead Epoxy DIP
(P-Suffix)



14-Lead Narrow-Body SOIC
(S-Suffix)



14-Lead Epoxy DIP
(P-Suffix)



OP292/OP492—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 2\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage OP292	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	0.8	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.3	1.2	mV
Offset Voltage OP492	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.5	2.5	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.1	1	mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.3	1.5	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	2.5	mV
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		450	700	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.75	2.5	μA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }4.0\text{ V}$	75	95		dB
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70	93		dB
Large-Signal Voltage Gain	A_{VO}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	65	90		dB
		$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to }4\text{ V}$	25	200		V/mV
Offset Voltage Drift Long-Term V_{OS} Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	10	100		V/mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	5	50		V/mV
Bias Current Drift	$\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		2	10	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	Note 1	1		$\mu\text{V}/\text{Month}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		6		$\text{pA}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		400		$\text{pA}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.5		$\text{pA}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OUT}	$R_L = 100\text{ k}\Omega$ to GND	4.0	4.3		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				V
Output Voltage Swing Low	V_{OUT}	$R_L = 2\text{ k}\Omega$ to GND	3.8	4.1		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.7	3.9		V
Short-Circuit Current Limit	I_{SC}	$R_L = 100\text{ k}\Omega$ to V+		8	20	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		12	20	mV
Short-Circuit Current Limit	I_{SC}	$R_L = 2\text{ k}\Omega$ to V+		280	450	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		300	550	mV
Short-Circuit Current Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	5	8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 4.5\text{ V to }30\text{ V}$, $V_O = 2\text{ V}$	75	95		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70	90		dB
Supply Current Per Amp OP292, OP492	I_{SY}	$V_O = 2\text{ V}$		0.8	1.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	1	3		V/ μs
Gain Bandwidth Product	GBP			2		V/ μs
Phase Margin	ϕ_m			4		MHz
Channel Separation	CS	$f_O = 1\text{ kHz}$		75		Degrees
Channel Separation	CS			100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		15		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.7		$\text{pA}/\sqrt{\text{Hz}}$

NOTES

¹Long-term offset voltage drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C with LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 5\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 2\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage OP292	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.0	2.0	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.2	2.5	mV
Offset Voltage OP492	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.5	3	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.4	2.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.7	2.8	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	3	mV
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		375	700	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.5	1	μA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		7	50	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	100	nA
Large-Signal Voltage Gain	A_{VO}	Note 1	-11		11	V
		$V_{CM} = \pm 11\text{ V}$	78	100		dB
Offset Voltage Drift Bias Current Drift	$\Delta V_{OS}/\Delta T$ $\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		75	95	dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	120	V/mV
Offset Voltage Drift Bias Current Drift	$\Delta V_{OS}/\Delta T$ $\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		10	75	V/mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	60	V/mV
Offset Voltage Drift Bias Current Drift	$\Delta V_{OS}/\Delta T$ $\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4	10	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		3		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$ to GND	± 11	± 12.2		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	± 10	± 11		V
Short-Circuit Current Limit	I_{SC}	$R_L = 100\text{ k}\Omega$ to GND	± 13.8	± 14.3		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	± 13.5	± 14.0		mV
		Short Circuit to GND	8	10.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.25\text{ V}$ to $\pm 15\text{ V}$	75	86		dB
		$40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70	83		dB
Supply Current Per Amp OP292, OP492	I_{SY}	$V_O = 0\text{ V}$		1	1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate		SR $R_L = 10\text{ k}\Omega$	2.5	4		V/ μs
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2	3		V/ μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			75		Degrees
Channel Separation	CS	$f_0 = 1\text{ k Hz}$		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ k Hz}$		15		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.7		$\text{pA}/\sqrt{\text{Hz}}$

NOTES

¹Input voltage range is guaranteed by CMRR tests.

Specifications subject to change without notice.

OP292/OP492

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	33 V
Input Voltage ²	-15 V to +14 V
Differential Input Voltage ²	V
Output Short-Circuit Duration	UNLIMITED
Storage Temperature Range	
P, S Package	-65°C to +150°C
Operating Temperature Range	
OP292/OP492 P, S	-40°C to +125°C
Junction Temperature Range	
P, S Package	-65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Package Type	θ_{JA} ³	θ_{JC}	Unit
8-Pin Plastic DIP (P)	103	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin SOIC (S)	120	36	°C/W

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

²For supply voltages less than 36 V, the absolute maximum input voltage is equal to the supply voltage.

³ θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

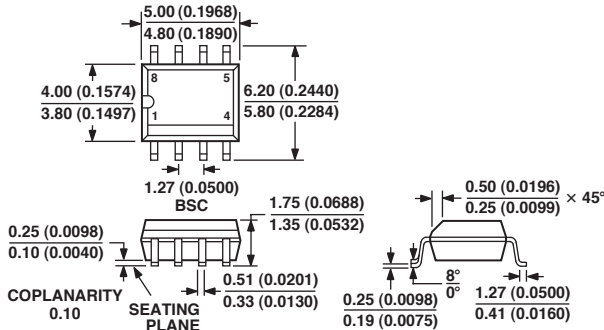
Model	Temperature Range	Package Option
OP292GP*	-40°C to +125°C	N-8
OP292GS	-40°C to +125°C	RN-8
OP492GP*	-40°C to +125°C	N-14
OP492GS	-40°C to +125°C	RN-14

*Not for new design, obsolete April 2002.

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC] Narrow Body (RN-8)

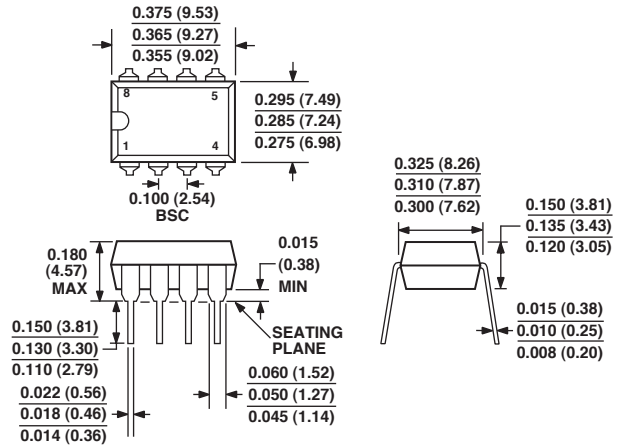
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-in-Line Package [PDIP] (N-8)

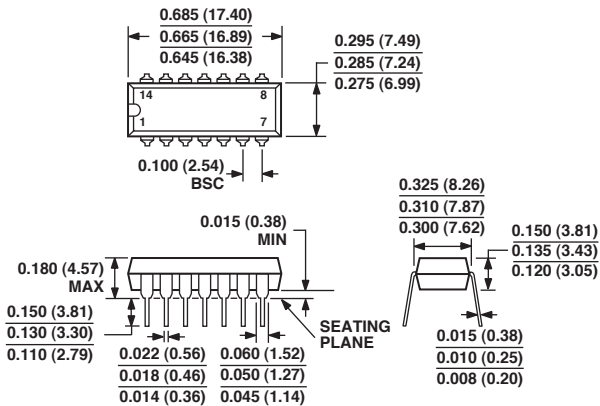
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES)

14-Lead Plastic Dual-in-Line Package [PDIP] (N-14)

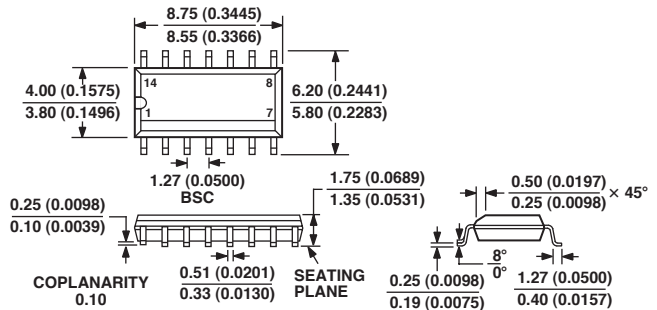
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095-AB
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14-Lead Standard Small Outline Package [SOIC] Narrow Body (RN-14)

Dimensions shown in millimeters and (inches)



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