

FEATURES

- Broad-range analog variable gain: -2.5 dB to $+42.5$ dB**
- 3 dB cutoff frequency of 500 MHz**
- Gain up and gain down modes**
- Linear-in-dB, scaled 20 mV/dB**
- Resistive ground referenced input**
- Nominal $Z_{IN} = 200 \Omega$**
- On-chip, square-law detector**
- Single-supply operation: 2.7 V to 5.5 V**

APPLICATIONS

- Cellular base stations**
- Broadband access**
- Power amplifier control loops**
- Complete, linear IF AGC amplifiers**
- High speed data I/O**

GENERAL DESCRIPTION

The AD8367 is a high performance 45 dB variable gain amplifier with linear-in-dB gain control for use from low frequencies up to several hundred megahertz. The range, flatness, and accuracy of the gain response are achieved using Analog Devices' X-AMP® architecture, the most recent in a series of powerful proprietary concepts for variable gain applications, which far surpasses what can be achieved using competing techniques.

The input is applied to a 9-stage, 200Ω resistive ladder network. Each stage has 5 dB of loss, giving a total attenuation of 45 dB. At maximum gain, the first tap is selected; at progressively lower gains, the tap moves smoothly and continuously toward higher attenuation values. The attenuator is followed by a 42.5 dB fixed gain feedback amplifier—essentially an operational amplifier with a gain bandwidth product of 100 GHz—and is very linear, even at high frequencies. The output third order intercept is $+20$ dBV at 100 MHz ($+27$ dBm, re 200Ω), measured at an output level of 1 V p-p with $V_S = 5$ V.

FUNCTIONAL BLOCK DIAGRAM

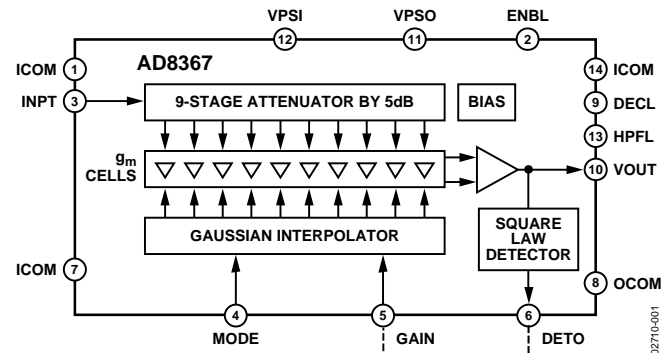


Figure 1.

The analog gain-control input is scaled at 20 mV/dB and runs from 50 mV to 950 mV. This corresponds to a gain of -2.5 dB to $+42.5$ dB, respectively, when the gain up mode is selected and $+42.5$ dB to -2.5 dB, respectively, when gain down mode is selected. The gain down, or inverse, mode must be selected when operating in AGC in which an integrated square-law detector with an internal setpoint is used to level the output to 354 mV rms, regardless of the crest factor of the output signal. A single external capacitor sets up the loop averaging time.

The AD8367 can be powered on or off by a voltage applied to the ENBL pin. When this voltage is at a logic LO, the total power dissipation drops to the milliwatt range. For a logic HI, the chip powers up rapidly to its normal quiescent current of 26 mA at 25°C. The AD8367 is available in a 14-lead TSSOP package for the industrial temperature range of -40°C to $+85^\circ\text{C}$.

Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

SPECIFICATIONS

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, system impedance $Z_O = 200\ \Omega$, $V_{\text{MODE}} = 5\text{ V}$, $f = 10\text{ MHz}$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		LF		500	MHz
GAIN Range			45		dB
INPUT STAGE					
Maximum Input	Pins INPT and ICOM To avoid input overload		700		mV p-p
Input Resistance	From INPT to ICOM	175	200	225	Ω
GAIN CONTROL INTERFACE					
Scaling Factor	Pin GAIN $V_{\text{MODE}} = 5\text{ V}$, $50\text{ mV} \leq V_{\text{GAIN}} \leq 950\text{ mV}$ $V_{\text{MODE}} = 0\text{ V}$, $50\text{ mV} \leq V_{\text{GAIN}} \leq 950\text{ mV}$		+20		mV/dB
Gain Law Conformance	$100\text{ mV} \leq V_{\text{GAIN}} \leq 900\text{ mV}$		± 0.2		dB
Maximum Gain	$V_{\text{GAIN}} = 0.95\text{ V}$		+42.5		dB
Minimum Gain	$V_{\text{GAIN}} = 0.05\text{ V}$		-2.5		dB
V_{GAIN} Step Response	From 0 dB to 30 dB		300		ns
	From 30 dB to 0 dB		300		ns
Small Signal Bandwidth	$V_{\text{GAIN}} = 0.5\text{ V}$		5		MHz
OUTPUT STAGE					
Maximum Output Voltage Swing	Pin VOUT $R_L = 1\text{ k}\Omega$ $R_L = 200\ \Omega$		4.3		V p-p
Output Source Resistance	Series resistance of output buffer		3.5		V p-p
Output Centering Voltage ¹			50		Ω
			$V_S/2$		V
SQUARE LAW DETECTOR					
Output Set Point	Pin DETO		354		mV rms
AGC Small Signal Response Time	$C_{\text{AGC}} = 100\text{ pF}$, 6 dB gain step		1		μs
POWER INTERFACE					
Supply Voltage	Pins VPSI, VPSO, ICOM, and OCOM	2.7		5.5	V
Total Supply Current	ENBL high, maximum gain, $R_L = 200\ \Omega$ (includes load current)		26	30	mA
Disable Current vs. Temperature	ENBL low $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1.3	1.6	mA
				1.8	mA
MODE CONTROL INTERFACE					
Mode LO Threshold	Pin MODE Device in negative slope mode of operation		1.2		V
Mode HI Threshold	Device in positive slope mode of operation		1.4		V
ENABLE INTERFACE					
Enable Threshold	Pin ENBL		2.5		V
Enable Response Time	Time delay following LO to HI transition until device meets full specifications.		1.5		μs
Enable Input Bias Current	ENBL at 5 V		27		μA
	ENBL at 0 V		32		nA
$f = 70\text{ MHz}$					
Gain	Maximum gain		+42.5		dB
	Minimum gain		-3.7		dB
Gain Scaling Factor			19.9		mV/dB
Gain Intercept			-5.6		dB
Noise Figure	Maximum gain		6.2		dB
Output IP3	$f_1 = 70\text{ MHz}$, $f_2 = 71\text{ MHz}$, $V_{\text{GAIN}} = 0.5\text{ V}$		36.5		dBm
			29.5		dBV rms
Output 1 dB Compression Point	$V_{\text{GAIN}} = 0.5\text{ V}$		8.5		dBm
			1.5		dBV rms

AD8367

Parameter	Conditions	Min	Typ	Max	Unit
f = 140 MHz					
Gain	Maximum gain		+43.5		dB
	Minimum gain		-3.6		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			-5.3		dB
Noise Figure	Maximum gain		7.4		dB
Output IP3	f1 = 140 MHz, f2 = 141 MHz, V _{GAIN} = 0.5 V		32.7		dBm
			25.7		dBV rms
Output 1 dB Compression Point	V _{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 190 MHz					
Gain	Maximum gain		+43.5		dB
	Minimum gain		-3.8		dB
Gain Scaling Factor			19.6		mV/dB
Gain Intercept			-5.3		dB
Noise Figure	Maximum gain		7.5		dB
Output IP3	f1 = 190 MHz, f2 = 191 MHz, V _{GAIN} = 0.5 V		30.9		dBm
			23.9		dBV rms
Output 1 dB Compression Point	V _{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 240 MHz					
Gain	Maximum gain		+43		dB
	Minimum gain		-4.1		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			-5.2		dB
Noise Figure	Maximum gain		7.6		dB
Output IP3	f1 = 240 MHz, f2 = 241 MHz, V _{GAIN} = 0.5 V		29.2		dBm
			22.2		dBV rms
Output 1 dB Compression Point	V _{GAIN} = 0.5 V		8.1		dBm
			1.1		dBV rms

¹ The output dc centering voltage is normally set at V_S/2 and can be adjusted by applying a voltage to DECL.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_{PSO} , V_{PSI}	5.5 V
ENBL Voltage	$V_s + 200$ mV
MODE Select Voltage	$V_s + 200$ mV
V_{GAIN} Control Voltage	1.2 V
Input Voltage	± 600 mV
Internal Power Dissipation	250 mW
θ_{JA}	150°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

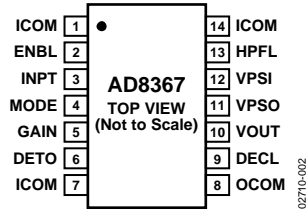


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 14	ICOM	Signal Common. Connect to low impedance ground.
2	ENBL	A HI Activates the Device.
3	INPT	Signal Input. 200 Ω to ground.
4	MODE	Gain Direction Control. HI for positive slope; LO for negative slope.
5	GAIN	Gain Control Voltage Input.
6	DETO	Detector Output. Provides output current for RSSI function and AGC control.
8	OCOM	Power Common. Connect to low impedance ground.
9	DECL	Output Centering Loop Decoupling Pin.
10	VOUT	Signal Output. To be externally ac-coupled to load.
11	VPSO	Positive Supply Voltage. 2.7 V to 5.5 V. VPSI and VPSO are tied together internally with back-to-back PN junctions. They should be tied together externally and properly bypassed.
12	VPSI	Positive Supply Voltage. 2.7 V to 5.5 V.
13	HPFL	High-Pass Filter Connection. A capacitor to ground sets the corner frequency of the output offset control loop.

