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EWM-900-FDTC

Low Cost 902-928MHz Full Duplex
Audio/Data Transceiver

Typical Applications

- Automated Meter Reading
- Wireless Handsets
- On-Site Paging
- Asset Tracking
- Wireless Alarm and Security Systems
- Long Range RFID
- Automated Resource Management

Features

- Low Cost
- 56 Channels
- 3V Operation
- Small Size: 1.22” x 0.82”
- No External Parts are required
- Simple serial programming interface
- RSSI

Description

The EWM-900-FDTC is ideal for unlicensed voice and data applications. The transceiver module requires no external RF components except for the antenna. It is designed to make FCC and ETSI approvals easy.
The transceiver operates in full duplex. It can transmit and receive data and/or voice simultaneously. The receiver section employs a direct-conversion, zero IF architecture, eliminating image frequency interference. The manufacturing-friendly DIP style package and low-cost make the EWM-900-FDTC suitable for high volume applications.

Document Control

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Engineering Review		
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Revision History

Revision	Author	Date	Description
1.0	SJM	10/30/01	Document Created
1.1	SJM	11/18/02	Module pin-out diagram and table corrected
1.2	GWH	01/22/03	Updated.
1.3	TRM	11/26/03	Fixed erroneous frequency table headers
1.4	GWH	2/10/04	Updated to reflect Rev D hardware.

Table of Contents

Table of Figures

Pin Out Diagram

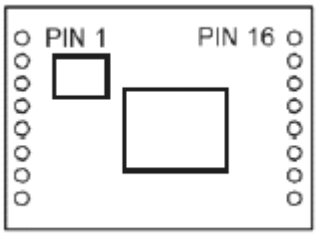

Figure 1, Module Pin Diagram

Pin Description

Pin No.	Pin Name	Description
1	GND	Transceiver Ground. Connect to Ground Plane.
2	ANT	50 ohm Antenna Input.
3	GND	Transceiver Ground. Connect to Ground Plane.
4	GND	Transceiver Ground. Connect to Ground Plane.
5	GND	Transceiver Ground. Connect to Ground Plane.
6	GND	Transceiver Ground. Connect to Ground Plane.
7	AUDIO	Receive Audio Output.
8	NC	No Connection.
9	GND	Transceiver Ground. Connect to Ground Plane.
10	CLK	Serial programming interface clock.
11	DAT	Serial programming interface data.
12	LE	Serial programming interface latch enable.
13	RSSI	Receive Signal Strength Indicator.
14	RXD	Receive Data Output.
15	TXD/AUDIN	Transmit Data/Audio Input.
16	VCC	Power Supply. Vcc should be bypassed with a .01uF ceramic capacitor and filtered with a 4.7uF tantalum capacitor. Noise on the power supply will degrade receiver sensitivity.

Table 1, EWM-900-FDTC Module Pin Description

Mechanical Drawing

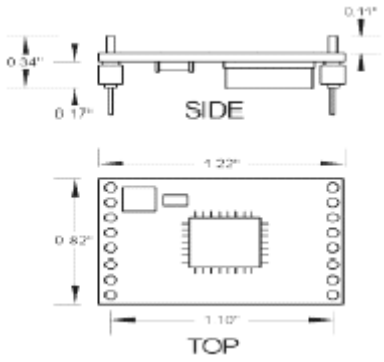

Figure 2, Mechanical Drawing of EWM-900-FDTC

Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supply & all input pins	-0.3	+12	VDC
Soldering Temp (10 sec)		350	°C
Storage Temperature	-50	150	°C
Operating Temperature	0	70	°C

Table 2, Absolute Maximum Ratings

Detailed Electrical Specifications

Parameter (General)	Min	Typ.	Max	Units	Notes
Operating Voltage	2.7	3.0	3.3	Volts DC	
Sleep Current		5		uA	
RX Current		35		mA	
TX Current		26		mA	
Parameter (Receiver)	**Min**	**Typ.**	**Max**	**Units**	**Notes**
Audio Sensitivity		-109		dBm	Note 1
Data Sensitivity		-100		dBm	Note 2
Strong Signal SINAD		44		dB	Note 3
Input IP3		-1		dBm	
Input P1DB		-18		dBm	
Adjacent Channel Rejection		60		dB	
TX Carrier Suppression		45		dB	
LO Feedthrough		-65		dBm	

Audio Output Level		600		mV p-p	
Data High Voltage	Vcc-0.7		Vcc	Volts DC	
Data Low Voltage	0		0.7	Volts DC	
RSSI Voltage Range	0.1		2.1	Volts DC	
RSSI Gain		-32		mV/dB	
RSSI Dynamic Range		65		dB	
Parameter (Transmitter)	**Min**	**Typ.**	**Max**	**Units**	**Notes**
Output Power		0		dBm	Note 4
2nd Harmonic Power		-50		dBm	Note 4
3rd Harmonic Power		-60		dBm	Note 4
4th Harmonic Power		-70		dBm	Note 4
Modulation Bandwidth	0.3		10	kHz	
Data Input High Voltage	Vcc-0.7		Vcc	Volts DC	
Data Input Low Voltage	0		0.7	Volts DC	
Peak Deviation		25		kHz pk	

Table 3, Detailed Electrical Specifications

Notes:

1) 12dB SINAD, 1kHz modulation tone, 25kHz frequency deviation.
2) 19.2kBit/second, 10^{-5} BER, 25kHz p-p deviation.
3) –85dBm input level, 1kHz tone, 25kHz p-p deviation.
4) 50 ohm load.

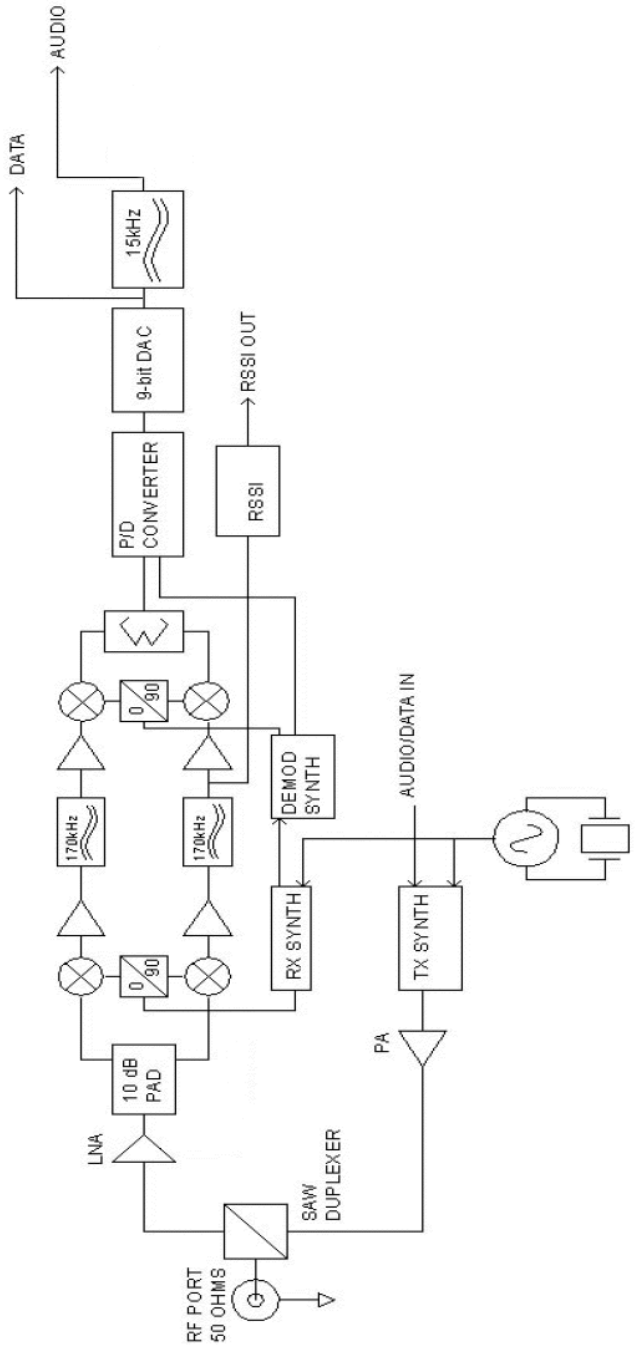

Figure 3: Block Diagram

Figure 3, Block Diagram of Module

Circuit Description

The EWM-900-FDTC is a complete, fully integrated FM/FSK transceiver module capable of full-duplex transmission and reception of voice and data. The transceiver operates on one of 56 channels in the 902-928MHz unlicensed band.

No external RF components (except for the antenna) are required.

The transceiver is configured via a 3-wire serial programming interface comprised of LE, DAT, and CLK. Parameters that can be set using this interface include transmit channel, receive channel, transmit enable, and receive enable.

The unique zero-IF receiver architecture allows for a simple, low-cost solution that does not exhibit the image frequency interference problems of traditional super-het designs.

Theory of Operation

A block diagram of the EWM-900-FDTC transceiver is shown in figure 3.

The antenna input pin is connected directly to the SAW duplexer. The purpose of the duplexer is to separate the receive and transmit frequency bands, effectively combining them while isolating the transmit and receive circuitry. Table 9 shows the frequency plan for -BS (base station) and -HS (handset) versions of the module. It should be noted that -BS modules can only talk to -HS modules and visa-versa because of the complimentary frequency plan.

The receive port of the duplexer is connected to a low noise-amplifier. The purpose of the amplifier is to compensate for the signal loss through the duplexer and to improve the noise figure of the receiver.

After the LNA, the incoming carrier is directly converted to baseband (zero-IF) using a pair of quadrature mixers. Special DC offset correction circuitry is employed to ensure proper operation at zero-IF. After the mixers, the receive chain is split into a quadrature pair (I-chain and Q-chain).

Following the quadrature mixers, a pair of variable gain amplifiers and low-pass-filters are used to amplify and filter the low-level input signal. Because the receiver uses a zero-IF architecture, these filters can be realized on-chip using only resistors and capacitors, reducing the size and cost of the transceiver. The gain of the quadrature down-conversion mixers and variable-gain amplifiers is automatically controlled by an internal AGC circuit. This is done to maintain linearity in the receive chain.

The RSSI circuit derives the RSSI voltage from the Q receive chain.

Demodulation is achieved by up-converting the baseband to 140kHz and digitizing the resultant frequency spectrum. A special P/D circuit is used to demodulate the carrier and generate an analog waveform using a 9-bit D/A converter. In strong signal conditions, this will result in a 44dB SINAD. The analog output is low-pass filtered to remove IF noise.

The demodulated output of the receiver is available at two pins on the module. In data mode, Pin 14 (RXD) should be used. In audio mode, Pin 7 should be used. Pin 14 is the unfiltered output.

The transceiver includes on-board frequency synthesizers for the transmitter and the receiver. These are programmed through the serial programming interface discussed later in this document. The transmitter synthesizer includes a modulation input that can be driven with digital or analog information. There is a 150Hz high-pass filter on this input.

Therefore, DC voltage levels cannot be sent. The output of the transmitter synthesizer is connected to a power amplifier that boosts the output power to +3dBm typical. After the losses through the duplexer, the output transmit power is 0dBm typical.

Configuration

The transceiver is configured by programming four registers via a three-wire serial interface comprised of CLK (pin 10), DAT (pin 11), and LE (pin 12).
When LE is high, bits are shifted in from DAT on each rising edge of CLK. The most significant bit of the most significant byte is shifted in first. Bits 0 and 1 of byte 0 determine which register is programmed.

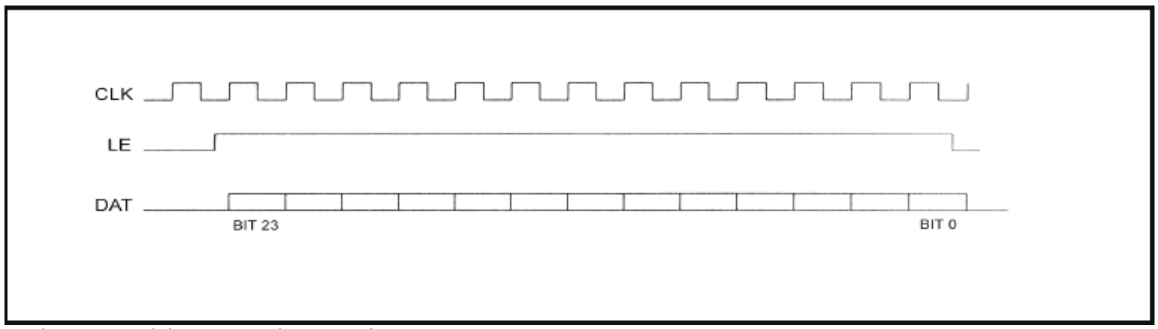

Figure 4, Serial Programming Waveforms.

Reference Frequency Control Register
The value programmed into this register determines the reference frequency for the transceiver. For proper operation, the reference frequency MUST be set to 50kHz. The programming word is:

binary: 00000000 01000011 11000000
hex: 0x0043C0

Bit Position								Byte
7	6	5	4	3	2	1	0	
1	1	0	0	0	0	0	0	**0**
0	1	0	0	0	0	1	1	**1**
0	0	0	0	0	0	0	0	**2**

Table 4, Reference Frequency Register

Bits 0 and 1 of byte 0 of all register programming words are the register select bits, as described in the following table. The reference frequency should be fixed at 50kHz and should not be changed.

Bit 1	Bit 0	Register
0	0	Reference frequency control
0	1	RX VCO control
1	0	TX VCO control
1	1	Mode control

Table 5, Register Address Bits

Each register is either 22 or 23 bits. For consistency's sake, 24 bits should be shifted into the DAT pin to successfully program a register. When LE transitions high, the incoming bits are stored in a shift register until LE transitions low. On the falling edge of the transition, the contents of the shift register are transferred to the appropriate control register.

Bit Position								Byte
7	6	5	4	3	2	1	0	
A Count [2:0]			F Register [2:0]			Register Sel [1:0]		0
A_2	A_1	A_0	F_2	F_1	F_0	0	1	
M Count [5:0]						A Count [4:3]		1
M_5	M_4	M_3	M_2	M_1	M_0	A_4	A_3	
Pad		Trim [1:0]		M Count [9:6]				2
0	0	T_1	T_0	M_9	M_8	M_7	M_6	

Table 6, Receive VCO Register

The receive VCO control register determines the operating channel of the receiver. The receive frequency is determined by the values of the A, F, and M counters. The trim bits are used to adjust the tuning range of the receive VCO. The trim value is determined at the factory and is provided with each module. It is clearly marked on the top of the module in indelible ink on either the module's PCB or, on newer modules, indicated on the product barcode sticker. The number is two digits. The second digit represents the RX VCO trim value.

The actual receive frequency can be calculated using the following formula:

F=50E3 * (32 * M) + A +(F/8)

Example: Calculate the A, M, and F values for a base station (BS) receive frequency of 926 MHz.

M=578
A=24
F=0

For this example, assuming a trim value of 2, the programming word will be:

binary: 00101001 00001011 00000001
hex: 0x290B01

Table 9 lists the receive frequency and register values for each of the 56 receive channels. The table lists these values for both the -BS and -HS versions of the transceiver.

Bit Position								Byte
7	6	5	4	3	2	1	0	
A Count [2:0]			F Register [2:0]			Register Sel [1:0]		0
A_2	A_1	A_0	F_2	F_1	F_0	1	0	
M Count [5:0]						A Count [4:3]		1
M_5	M_4	M_3	M_2	M_1	M_0	A_4	A_3	
Pad	Trim [2:0]			M Count [9:6]				2
0	T_2	T_1	T_0	M_9	M_8	M_7	M_6	

Table 7, Transmit VCO Register

The transmit VCO control register determines the operating channel of the transmitter. The receive frequency is determined by the values of the M, A, and F counters.

Note that the TX register has three trim bits, where the RX register has only two. The trim bits are used to adjust the tuning range of the transmit VCO. The trim value is determined at the factory and is provided with each module. It is clearly marked on the top of the module in indelible ink. The number is two digits. The first digit represents the TX VCO trim value. The actual transmit frequency can be calculated using same formula as for the receive register. See the receive register description for more information on calculating the M, A, and F values.

Table 9 lists the M, A, and F values for each channel. Use this table to quickly determine the values for programming.

Bit Position								Byte
7	6	5	4	3	2	1	0	
0	0	1	TXE	RXE	1	1	1	**0**
0	0	0	0	0	0	0	0	**1**
0	0	0	0	0	0	0	DAT*	**2**

Table 8, Mode Control Register

The mode control register determines the operating modes of the transceiver. With the register, the designer can turn on and off the transmitter and operating channel of the transmitter. The receive frequency is determined by the values of the M, A, and F counters.

Note that the TX register has three trim bits, where the RX register has only two. The trim bits are used to receiver sections of the transceiver. RXE determines the state of the receiver. When the bit is set to 1, the receiver is on. When the bit is set to 0 the bit is off.

TXE determines the state of the transmitter. When the bit set to 1, the transmitter is on. When the bit is set to 0, the bit is off.

The transceiver is placed in power-down mode by turning both the transmitter and receiver off. In this mode, the transceiver will draw <5uA. The on-board crystal oscillator is automatically enabled when either the transmitter or receiver is enabled.

DAT determines the operating mode of the transmitter/receiver. When this bit is set to 1, the internal data-slicer is enabled. This allows data reception.
When the DAT bit is set to 0, then internal data-slicer is disabled for audio reception.

Channel	RX: EWM-900-FDTC-BS TX: EWM-900-FDTC-HS				RX: EWM-900-FDTC-HS TX: EWM-900-FDTC-BS			
	Frequency	M	A	F	Frequency	M	A	F
0	902.250	563	29	0	924.850	578	1	0
1	902.300	563	30	0	924.900	578	2	0
2	902.350	563	31	0	924.950	578	3	0
3	902.400	564	0	0	925.000	578	4	0
4	902.450	564	1	0	925.050	578	5	0
5	902.500	564	2	0	925.100	578	6	0
6	902.550	564	3	0	925.150	578	7	0
7	902.600	564	4	0	925.200	578	8	0
8	902.650	564	5	0	925.250	578	9	0
9	902.700	564	6	0	925.300	578	10	0
10	902.750	564	7	0	925.250	578	11	0
11	902.800	564	8	0	925.400	578	12	0
12	902.850	564	9	0	925.450	578	13	0
13	902.900	564	10	0	925.500	578	14	0
14	902.950	564	11	0	925.550	578	15	0
15	903.000	564	12	0	925.600	578	16	0
16	903.050	564	13	0	925.650	578	17	0
17	903.100	564	14	0	925.700	578	18	0
18	903.150	564	15	0	925.750	578	19	0
19	903.200	564	16	0	925.800	578	20	0
20	903.250	564	17	0	925.850	578	21	0
21	903.300	564	18	0	925.900	578	22	0
22	903.350	564	19	0	925.950	578	23	0
23	903.400	564	20	0	926.000	578	24	0
24	903.450	564	21	0	926.050	578	25	0
25	903.500	564	22	0	926.100	578	26	0
26	903.550	564	23	0	926.150	578	27	0
27	903.600	564	24	0	926.200	578	28	0
28	903.650	564	25	0	926.250	578	29	0
29	903.700	564	26	0	926.300	578	30	0
30	903.750	564	27	0	926.350	578	31	0
31	903.800	564	28	0	926.400	579	0	0
32	903.850	564	29	0	926.450	579	1	0
33	903.900	564	30	0	926.500	579	2	0
34	903.950	564	31	0	926.550	579	3	0
35	904.000	565	0	0	926.600	579	4	0
36	904.050	565	1	0	926.650	579	5	0
37	904.100	565	2	0	926.700	579	6	0
38	904.150	565	3	0	926.750	579	7	0
39	904.200	565	4	0	926.800	579	8	0
40	904.250	565	5	0	926.850	579	9	0
41	904.300	565	6	0	926.900	579	10	0
42	904.350	565	7	0	926.950	579	11	0
43	904.400	565	8	0	927.000	579	12	0
44	904.450	565	9	0	927.050	579	13	0
45	904.500	565	10	0	927.100	579	14	0
46	904.550	565	11	0	927.150	579	15	0
47	904.600	565	12	0	927.200	579	16	0
48	904.650	565	13	0	927.250	579	17	0
49	904.700	565	14	0	927.300	579	18	0
50	904.750	565	15	0	927.350	579	19	0
51	904.800	565	16	0	927.400	579	20	0
52	904.850	565	17	0	927.450	579	21	0
53	904.900	565	18	0	927.500	579	22	0
54	904.950	565	19	0	927.550	579	23	0
55	905.000	565	20	0	927.600	579	24	0

Table 9, Receive/Transmit Channel Programming Table

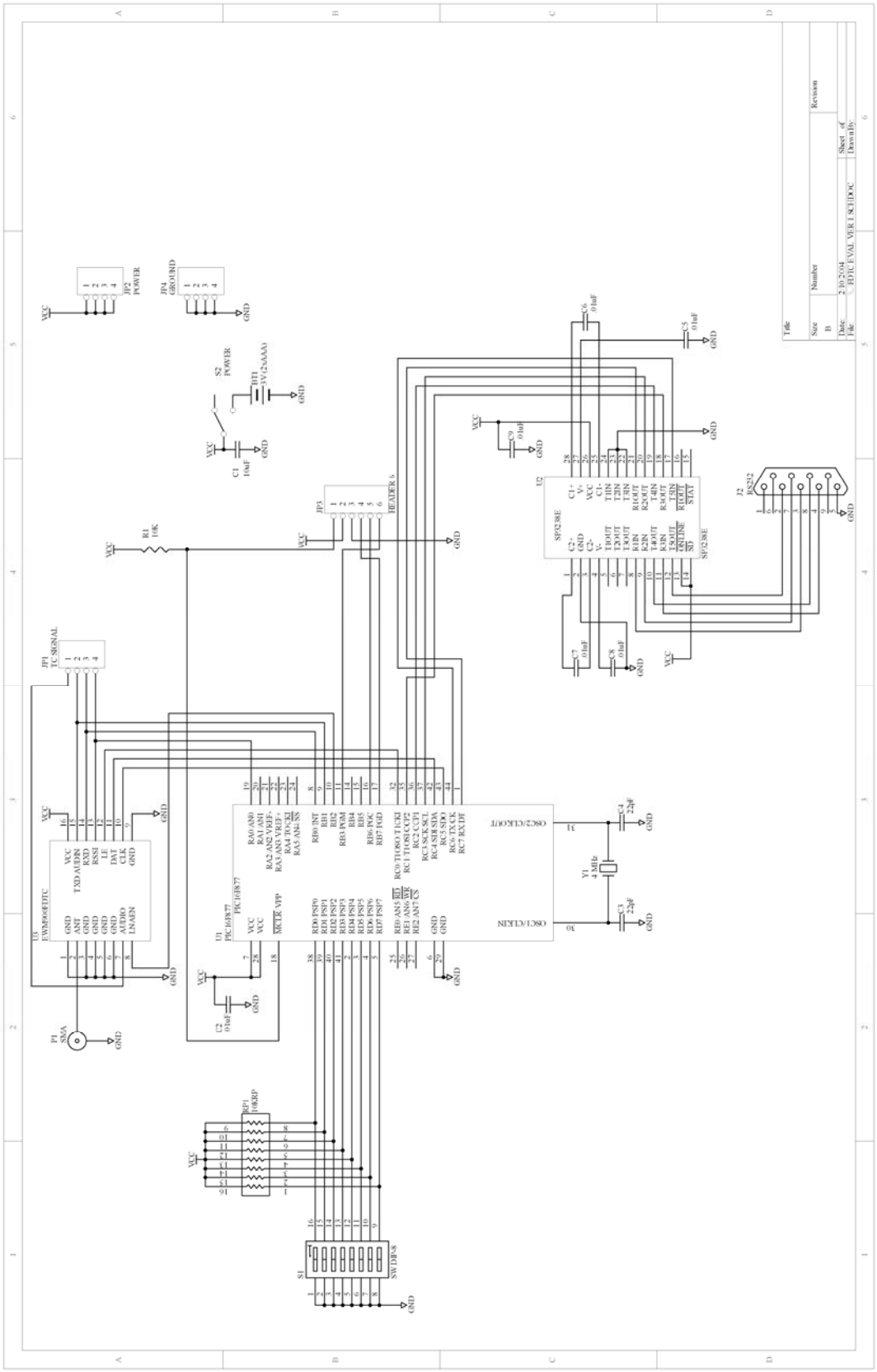

Figure 5, Evaluation Board Schematic Diagram

Applications Information

Figure 5 shows the schematic diagram of our evaluation board. All of the transceiver parameters in the specification sheet were determined on this board.

Power Supply

The transceiver is designed to operate from a 3V DC power supply. Power is provided to the transceiver on pin 16. This power supply should be noise-free. Noise on the power supply will degrade the receiver sensitivity, thereby decreasing range.

Ground

It is important to have a good ground system for any wireless design. The ground plane serves as a base reference for the operation of RF circuitry. All filters are referenced to ground. All oscillators are referenced to ground. If the ground system design is bad, RF circuitry may not function correctly. The results may be reduced performance or spurious emissions.

As a rule of thumb, it is best to use a solid fill ground plane to connect all of the ground pins of the transceiver.

Transmitter Start-Up Time

The start-up time for the transmitter is determined mainly by the loop bandwidth of the PLL loop filter. When the transmitter is enabled by setting the TXE bit in the mode register to a 1, it can take up to 20mSec for the transmitter to be on-channel and ready to transmit information.

Transmitter Channel-Change Time

The channel change time for the transmitter is the time it takes for the transmitter to be locked onto the new channel after programming the TX channel register. For a 1MHz jump, the channel change time is 11mSec. For a 100kHz jump, the channel change time is 7 mSec.

Transmitter Audio/Data Input Requirements

The TXD/AUDIN pin is connected to the transmit VCO. Voltage changes on this pin will frequency modulate the VCO.

The input impedance of this pin will vary from module to module as required to set the proper frequency deviation. Therefore, the pin must be driven by a low impedance source. If the driving circuit is digital, it must have a push-pull output. If the driving circuit is analog, the signal should be buffered by an operational amplifier.

A 3V p-p signal present at this pin will result in a +/-25kHz frequency deviation.

There is a 150Hz high-pass response on this pin due to the TX PLL loop filter. Therefore, the transmitter is not capable of transmitting DC voltage levels. The bandwidth of the signal used to modulate the transmitter should be between 300Hz and 15kHz. For data applications, the baud rate should be between 9600 bps and 19.2kbps.

Receiver Start-Up Time

Like the transmitter, the receiver start-up time is determined by the loop bandwidth of the PLL loop filter. When the receiver is enabled by setting the RXE bit in the mode register to a 1, it can take up to 20mSec for the receiver to be on-channel and ready to receive information.

Receiver Channel-Change Time

The channel change time for the receiver is the time it takes for the receiver to be locked onto the new channel after programming the RX channel register.

For a 1MHz jump, the channel change time is 7mSec. For a 100kHz jump, the channel change time is 5 mSec.

Receiver Audio Output (Audio Mode Only)

The receiver audio output is the analog signal directly from the FM demodulator. It is filtered by a 3rd order LPF with a cut-off frequency of 15kHz.

The audio signal is 600mV typically.

The receiver sensitivity can be increased for audio applications by using an external LPF with a 4kHz cutoff frequency.

Without this filter, the audio sensitivity is -109dBm for a 12dB SINAD. With this filter, the sensitivity should improve by 3-6dB.

Receiver Data Output (Data Mode Only)

The receiver data output is the digital signal from the bit-slicer. It represents the binary data used to modulate the transmitter in data applications. The data output is rail-to-rail and is compatible with CMOS and TTL signal levels.

RSSI

The RSSI pin indicates the received signal strength of the incoming carrier via a DC voltage.

The RSSI dynamic range is 65dB. However, the LNA extends this dynamic.

The RSSI will indicate from -112 to -62dBm. The voltage range is 0.1 to 2.1 V with 0.1V representing -62dBm.

NOTE: The RSSI is not a calibrated value. The actual signal range, dynamic range, and voltage will vary from part to part. The LNA should be turned off by bringing LNAEN low whenever the input signal level is above -70dBm.

Ordering Information

PRODUCT	ORDER CODE
EWM-900-FDTC-BS	100-900-01A
EWM-900-FDTC-HS	100-900-02A

Table 10, Ordering Information