MC74HCT14A

Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high−speed CMOS inputs.

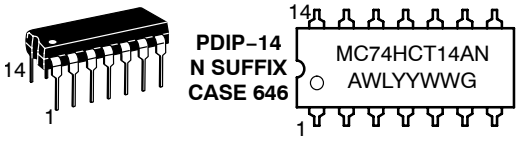
The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

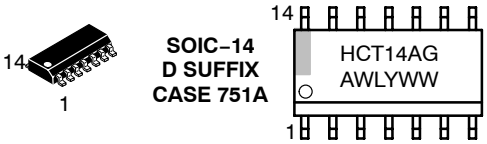
Features

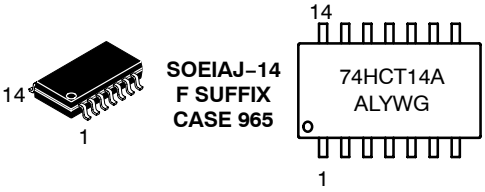
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb−Free Packages are Available

ON Semiconductor®

MARKING DIAGRAMS







A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

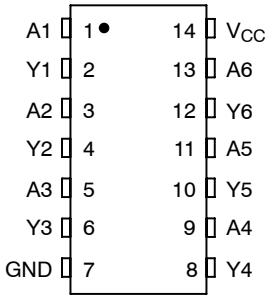
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Publication Order Number:
MC74HCT14A/D

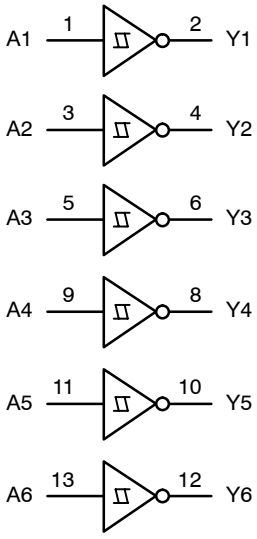
PIN ASSIGNMENT



FUNCTION TABLE

Input A	Output Y
L	H
H	L

LOGIC DIAGRAM



$Y = \overline{A}$ PIN 14 = V_{CC}
PIN 7 = GND

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT14AN	PDIP−14	25 Units / Rail
MC74HCT14ANG	PDIP−14 (Pb−Free)	
MC74HCT14AD	SOIC−14	55 Units / Rail
MC74HCT14ADG	SOIC−14 (Pb−Free)	
MC74HCT14ADR2	SOIC−14	2500 / Tape & Reel
MC74HCT14ADR2G	SOIC−14 (Pb−Free)	
MC74HCT14ADTR2	TSSOP−14*	
MC74HCT14ADTR2G	TSSOP−14*	
MC74HCT14AFEL	SOEIAJ−14	2000 / Tape & Reel
MC74HCT14AFELG	SOEIAJ−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	−0.5 to +7.0	V
V_I	DC Input Voltage	(Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_O	DC Output Voltage	(Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±25	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
I_{GND}	DC Ground Current per Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	78 125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>4000 >300 >1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 4)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.
5. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	4.5	5.5	V
V_I, V_O	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)		−	(Note 6)	ns

6. No Limit when $V_I \approx 50\%$ V_{CC}, $I_{CC} > 1$ mA.
7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit −55°C to 25°C Min	−55°C to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
V_{T+} max	Maximum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V_{T+} min	Minimum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
V_{T-} max	Maximum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
V_{T-} min	Minimum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V_H max	Maximum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V_H min	Minimum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0 4		
V_{OH}	Minimum High−Level Output Voltage	$V_I < V_{T-}$ min $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		$V_I < V_{T-}$ min $\|I_{out}\| \le 4.0$ mA	4.5	3.98		3.84		3.7		
V_{OL}	Maximum Low−Level Output Voltage	$V_I \ge V_{T+}$ max $\|I_{out}\| \le 20\ \mu A$	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_I \ge V_{T+}$ max $\|I_{out}\| \le 4.0$ mA	4.5		0.26		0.33		0.4	
I_{IK}	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	$V_I = V_{CC}$ or GND I_{out} = 0 μA	5.5		1.0		10		40	μA
				≥ −55°C		25°C to 125°C				
ΔI_{CC}	Additional Quiescent Supply Current	V_I = 2.4 V, Any One Input $V_I = V_{CC}$ or GND, Other Inputs I_{out} = 0 μA	5.5	2.9		2.4				mA

8. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF; Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Test Conditions	Figures	Guaranteed Limit −55°C to 25°C Min	−55°C to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V_{CC} = 5.0 V ±10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	1 & 2		32		40		48	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	V_{CC} = 5.0 V ± 10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	1 & 2		15		19		22	ns

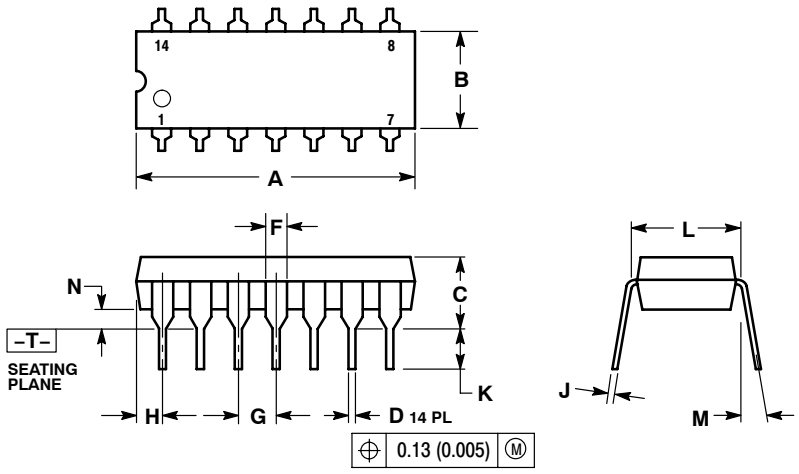
9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance, per Inverter (Note 10)	32	pF

10. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01