National Semiconductor

LP38500/2-ADJ, LP38500A/2A-ADJ 1.5A FlexCap Low Dropout Linear Regulator for 2.7V to 5.5V Inputs

General Description

National's FlexCap LDO's feature unique compensation that allows the use of any type of output capacitor with no limits on minimum or maximum ESR. The LP38500/2 series of low-dropout linear regulators operates from a +2.7V to +5.5V input supply. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. Developed on a CMOS process, (utilizing a PMOS pass transistor), the LP38500/2 has low quiescent current that changes little with load current.

Ground Pin Current: Typically 2 mA at 1.5A load current.

Disable Mode: Typically 25 nA quiescent current when the Enable pin is pulled low.

Simplified Compensation: Stable with any type of output capacitor, regardless of ESR.

Precision Output: "A" grade versions available with 1.5% V_{ADJ} tolerance (25°C) and 3% over line, load and temperature.

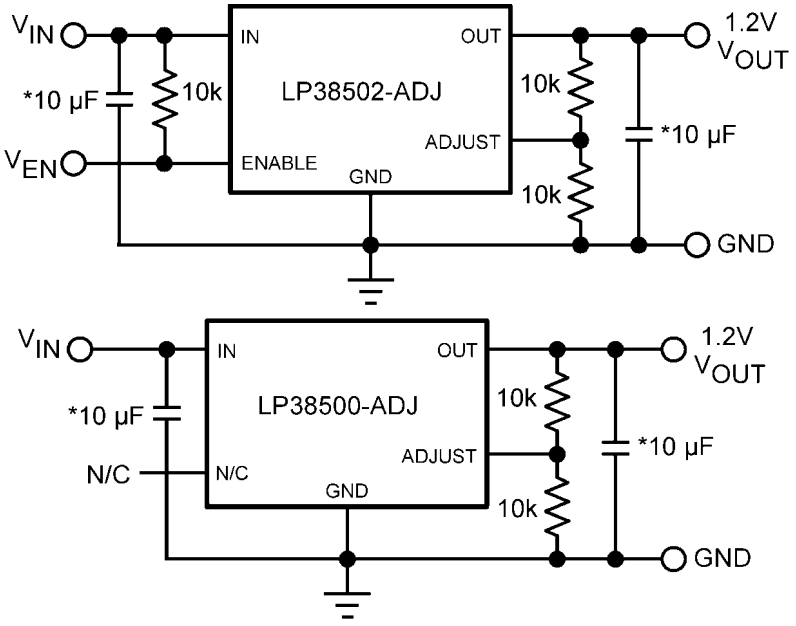
Features

- FlexCap: Stable with ceramic, tantalum, or aluminum capacitors
- Stable with 10 µF input/output capacitor
- Adjustable output voltage from 0.6V to 5V
- Low ground pin current
- 25 nA quiescent current in shutdown mode
- Guaranteed output current of 1.5A
- Available in TO-263, TO-263 THIN, and LLP-8 packages
- Guaranteed V_{ADJ} accuracy of ±1.5% @ 25°C (A Grade)
- Guaranteed accuracy of ±3.5% @ 25°C (STD)
- Over-Temperature and Over-Current protection
- −40°C to +125°C operating T_J range
- Enable pin (LP38502)

Applications

- ASIC Power Supplies In:
  Printers, Graphics Cards, DVD Players
  Set Top Boxes, Copiers, Routers
- DSP and FPGA Power Supplies
- SMPS Regulator
- Conversion from 3.3V or 5V Rail

Typical Application Circuit



*Minimum capacitance required (see Application Information)

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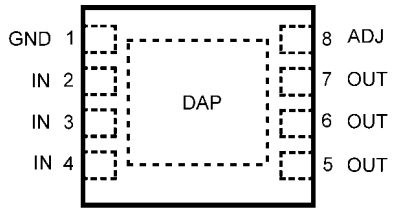
Connection Diagrams for LLP-8 (SD) Package



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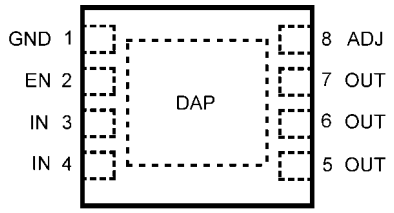
Top View (LP38500SD-ADJ, LP38500ASD-ADJ)
LLP-8 Package



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Top View (LP38502SD-ADJ, LP38502ASD-ADJ)
LLP-8 Package

Pin Descriptions for LLP-8 (SD) Package

Pin #	Designation	Function
1	GND	Ground
2	IN	Input Supply (LP38500 only). Input Supply pins share current and must be connected together on the PC Board.
	EN	Enable (LP38502 only). Pull high to enable the output, low to disable the output. This pin has no internal bias and must be either tied to the input voltage, or actively driven.
3, 4	IN	Input Supply. Input Supply pins share current and must be connected together on the PC Board.
5, 6, 7	OUT	Regulated Output Voltage. Output pins share current and must be connected together on the PC Board.
8	ADJ	Sets output voltage
DAP	DAP	The DAP is used to remove heat from the device by conducting it to a copper clad area on the PCB which acts as a heatsink. The DAP is electrically connected to the backside of the die. The DAP must be connected to ground potential, but can not be used as the only ground connection.

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Package Type	Package Marking	Supplied As:
ADJ	LP38500SDX-ADJ	LLP-8	LP38500SD-ADJ	Tape and Reel of 4500 Units
	LP38500SD-ADJ		LP38500SD-ADJ	Tape and Reel of 1000 Units
	LP38502SDX-ADJ		LP38502SD-ADJ	Tape and Reel of 4500 Units
	LP38502SD-ADJ		LP38502SD-ADJ	Tape and Reel of 1000 Units
	LP38500ASDX-ADJ		LP38500ASD-ADJ	Tape and Reel of 4500 Units
	LP38500ASD-ADJ		LP38500ASD-ADJ	Tape and Reel of 1000 Units
	LP38502ASDX-ADJ		LP38502ASD-ADJ	Tape and Reel of 4500 Units
	LP38502ASD-ADJ		LP38502ASD-ADJ	Tape and Reel of 1000 Units
ADJ	LP38500TSX-ADJ	TO-263	LP38500TS-ADJ	Tape and Reel of 500 Units
	LP38500TS-ADJ		LP38500TS-ADJ	Rail of 45 Units
	LP38502TSX-ADJ		LP38502TS-ADJ	Tape and Reel of 500 Units
	LP38502TS-ADJ		LP38502TS-ADJ	Rail of 45 Units
ADJ	LP38500TJ-ADJ	TO-263 THIN	LP38500TJ-ADJ	Tape and Reel of 1000 Units
	LP38502TJ-ADJ		LP38502TJ-ADJ	Tape and Reel of 1000 Units
	LP38500ATJ-ADJ		LP38500ATJ-ADJ	Tape and Reel of 1000 Units
	LP38502ATJ-ADJ		LP38502ATJ-ADJ	Tape and Reel of 1000 Units

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating (Note 2)	±2 kV
Power Dissipation(Note 3)	Internally Limited
Input Pin Voltage (Survival)	−0.3V to +6.0V
Enable Pin Voltage (Survival)	−0.3V to +6.0V
Output Pin Voltage (Survival)	−0.3V to +6.0V
I_{OUT} (Survival)	Internally Limited

Operating Ratings (Note 1)

Input Supply Voltage	2.7V to 5.5V
Enable Input Voltage	0.0V to 5.5V
Output Current (DC)	0 to 1.5A
Junction Temperature(Note 3)	−40°C to +125°C
V_{OUT}	0.6V to 5V

Electrical Characteristics LP38500/2–ADJ

Unless otherwise specified: V_{IN} = 3.3V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	Adjust Pin Voltage (Note 6)	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	0.584 **0.575**	0.605	0.626 **0.635**	V
V_{ADJ}	Adjust Pin Voltage (Note 6) "A" GRADE	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	0.596 **0.587**	0.605	0.614 **0.623**	V
I_{ADJ}	Adjust Pin Bias Current	2.7V ≤ V_{IN} ≤ 5.5V		50	**750**	nA
V_{DO}	Dropout Voltage (Note 7)	I_{OUT} = 1.5A		220	275 **375**	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation (Notes 4, 6)	2.7V ≤ V_{IN} ≤ 5.5V	—	0.04 **0.05**	—	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (Notes 5, 6)	10 mA ≤ I_{OUT} ≤ 1.5A	—	0.18 **0.33**	—	%/A
I_{GND}	Ground Pin Current In Normal Operation Mode	10 mA ≤ I_{OUT} ≤ 1.5A	—	2	3.5 **4.5**	mA
$I_{DISABLED}$	Ground Pin Current	V_{EN} < $V_{IL(EN)}$	—	0.025	0.125 **15**	µA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{OUT(NOM)}$ - 5%		3.6		A
I_{SC}	Short Circuit Current	V_{OUT} = 0V	**2**	3.7		A
Enable Input (LP38502 Only)						
$V_{IH(EN)}$	Enable Logic High	V_{OUT} = ON	**1.4**	—	—	V
$V_{IL(EN)}$	Enable Logic Low	V_{OUT} = OFF	—	—	**0.65**	
$t_{d(off)}$	Turn-off delay	Time from V_{EN} < $V_{IL(EN)}$ to V_{OUT} = OFF I_{LOAD} = 1.5A	—	25	—	µs
$t_{d(on)}$	Turn-on delay	Time from V_{EN} >$V_{IH(EN)}$ to V_{OUT} = ON I_{LOAD} = 1.5A	—	25	—	
$I_{IH(EN)}$	Enable Pin High Current	V_{EN} = V_{IN}	—	1	—	nA
$I_{IL(EN)}$	Enable Pin Low Current	V_{EN} = 0V	—	0.1	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 3.0V, I_{OUT} = 1.5A f = 120Hz	—	58	—	dB
		V_{IN} = 3.0V, I_{OUT} = 1.5A f = 1 kHz	—	56	—	
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz, C_{OUT} = 10 µF CER	—	1.0	—	µV/$\sqrt{Hz}$
e_n	Output Noise Voltage	BW = 100Hz – 100kHz C_{OUT} = 10 µF CER	—	100	—	µV (rms)
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	—	170	—	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	—	10	—	
θ_{J-A}	Thermal Resistance Junction to Ambient	TO-263, TO-263 THIN(Note 8) 1 sq. in. copper	—	37	—	°C/W
	Thermal Resistance Junction to Ambient	LLP-8 (Note 9)	—	80	—	
θ_{J-C}	Thermal Resistance Junction to Case	TO-263, TO-263 THIN	—	5	—	°C/W
		LLP-8	—	16	—	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 3: Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}). See Application Information.

Note 4: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the voltage at the input.

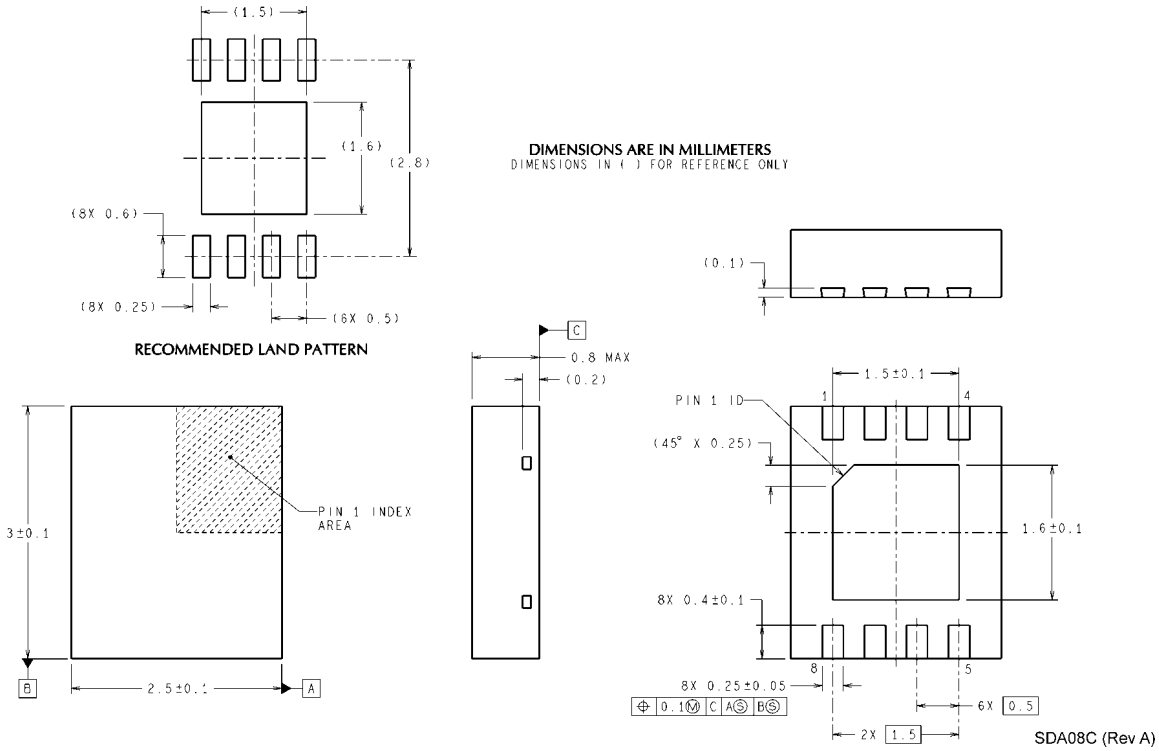
Note 5: Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current.

Note 6: The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.

Note 7: Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.

Note 8: The value of θ_{JA} for the TO-263 (TS) package and TO-263 THIN (TJ) package can range from approximately 30 to 60°C/W depending on the amount of PCB copper dedicated to heat transfer (See Application Information).

Note 9: θ_{JA} for the LLP-8 package was measured using the LP38502SD-ADJ evaluation board (See Application Information).



8-Lead LLP Package
NS Package Number SDA08C