Dual/Quad Low Power, High Speed JFET Operational Amplifiers

OP282/OP482

FEATURES

High slew rate: 9 V/µs
Wide bandwidth: 4 MHz
Low supply current: 250 µA/amplifier maximum
Low offset voltage: 3 mV maximum
Low bias current: 100 pA maximum
Fast settling time
Common-mode range includes V+
Unity-gain stable

APPLICATIONS

Active filters
Fast amplifiers
Integrators
Supply current monitoring

GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/µs with a supply current under 250 µA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

With a wide output swing, within 1.5 V of each supply, low power consumption, and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. The OP282 is available in the standard 8-lead narrow SOIC and MSOP packages. The OP482 is available in PDIP and narrow SOIC packages.

PIN CONNECTIONS

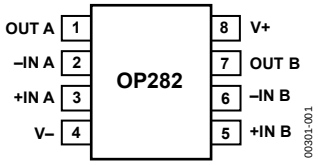


Figure 1. 8-Lead Narrow-Body SOIC (S-Suffix) [R-8]

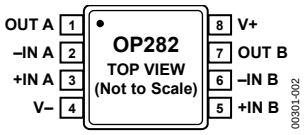


Figure 2. 8-Lead MSOP [RM-8]

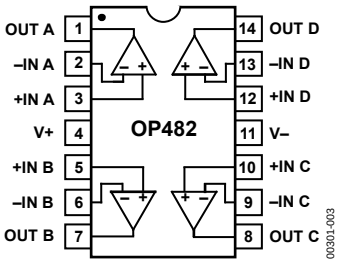


Figure 3. 14-Lead PDIP (P-Suffix) [N-14]

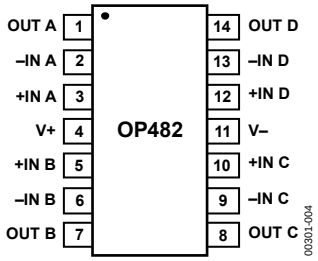


Figure 4. 14-Lead Narrow-Body SOIC (S-Suffix) [R-14]

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At V_S = ±15.0 V, T_A = 25°C, unless otherwise noted; applies to both A and G grades.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282		0.2	3	mV
		OP282, −40°C ≤ T_A ≤ +85°C			4.5	mV
		OP482		0.2	4	mV
		OP482, −40°C ≤ T_A ≤ +85°C			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V[1]			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V[1]			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection Ratio	CMRR	−11 V ≤ V_{CM} ≤ +15 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +85°C	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	13.5	13.9		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ		−13.9	−13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		−12	−8	mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ 85°C		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Ø_M$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

[1] The input bias and offset currents are characterized at T_A = T_J = 85°C. Bias and offset currents are guaranteed but not tested at −40°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Ratings
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Operating Temperature Range	
OP282G, OP282A, OP482G	−40°C to +85°C
Junction Temperature Range	
P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

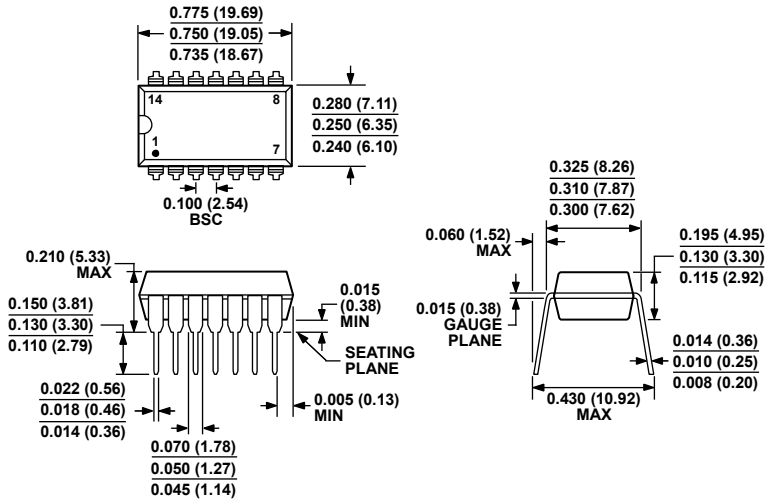
θ_{JA} is specified for the worst-case conditions, that is, a device in socket for CERDIP and PDIP. θ_{JA} is specified for device soldered in circuit board for SOIC_N or MSOP packages.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP [RM]	206	44	°C/W
8-Lead SOIC_N (S-Suffix) [R]	157	56	°C/W
14-Lead PDIP (P-Suffix) [N]	83	39	°C/W
14-Lead SOIC_N (S-Suffix) [R]	104	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

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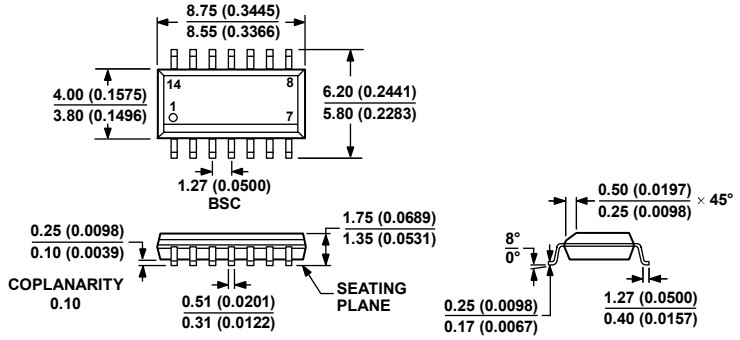
Figure 50. 14-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix (N-14)
Dimension shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 51. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
S-Suffix (R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
OP282ARMZ-R2[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP482GP	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GPZ[1]	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GS	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL7	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ[1]	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL[1]	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL7[1]	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	

[1] Z = RoHS Compliant Part.