UM0469
User manual

Using the VS6724-based camera module with the STR9 dongle

1 Introduction

This user manual describes how the VS6724-based 2 mega pixel CMOS camera module board is used with the STR9 dongle. The camera is controlled via an I^2C bus, and data is transferred by GPIO and accelerated using DMA and interrupts.

Figure 1. Camera module based on the VS6724

Figure 2. Camera module connected to the STR9 dongle, ARM9 platform

Figure 3. Surface mounting the camera socket to prevent lens damage

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2.1 Board description and interconnection

2.1.1 STR9 dongle

The camera module can be used with a fast GPIO of any microcontroller and I^2C interface. For fast and simple evaluation the STR9 dongle evaluation platform with the ARM9 microcontroller is recommended. Interconnection of the camera module to the dongle is simple and is shown in *Figure 2*. Please refer to user manual UM0282 for additional information about the STR9 dongle platform.

2.1.2 Application

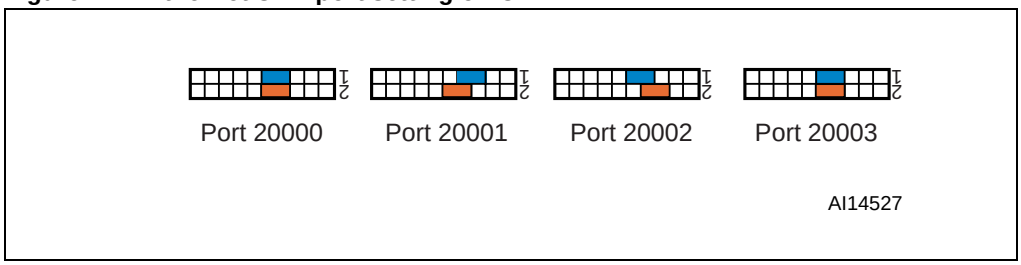
After connecting the camera module to a microcontroller, the initialization sequence of the commands must be sent to the camera module via I^2C. The last command should be the start of the streaming process. The commands and I^2C signals are described in user manual UM0217 and the VS6724 datasheet.

Table 1. STR9 and the VS6724-based camera board interconnection

STR9	VS6724	Module pin-out	Note
P97	D7	CN3 - 13	
P96	D6	CN3 - 11	
P95	D5	CN3 - 7	
P94	D4	CN3 - 5	
P93	D3	CN3 - 4	
P92	D2	CN3 - 3	
P91	D1	CN3 - 2	
P90	D0	CN3 - 1	
P35	SDA	CN3 - 14	I^2C data
P34	SCL	CN3 - 12	I^2C clock
3.3 V	3.3 V	CN3 - 17, 19	Power module supply
GND	GND	CN3 - 18, 20	
P36	CE	CN3 - 15	Camera chip enable
P30	PCLK	CN4 - 6	Pixel qualification clock
P33	H_{SYNC}	CN4 - 10	Vertical sync. frame start
P32	V_{SYNC}	CN4 - 9	Horizontal sync. line start
P31	FLASH	CN4 - 8	Camera flash request
P37	MAINCLK	CN4 - 16	Clock for camera

The power supply for the camera is derived from 3.3 V supplied by the STR9 platform. A double Shottky diode (D1) is used to reduce 3.3 V to 2.8 V. If R4 is not assembled, only one of the two diodes is used and the output voltage is 2.76 V. If R4 is assembled, both of the diodes are used in parallel and the output voltage is 2.84 V.

Figure 4. Ethernet UDP port setting on CN4



When an application using more than one camera is used, the evaluation kits must have different addresses in order to distinguish between the packets from each. Connector CN4 allows this function to be achieved (see *Figure 4*). If no jumper is used, the port address 20000 is assigned as the default value.

2.2 Software description

2.2.1 SW block diagram

Figure 5. Reading of data from the camera using polling

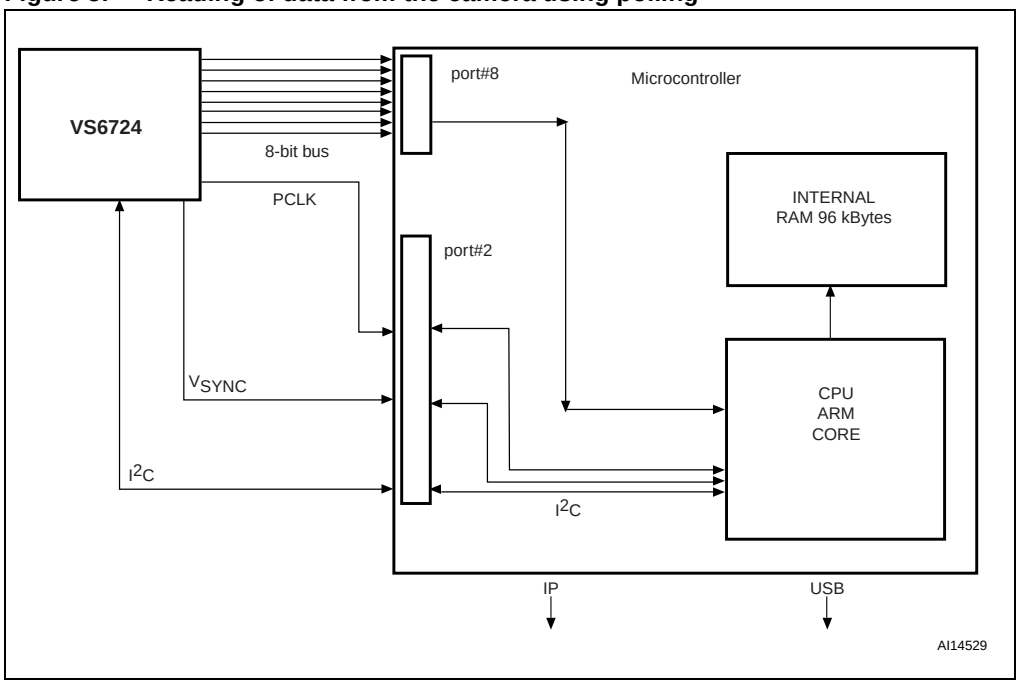
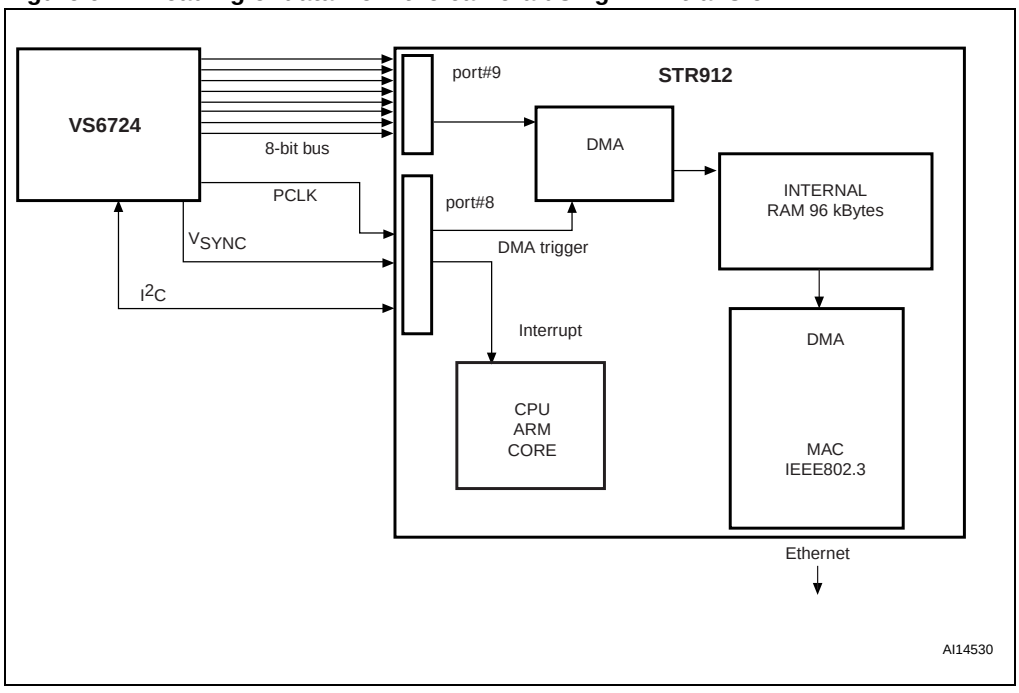


Figure 6. Reading of data from the camera using DMA transfer



2.2.2 C code - image download using polling

Configuration part:

```
while(cameraWarmUp(12) == ERROR);

cameraFormat(ImageFormatYCC400);

cameraResolution(ImageSizeQCIF);

cameraRun();
```

This code reads the data from the port 9 if there is a rising edge on the port 3.

```
__ramfunc void getImageFromCamera(char buffer[]){
 //VSYNC log.1 - frame valid
 //wait for the valid frame
   do{
     SIGNALS = GPIO3->DR[0x3FC];
   }while((SIGNALS & VSYNC));  //wait for the falling edge of VSYNC

   do{
     SIGNALS = GPIO3->DR[0x3FC];
   }while(!(SIGNALS & VSYNC));  //wait for the rising edge of VSYNC

  PCLKedge = 0;
  pixel = 0;
  while(1){
    while(1){
      SIGNALS = GPIO3->DR[0x3FC];
      if(SIGNALS & PCLK)
        if(!PCLKedge)
          break;
      if(!(SIGNALS & PCLK))
        PCLKedge = 0;
    }//wait for the rising edge of PCLK
    PCLKedge = 1;

    buffer[pixel] = GPIO9->DR[0x3FC];
    pixel++;

    if(pixel > QCIF)
      break;
  }
}
```

2.2.3 C code - image download using DMA

Configuration part:

```
while(cameraWarmUp(12) == ERROR);
cameraFormat(ImageFormatJPEG);
JPEGconfig(ETH_FRAME_PAYLOAD/2);
cameraResolution(ImageSizeCIF, cameraID);
cameraRun();
manualFPS(cameraID);
cameraFPS(14, cameraID);
```

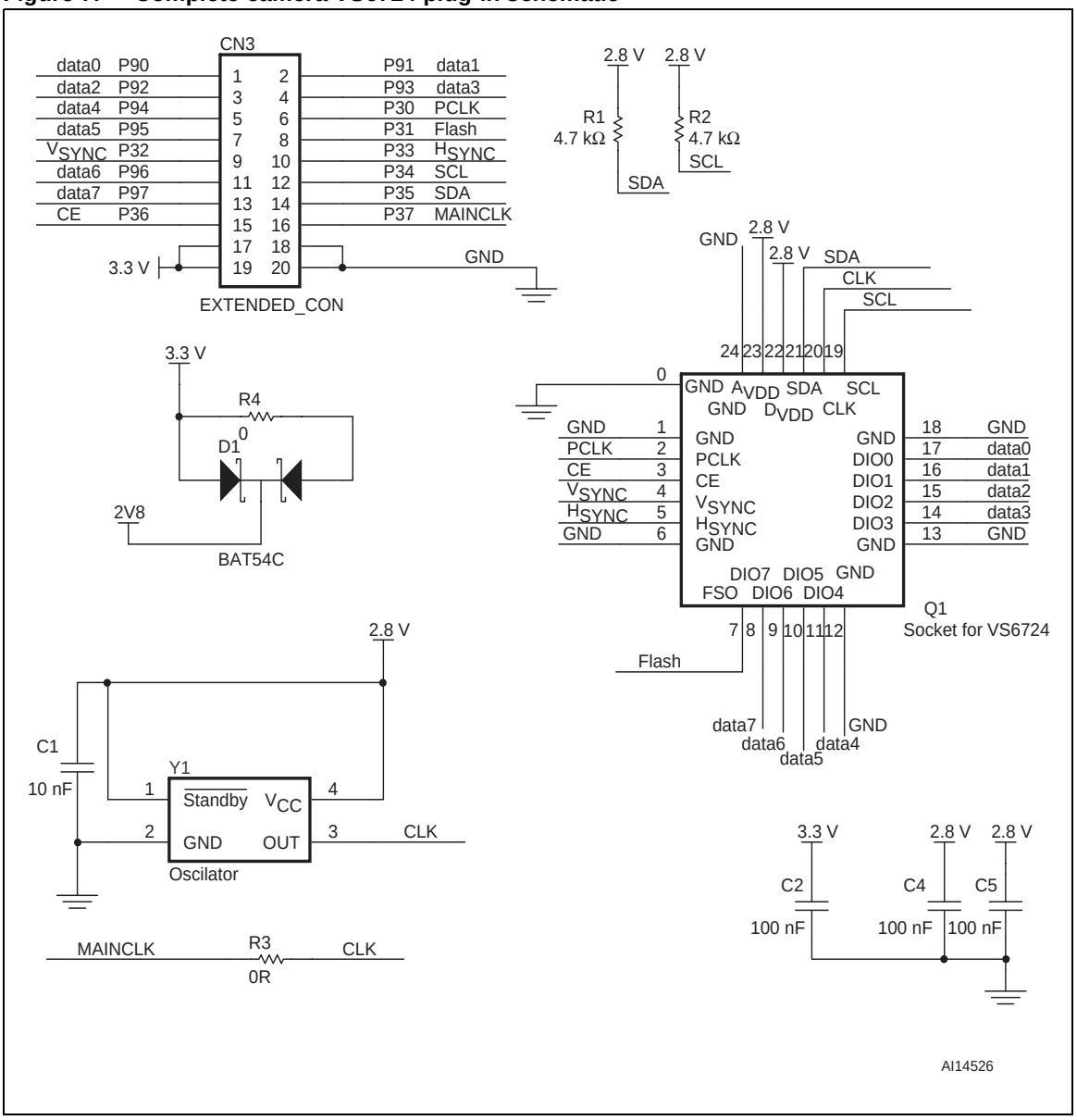
This code reads the data from the port 9 if there is a rising edge on the port 3.

```
void InitDMAforIPCAM(void){
  DMA_DeInit();
  /*Enable the DMA*/
  DMA_Cmd(ENABLE);
  DMA_ChannelCmd (DMA_Channel0, DISABLE);
  DMA_StructInit(&DMA_InitStruct);
  /********************* DMA configuration ********************/
  DMA_InitStruct.DMA_Channel_LLstItm = (u32)&link[1];

  /* Source address */
  DMA_InitStruct.DMA_Channel_SrcWidth= DMA_SrcWidth_Byte;
  DMA_InitStruct.DMA_Channel_SrcAdd = (u32)&GPIO9->DR[0x3FC];
  DMA_InitStruct.DMA_Channel_DesAdd = (u32) (eth_frame[0] +
ETH_HDR_LENGTH + IP_HDR_LENGTH + UDP_HDR_LENGTH + RTP_HDR_LENGTH);
  /* The Destination bus width is a word word*/
  DMA_InitStruct.DMA_Channel_DesWidth= DMA_DesWidth_Byte;
  /*This field must be set to transfer all data*/
  DMA_InitStruct.DMA_Channel_DesBstSize = DMA_DesBst_1Data ;
  DMA_InitStruct.DMA_Channel_SrcBstSize = DMA_SrcBst_1Data;

  /* DMA is The flow controller*/

  DMA_InitStruct.DMA_Channel_FlowCntrl = DMA_FlowCntrl2_DMA;
  DMA_InitStruct.DMA_Channel_Src = DMA_SRC_External_Req0;

  DMA_InitStruct.DMA_Channel_TrsfSize = ETH_FRAME_PAYLOAD;

  DMA_ChannelSRCIncConfig (DMA_Channel0, DISABLE);
  DMA_ChannelDESIncConfig (DMA_Channel0, ENABLE);
  /*Enable the terminal count interrupt for the first LLI*/
  DMA_ITConfig(DMA_Channel0, ENABLE);
  /*Enable the terminal count interrupt for the channel1*/
  DMA_ITMaskConfig(DMA_Channel0, DMA_ITMask_ITC, ENABLE);
  /*DMA init by its struct*/
  DMA_Init(DMA_Channel0,&DMA_InitStruct);
```

```
  DMA_ClearIT( Channel0,DMA_TCC);
  eth_buf_num = 0;
}

ConfigDMA();
InitDMAforIPCAM();
edgePCLKconfig(cameraID);
JPEGclockslowdown(slower8times);

while(1) {
  while (ext_cmd != 'S');  //wait for start packet
  ext_cmd = 0;
  cam_enet_init();         //initialize the Ethernet

  InitDMAforIPCAM();

  WIU->PR = WIU_Line2;     //Clear IT Pending Bit
  WIU->TR &= ~WIU_Line2;   //trigger on falling edge
  // enable interrupts
  VIC_ITCmd(DMA_ITLine, ENABLE);
  VIC_ITCmd(EXTIT0_ITLine, ENABLE);

  NewPictureRequest = DISABLE;
  DMA_ChannelCmd (DMA_Channel0, ENABLE);    //start DMA

  while (ext_cmd != 'T');  //wait for stop packet
  DMA_ChannelCmd (DMA_Channel0, DISABLE);   //stop DMA
  VIC_ITCmd(DMA_ITLine, DISABLE);   // disable interrupts
  VIC_ITCmd(EXTIT0_ITLine, DISABLE);
  ext_cmd = 0;
}
```

2.3 Schematic - VS6724

Figure 7. Complete camera VS6724 plug-in schematic



3 PCB bill of material for STR9 and VS6724 modules

Table 2. Bill of material

Reference	Value	Package	Quantity		Note
R4	0 Ω	0603	1	Resistor	
R3	0 Ω	0805	1	Resistor	
C2,C4,C5	100 nF	0805	3	Capacitor	
C1	10 nF	0805	1	Capacitor	
R1, R2	4.7 kΩ	0805	2	Resistor	
D1	BAT54C	SOT23	1	Schottky barrier double diode	ST Microelectronics
CN3	EXTENDED_CON	HDR2X10vertical	1	Header, 10-pin, dual row	GES06600345, 2 x 10 pins 2.54, 90°, PBD-20R, female
Y1	Oscillator	SG-310	1	SG-310	Not assembled
Q1	Socket for VS6724 + camera		1	VS6724Q0FB	ST Microelectronics

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
20-Nov-2007	1	Initial release.

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