AT91SAM9G45-EKES

User Guide

6481B–ATARM–27-Nov-09

Section 1

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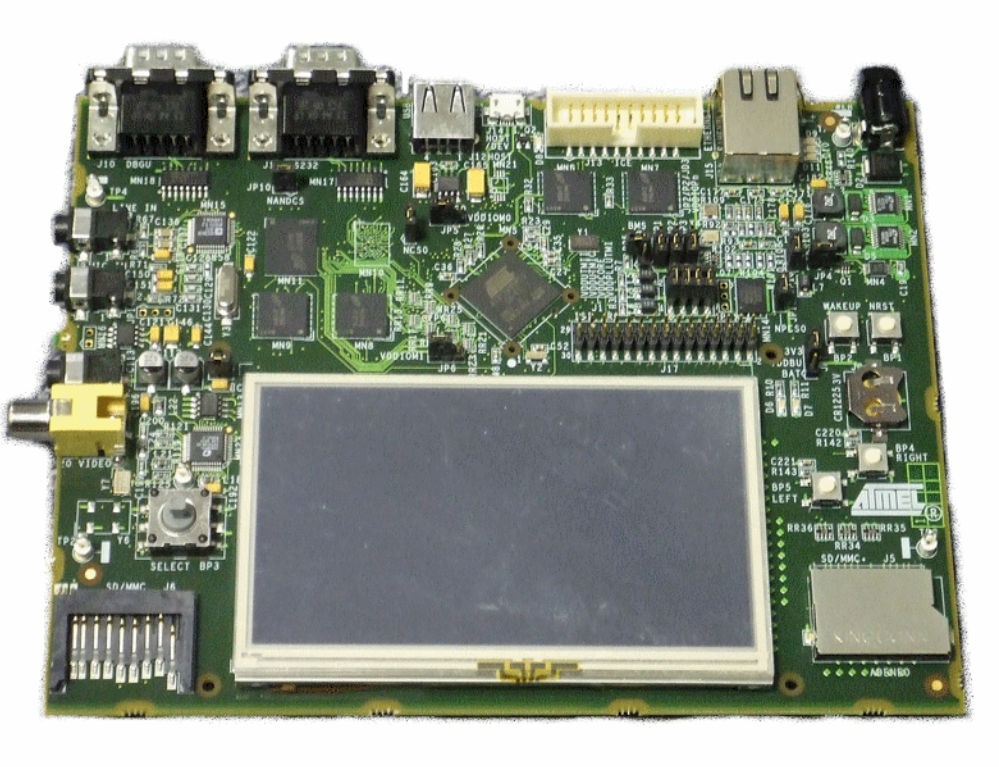
Section 1

Introduction

1.1 Scope

This User Guide introduces the SAM9G45 Evaluation Kit (SAM9G45-EKES) and describes its development and debugging capabilities.

Figure 1-1. Board Photo



The Atmel® SAM9G45-EKES is a fully-featured evaluation platform for the Atmel SAM9G45-based microcontroller. The evaluation kit allows users to extensively evaluate, prototype and create application-specific designs.

The SAM9G45-EKES includes many hardware peripherals such as:

- Two high speed USB hosts and one high speed device port
- An Ethernet 10/100 interface
- Two high speed multimedia card interfaces
- An LCD TFT display (480*RGB*272)
- A composite video output

- A camera interface
- Several communication peripherals such as:
  - Universal Synchronous/Asynchronous Receiver Transmitter (USART)
  - Serial Synchronous Controller (SSC)
  - Two-Wire Interface (TWI)

The external memory block is made of 3 memory types:

- DDR2-SDRAM
- NAND Flash
- NOR Flash

1.2 Applicable Documents

Table 1-1. Applicable Documents

Reference	Title	Comments
6438A	SAM9G45 Preliminary Datasheet	This document describes the SAM9G45, which is part of the Atmel's Smart ARM® Microcontrollers. It is available from http://www.atmel.com/dyn/products/product_card.asp?part_id=4596
6485A	Errata on AT91SAM9G45 Engineering Sample Devices	It is available from http://www.atmel.com/dyn/products/product_card.asp?part_id=4596

Section 2

Kit Contents

2.1 Deliverables

The Atmel SAM9G45-EKES toolkit includes:

- Board
  - The SAM9G45-EKES board
- Power supply
  - Universal input AC/DC power supply with US, Europe and UK plug adapters
  - One 3V Lithium Battery type CR1225
- Cables
  - One micro A/B-type USB cable
  - One serial RS232 cable
- A Welcome Letter

Figure 2-1. Unpacked SAM9G45-EKES

Unpack and inspect this kit carefully. Contact your local Atmel distributor, should you have issues concerning the contents of the kit.

2.2 Evaluation Board Specifications

Table 2-1. SAM9G45-EKES Specifications

Characteristics	Specifications
Clock speed	400 MHz PCK, 133 MHz MCK
Ports	Ethernet, USB, RS232, DBGU
Board supply voltage	5 VDC from connector
Temperature - operating - storage	 -10° to +50° C -40° to +85° C
Relative humidity	0 to 90% (non condensing)
Dimensions	180 mm x 160 mm
RoHS status	Compliant

2.3 Electrostatic Warning

The SAM9G45-EKES evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example...). Avoid touching the component pins or any other metallic element on the board.

Section 3

Power up

3.1 Power Up the Board

Unpack the board taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country, and insert it in the power supply.

Connect the power supply DC connector to the board and plug the power supply to an AC power plug.

The board LCD should light up and display a welcome page. Then, click or touch icons displayed on the screen and enjoy the demo.

3.2 Battery

The SAM9G45-EKES ships with a 3V coin battery.

This battery is not required for the board to start up.

The coin battery is provided for user convenience in case the user would like to exercise the date and time backup function of the SAM9G45 series devices when the board is switched off.

3.3 DevStart

The on-board NAND Flash contains a “SAM9G45-EKES DevStart”.

It is stored in the “SAM9G45-EKES DevStart” folder on the USB Flash disk available when the SAM9G45-EKES is connected to a host computer.

Click the file “welcome.html” in this folder to launch SAM9G45-EKES DevStart.

SAM9G45-EKES DevStart guides you through installation processes of IAR™ EWARM, Keil MDK and GNU toolkits. Then, it gives you step-by-step instructions on how to rebuild a single example project and how to program it into the SAM9G45-EKES. Optionally, if you have a SAM-ICE™, instructions are also given about how to debug the code.

We recommend that you backup the “SAM9G45-EKES DevStart” folder on your computer before launching it.

3.4 Recovery Procedure

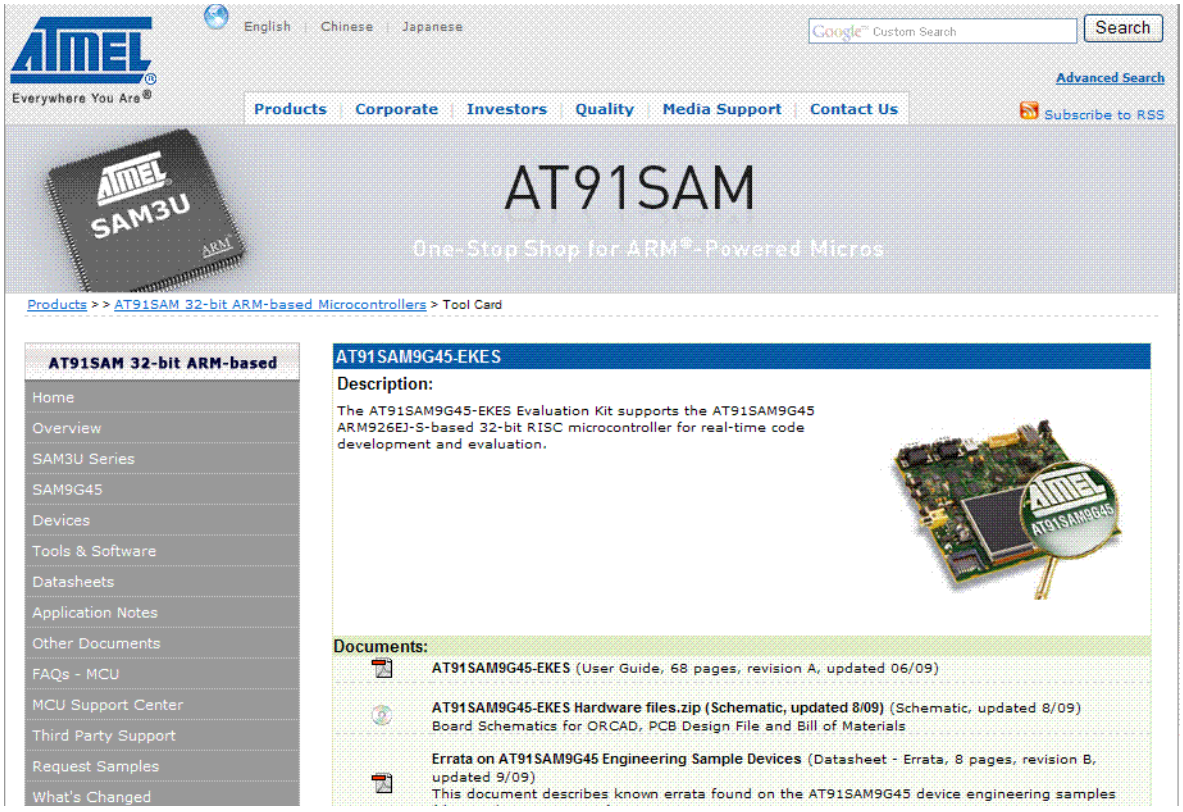
The DevStart ends by giving step-by-step instructions on how to recover the SAM9G45-EKES to the state as it was when shipped by Atmel.

Follow the instructions if you deleted the contents of the embedded Flash or the NAND Flash and want to recover from this situation.

3.5 Sample Code and Technical Support

After boot up, you can run some sample code or your own application on the development kit. You can download sample code and get technical support from Atmel website http://www.atmel.com/dyn/products/tools_card.asp?tool_id=4597

Figure 3-1. Atmel Website for SAM9G45 Series

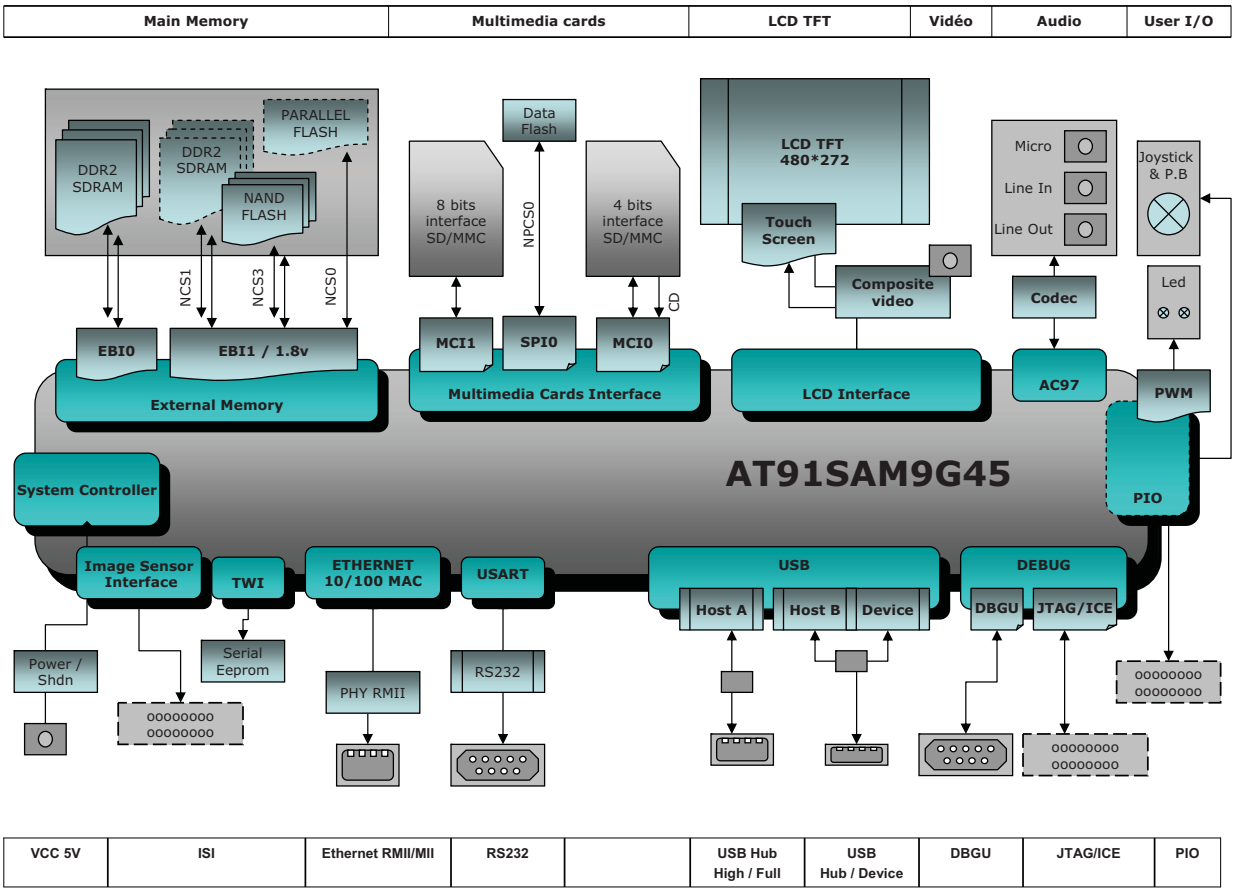


Section 4

Board Description

4.1 Equipment on the Board

Figure 4-1. Board Architecture



4.1.1 Interfaces

The board is equipped with a SAM9G45-CU chip (324-ball TFBGA package) together with the following interfaces or peripherals:

- DDR2/LPDDR memory interface is connected to 128 MB DDR2-SDRAM memory
- External Bus Interface (EBI) is connected to three kinds of memory devices (DDR2-SDRAM, NAND Flash and NOR Flash (not populated))

- One TWI serial memory
- One USB Host/Device multiplexed port interface
- One USB Host port interface
- One RS232 serial communication port
- One DBGU serial communication port
- One JTAG/ICE debug interface
- One Ethernet 100-base TX with three status LEDs
- One AC97 Audio DAC with headphone line out, line in and mono/stereo micro inputs
- One TV interface (composite video output)
- One 4.3" TFT LCD Module with touch screen and back light
- One ISI connector (camera interface)
- One Power red LED and two general-purpose green LEDs
- Two user input push buttons
- One joystick with 4-direction control and selector
- One Wakeup input push button
- One reset input push button
- One DataFlash®/SD/SDIO/MMC plus card slot (4/8 bit interface)
- One SD/SDIO/MMC card slot (4-bit interface)
- One Lithium Coin Cell Battery Retainer for 12 mm cell size (memory backup usage)

4.1.2 Board Interface Connection

- Ethernet using RJ45 connector (J15)
- USB Host, support USB host using a type A connector (J12)
- USB Host/Device, support USB host/device using a type micro AB connector (J14)
- UART1 (Rx, Tx, Rts, Cts) connected to a 9-way male D-type RS232 connector (J11)
- DBGU (Rx and Tx only) connected to a 9-way male D-type RS232 connector (J10)
- JTAG, 20 pin IDC connector (J13)
- SD/MMCplus connector (J5)
- SD/MMC connector (J6)
- Headphone (J7), line-in (J8) and microphone headset (J9)
- Speaker output (JP15)
- Image sensor connector (J17)
- TFT LCD display (J16), with TouchScreen (J19) and BackLigth (J21)
- Test points; various test points are located throughout the board
- Main power supply (J2)

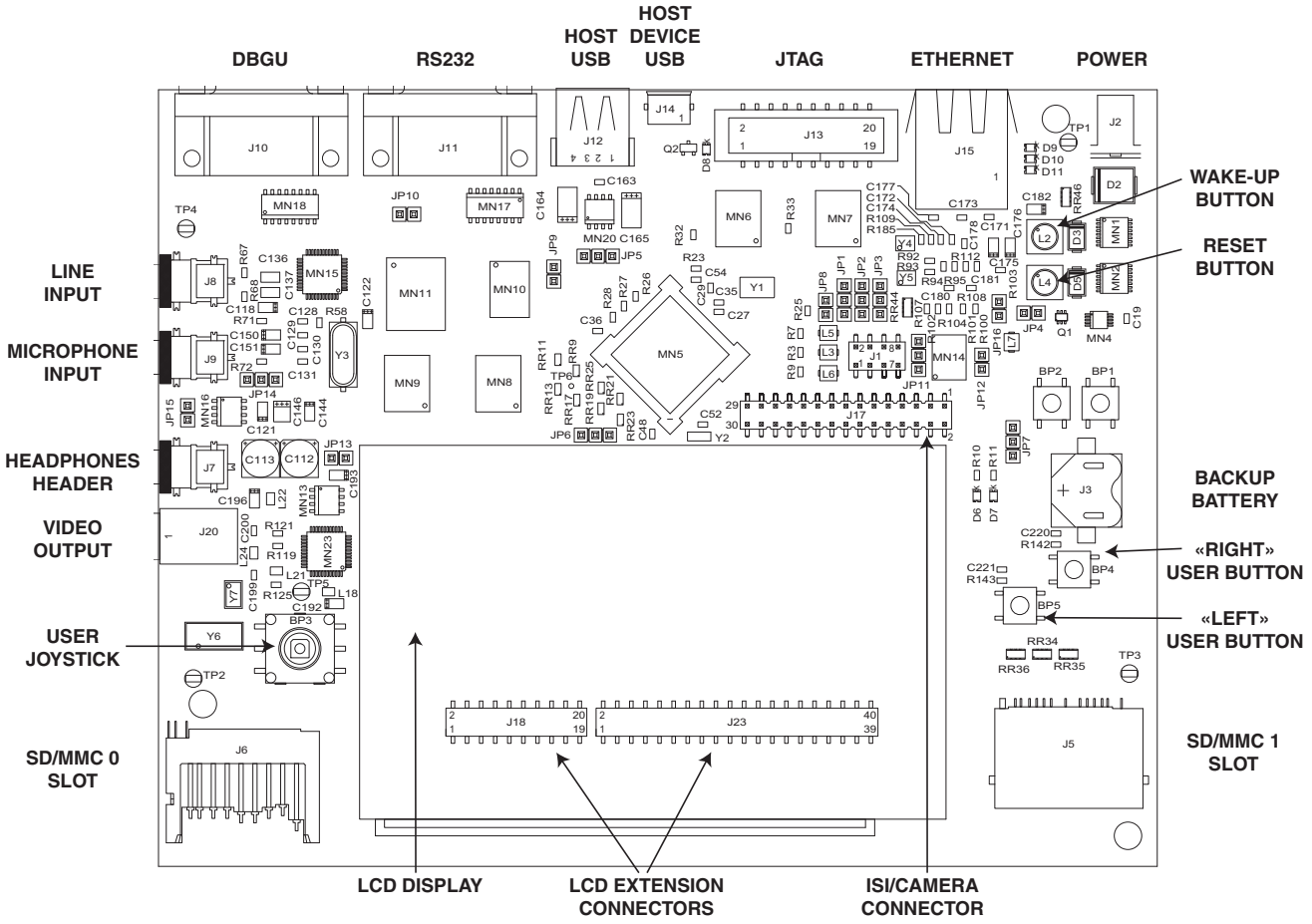
4.1.3 Push Button Switches

- Reset, board reset (BP1)
- Wake up, push button to bring processor out of low power mode (BP2)
- Right and left click, user push button switches (BP4 and BP5)
- Joystick (BP3)

4.1.4 Display LCD and LEDs

- Display, 480xRGBx272 pixels LCD module display connected to the PIO port E (LCD1)
- One surface-mounted power red LED, user interface (D8)
- Two surface-mounted green LEDs, user interface (D6 and D7)
- Three surface-mounted LEDs indicate Ethernet status (D9, D10, D11)

Figure 4-2. Board Layout Commented



The major components of the SAM9G45-EKES board are shown in Figure 4-1.

4.2 Hardware Layout and Configuration

4.2.1 Processor

The board features the Atmel SAM9G45-CU 324-ball TFBGA package. This chip runs at a nominal frequency of 400 MHz for the core and 133 MHz for the system bus.

For more information, refer to the last SAM9G45 datasheet available from http://www.atmel.com/

4.2.2 Clock Circuitry

The SAM9G45-EKES includes six clock sources:

- Two are alternatives for the SAM9G45 main clock,
- One crystal and one crystal oscillator are used for the Ethernet MII/RMII chip,
- One crystal is used for the AC97 codec chip, and
- One crystal or one crystal oscillator is used for the TV encoder.

Table 4-1. Main Components Associated with the Clock Systems

Quantity	Description	Component assignment
1	Crystal for Internal Clock, 12 MHz	Y1
1	Crystal for RTC Clock, 32.768 kHz	Y2
1	Oscillator for Ethernet Clock RMII, 50 MHz	Y4
1	Crystal for Ethernet Clock MII, 25 MHz	Y5
1	Crystal for AC91 Codec Clock, 24.576 MHz	Y3
1	Crystal for TV Encoder Clock, 13 MHz, or Oscillator for TV Encoder, 13 MHz	Y7 Y6

4.2.3 Reset Circuitry

The reset sources are:

- Power on reset
- Push button reset
- JTAG reset from an in-circuit emulator interface.

4.2.4 Memory

4.2.4.1 External Memories

The SAM9G45 features a DDR2/LPDDR memory interface and an External Bus Interface (EBI) to permit interfacing to a wide range of external memories and to almost any kind of parallel peripheral.

The SAM9G45-EKES board is equipped with DDR2/LPDDR devices featuring 128 MB of DDR2-SDRAM memory (Micron MT47H64M8B6-3 16Meg*8*4).

The External Bus Interface (EBI) is connected to three kinds of memory devices:

- One Parallel Flash AT49SV322DT (not populated by default)
- Two DDR2-SDRAM MT47H64M8B6-3
- One NAND Flash MT29F2G16ABD (not populated by default) or MT29F2G08ABD (single footprint)

The chip select NCS0, NCS1 and CS3 are used for NOR Flash, DDR2-SDRAM and NAND Flash memories, respectively. Furthermore, a dedicated jumper can disconnect each of these NCS0, NCS1, and NCS3 signals, making them available for other functions.

Figure 4-3. EBI0 - DDR2

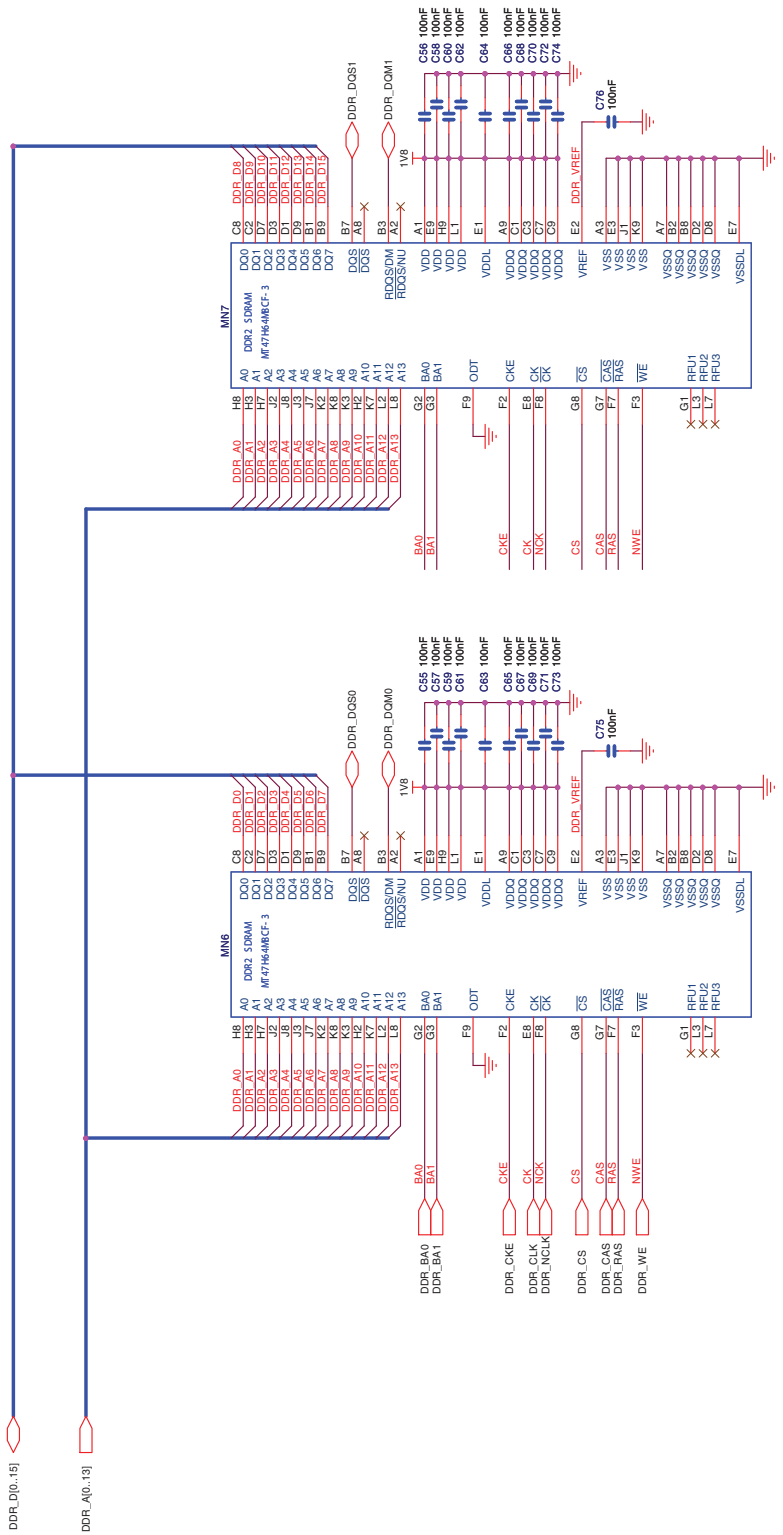
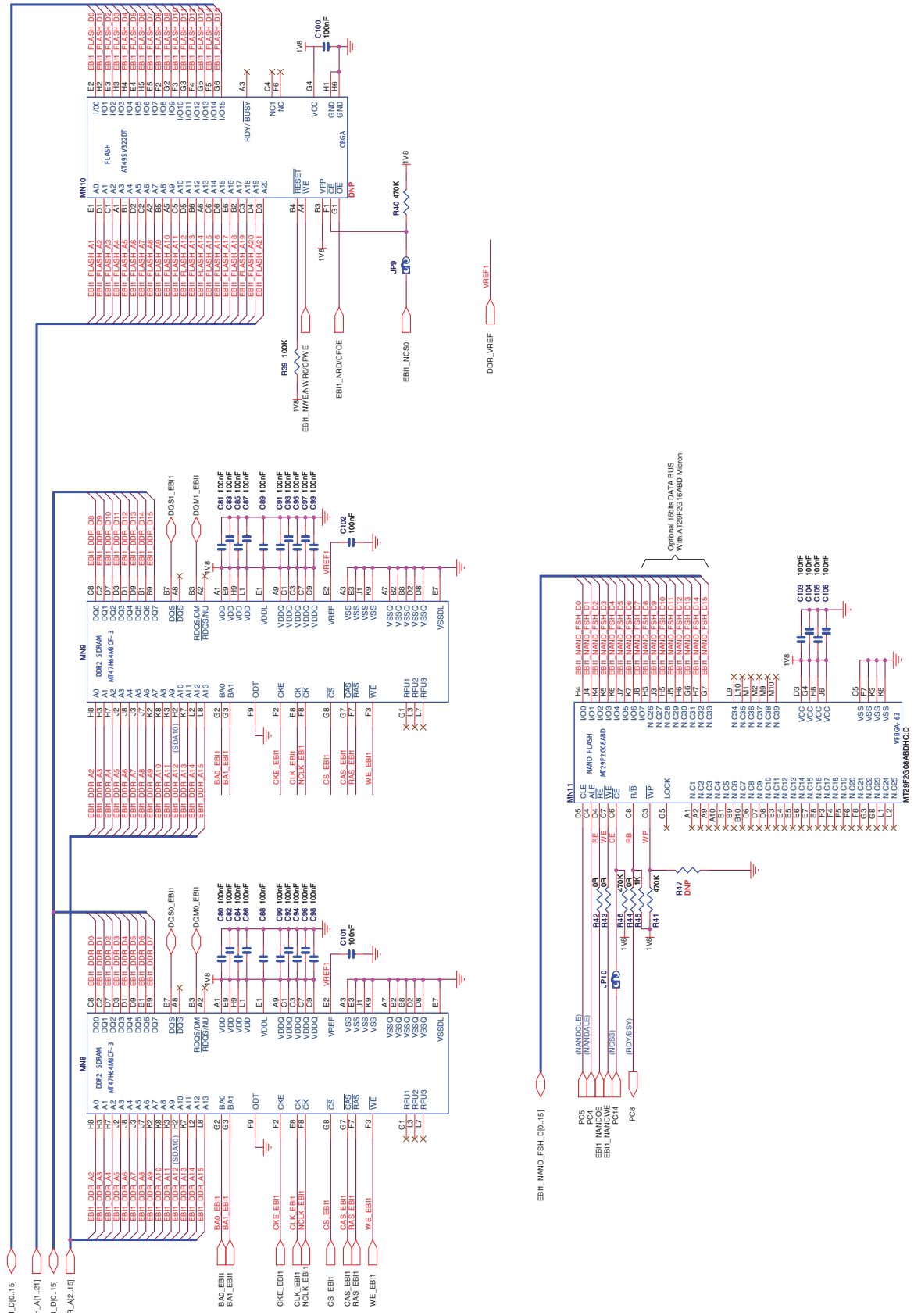


Figure 4-4. EBI1 - DDR2 + Flash



4.2.5 Power Supplies

The SAM9G45 Board contains four regulated power supplies:

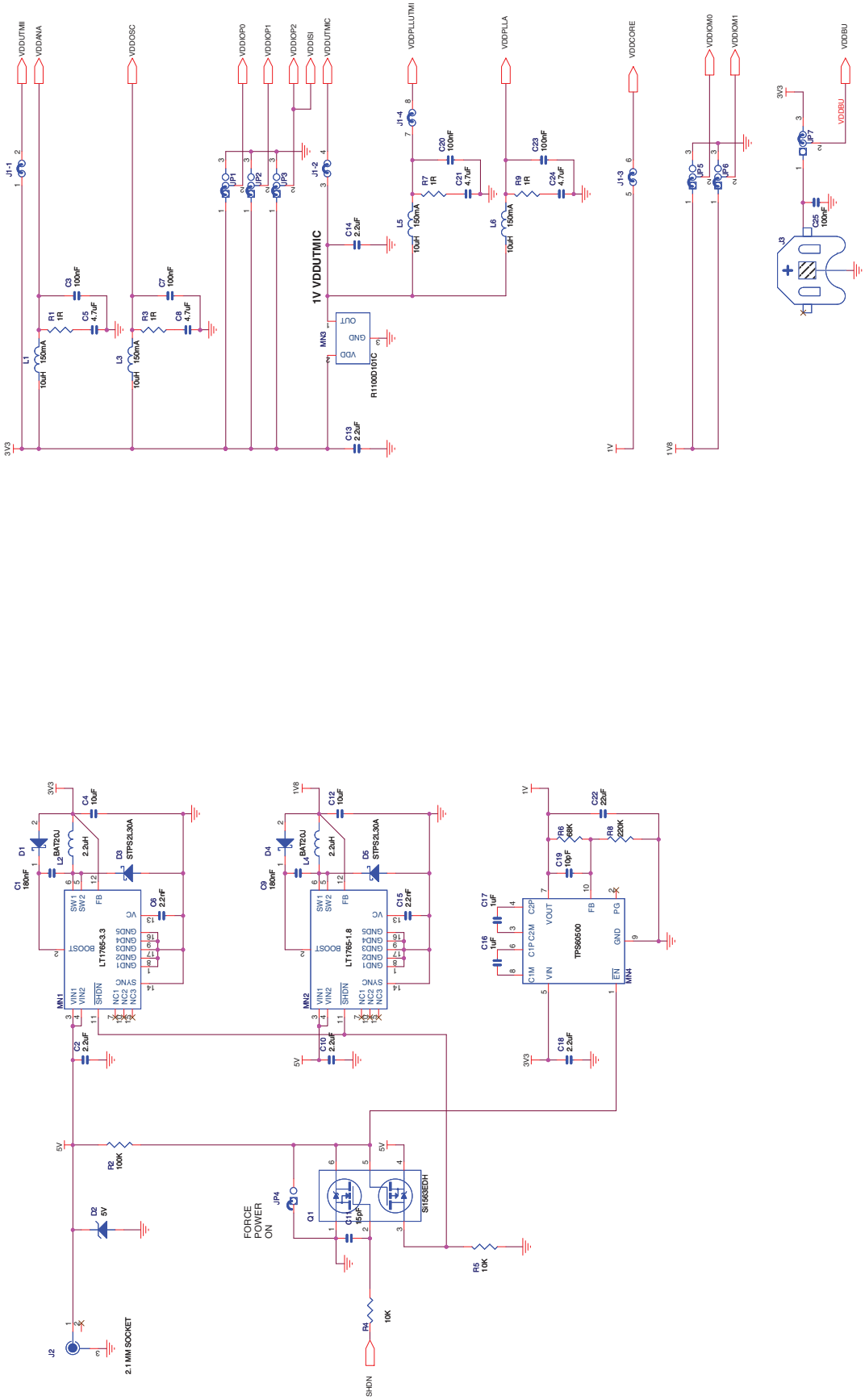
- 3.3 VDC Supply
- 1.8 VDC Supply
- 1.0 VDC Core Supply
- 1.0 VDC Core UTMI Supply, PLL

The outputs of these regulated power supplies[1] are distributed as necessary to each part of the circuit board.

- The 3.3 VDC Supply is generated by an LTC1765-3.3 chip. It accepts VIN 5 VCC power and outputs a regulated +3.3 V to most other circuits in the SAM9G45-VB.
- The 1.8 VDC Supply (VDDIOM0, VDDIOM1) is generated by an LT1765-1.8. It is powered by VIN 5 VCC power and outputs a regulated +1.8V.
- The 1.0 VDC Core Supply (VDDCORE) is generated by a TPS60500 IC. It is powered by the VIN 5 VCC power.
- The 1.0 VDC Core Supply (VDDUTMIC, VDDPLLUTMI and VDDPLLA) is generated by a CMOS voltage regulator R1100D series. It is powered by the output of the 3.3 VDC Supply.

Note: ***1.*** Corresponding test points (TP1 to TP4, GND) are used with jumpers (JP1.1 to JP7) to permit probing of these voltages.

Figure 4-5. Power Supply and Management Power Block

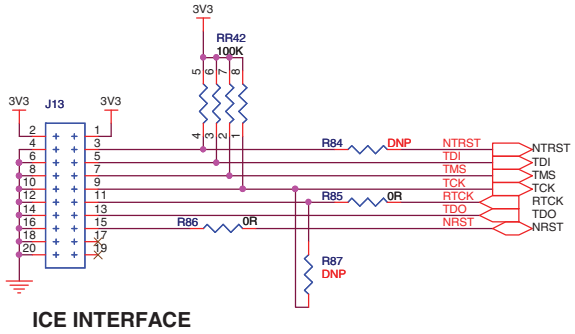


4.2.6 Debug Interface

4.2.6.1 JTAG/ICE

Software debug is accessed by a standard 20-pin JTAG connection. This allows connection to a standard USB-to-JTAG in-circuit emulator.

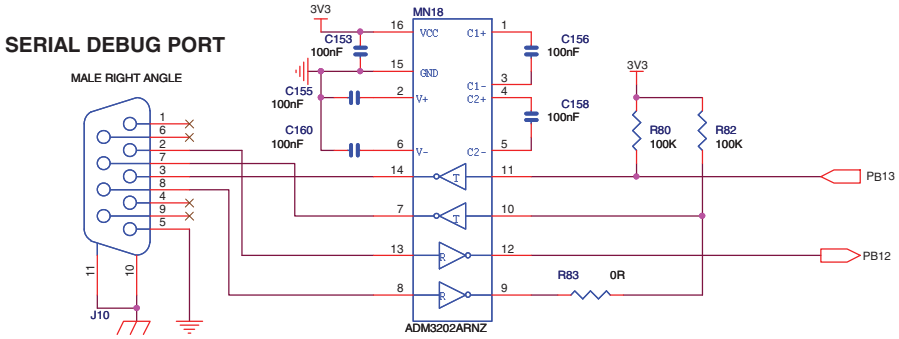
Figure 4-6. JTAG Interface



4.2.6.2 DBGU Com Port

This UART is connected to the DB-9 male socket through an RS-232 Transceiver (TXD and RXD only).

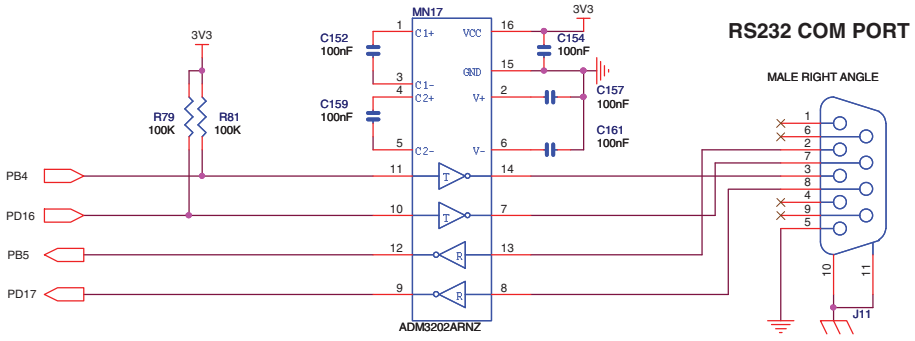
Figure 4-7. DBGU Com Port



4.2.6.3 User Serial Com Port

The USART1 is used as a user serial com port. This USART1 is buffered with an RS-232 Transceiver (TXD, RXD and handshake CTS/RTS control) and connected to the DB-9 male socket. Software must assign the appropriate PIO pins (PB5 = RXD1, PB4 = TXD1, PD16 = RTS1, PD17 = CTS1) to enable the UART1 function.

Figure 4-8. User Serial Com Port



Refer to the SAM9G45 datasheet for more information about the SAM9G45 USARTs.

4.2.6.4 USB Port

The SAM9G45-EKES features USB communication ports:

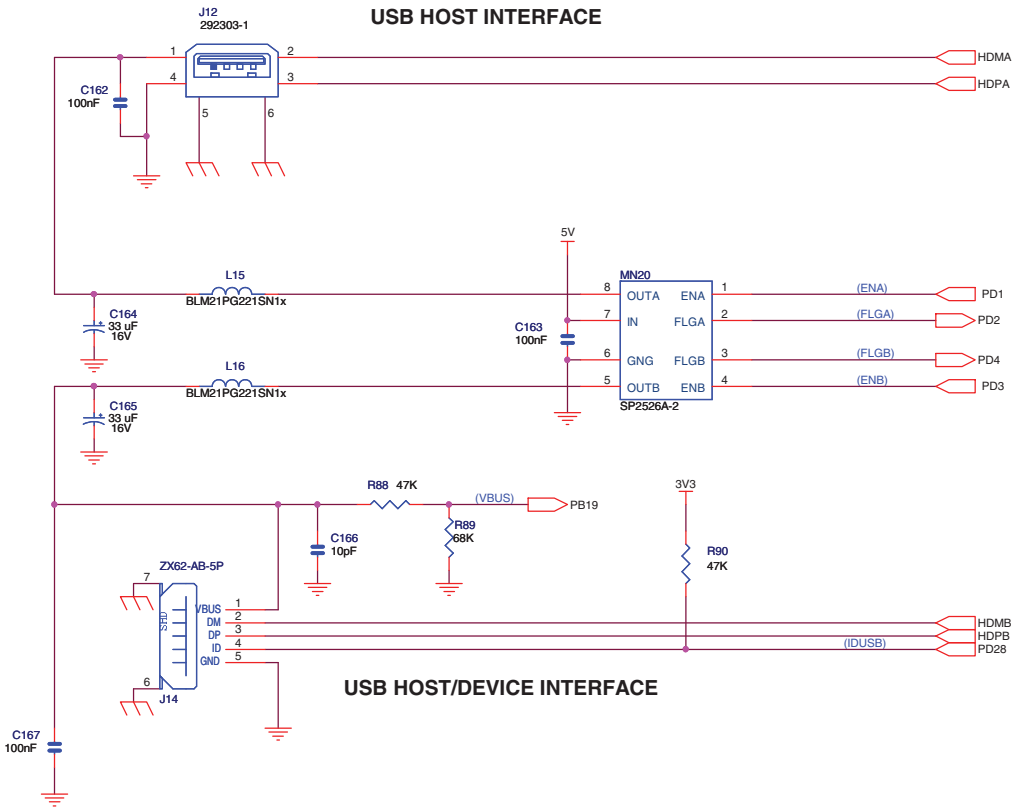
- Two Host Ports: Full speed OHCI and High speed EHCI
- One Device Port: High speed.

USB Host Port0 is directly connected to the first UTMI transceiver. The second Host Port (Port1) is multiplexed with the USB device High speed and connected to the second UTMI port.

- One USB high/full speed type standard A connector
- One USB interface Host/Device Micro AB connector

Refer to the SAM9G45 datasheet for detailed programming information.

Figure 4-9. USB Port



4.2.6.5 Ethernet 10/100 (EMAC) Port

The port is compatible with IEEE® Standard 802.3.

The SAM9G45-EKES is equipped with a Davicom DM9161AEP 10/100 Mbps Fast Ethernet Physical Layer TX/FX Single Chip Transceiver. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE 802.3u, including the Physical Coding Sublayer (PCS), Physical Medium attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10BASE-TX Encoder/Decoder (ENC/DEC), and Twisted Pair Media Access Unit (TPMAU).

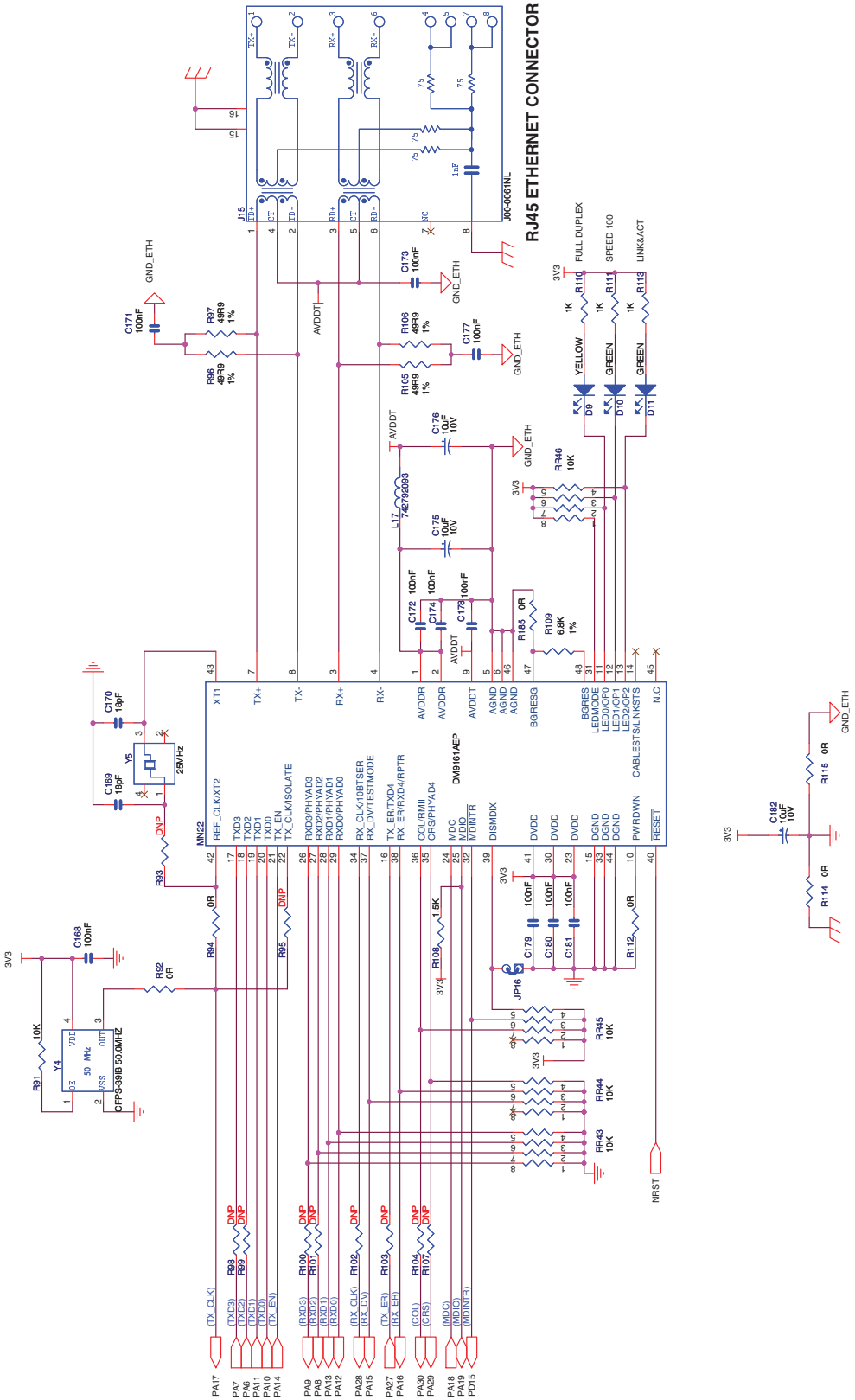
The Ethernet interface integrates an RJ45 connector with an embedded transformer, and three status LEDs.

The Ethernet interface provides two selectable modes, MII or RMII (Reduced MII), for 100Base-Tx or 10Base-Tx. The MII and RMII interfaces are capable of both 10Mb/s and 100Mb/s data rates as described in the IEEE 802.3u standard. The signals used by MII and RMII interfaces are described in the table below.

Table 4-2. Pin Mapping for Normal MII and Reduced MII

Pin Name	Normal MII Mode		Reduced MII Mode	
	SAM9G45	DM9161	SAM9G45	DM9161
ETX0-ETX1	ETX[0:1] transmit data	TXD [0:1]	ETX[0:1]	TXD [0:1]
ETX2-ETX3	ETX[2:3] transmit data	TXD [2:3]	NC	NC
ETXEN	ETXEN: transmit enable	TXEN	ETXEN: transmit enable	TXEN
ETXER	ETXER: transmit error	TXER/TXD[4]	NC	NC
ETXCK/REFCK	ETXCK: transmit clock	TXCLK	REFCK: reference clock	REF_CLK
ERX0-ERX1	ERX[0:1]: receive data	RXD [0:1]	ERX[0:1]: receive data	RXD [0:1]
ERX2-ERX3	ERX[2:3]: receive data	RXD [2:3]	NC	NC
ERXER	ERXER: receive error	RXER/RXD[4]/ RPTR/NODE	ERXER: receive error	RPTR/NODE
ERXDV	ERXDV: receive valid data	RXDV	ECRSDV: carrier sense / data valid	CRS DV
ERXCK	ERXCK: receive clock	RXCLK	NC	NC
ECOL	ECOL: collision detect	COL	NC	NC
ECRS	ECRS: carrier sense / data valid	CRS (PHYAD[2:4]	NC	NC
EMDC	EMDC: management data clock	MDC	EMDC: management data clock	MDC
EMDIO	EMDIO: management data input / output	MDIO	EMDIO: management data input / output	MDIO
NRST	NRST: microcontroller reset	RESET# XT1 (25 MHz)	NRST: microcontroller reset	RESET# XT1 (REF_CLK 50MHz)

Figure 4-10. Ethernet Port



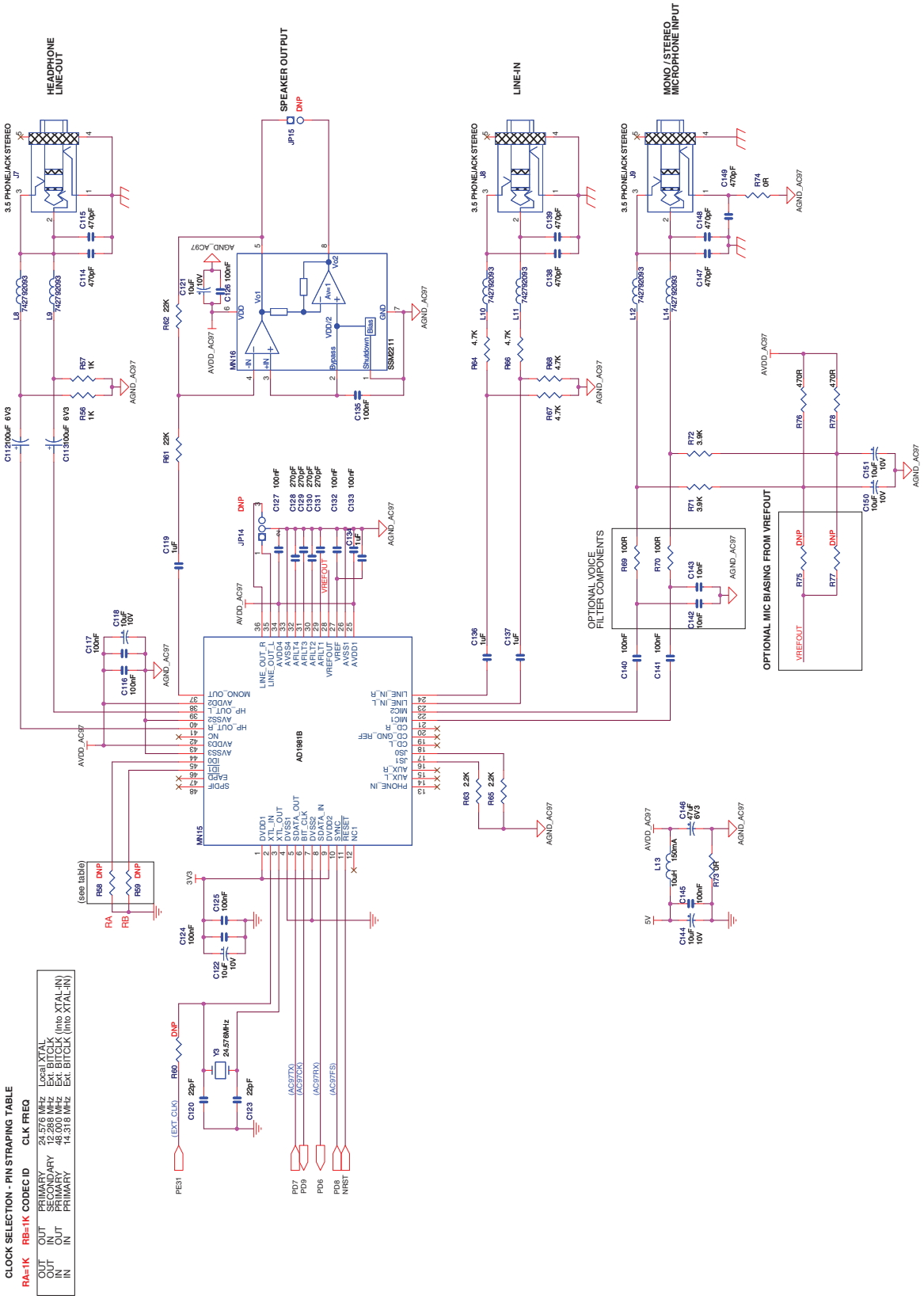
For more information about the Ethernet controller device, refer to the Davicom DM9161 controller manufacturer's datasheet.

4.2.7 Audio Stereo Interface

The SAM9G45-EKES includes an AD1981B AC97 SoundMAX® CODEC for digital sound input and output. This interface includes audio jacks for MIC input (J9), Line audio input (J8), Headphone line output (J7) and a 2-point speaker output connector (JP15).

It is compliant with AC97 Component Specification V2.2.

Figure 4-11. Audio Stereo Interface



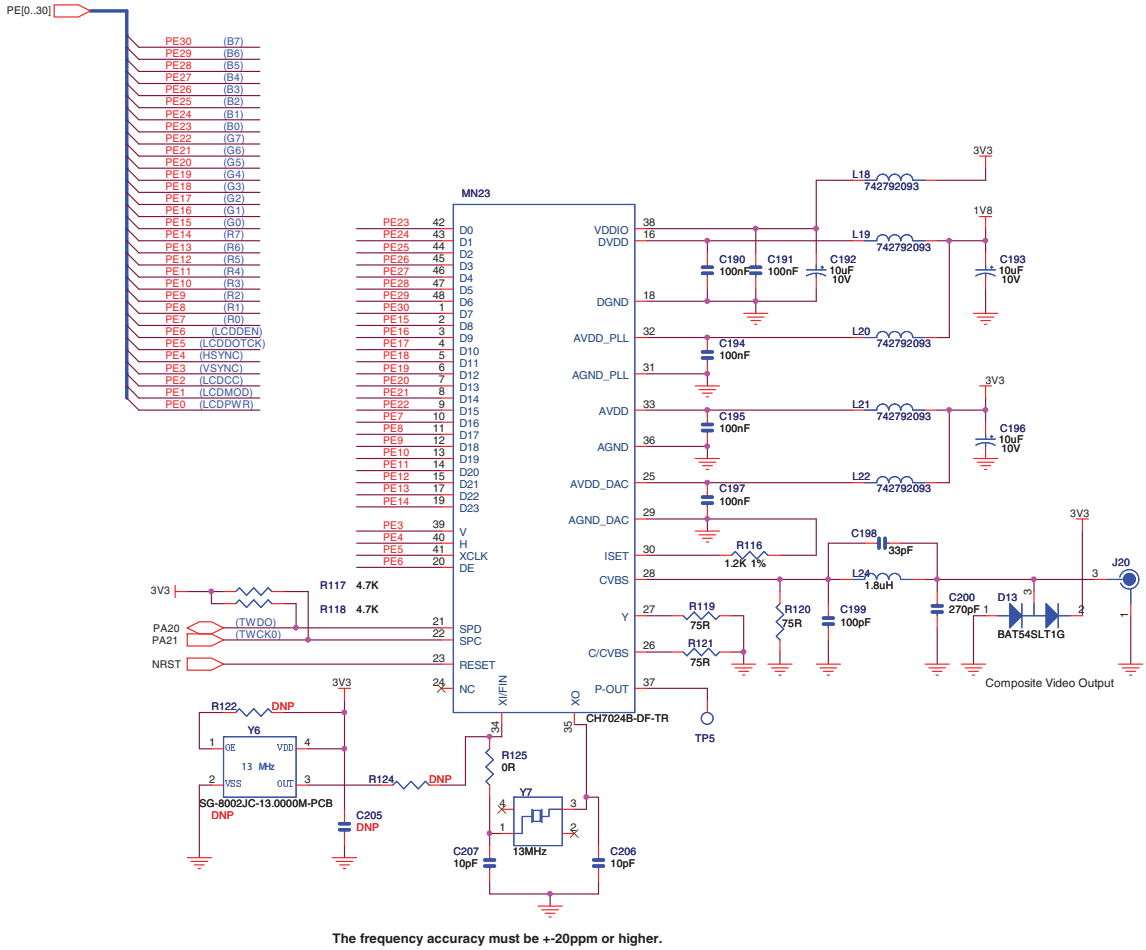
For more information about the AC97 codec device, refer to the Analog Devices AD1981B controller manufacturer's datasheet.

4.2.8 TV-Out Extension

The Chrontel™ CH7024 chip provides an interface between the SAM9G45 LCD Controller and a TV set by converting LCD signals to TV signals.

The CH7024 is a TV encoder device which encodes the video signals and generates synchronization signals for NTSC and PAL standards. Supported TV output formats are NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/A/I, PAL-M, PAL-N and PAL-60. The CH7024 provides video output support for CVBS or S-video.

Figure 4-12. TV-Out Extension Port



4.2.9 Software Controlled LEDs

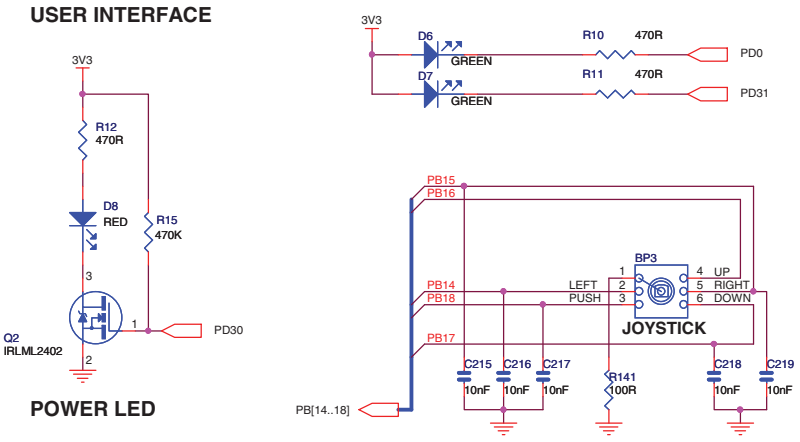
Three users LED are provided for general use. The LEDs are connected to PIO port lines, allowing their control through either GPIO or PWM control.

- LEDs D6 to D8 are software controlled by PIO pins.
- LEDs D9 to D11 indicate Ethernet traffic and link status. These are automatically managed by on-chip microcontroller hardware. See Section 7.1 ”Schematics” .

Table 4-3. Discrete LEDs

LED	Description	Comment
D6	Green LED	User software controlled
D7	Green LED	User software controlled
D8	Red LED	User software controlled
D9	Yellow LED	Indicates transmission or reception via Ethernet
D10	Green LED	Indicates speed 100
D11	Green LED	Is lit when a good link test has been detected

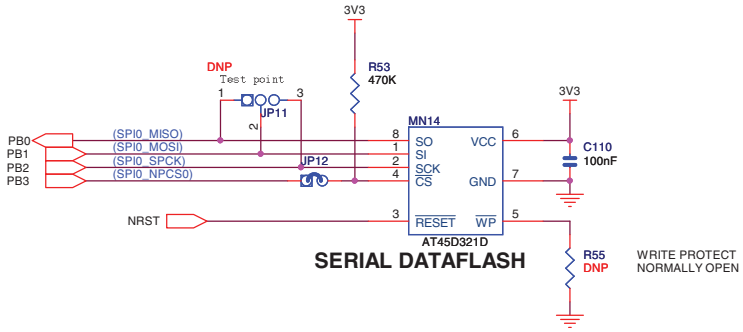
Figure 4-13. Software Controlled LEDs



4.2.10 Serial Peripheral Interface Controller (SPI)

The SAM9G45 provides two high-speed Serial Peripheral Interface (SPI) controllers. One port is used to interface with the on-board serial EEPROM.

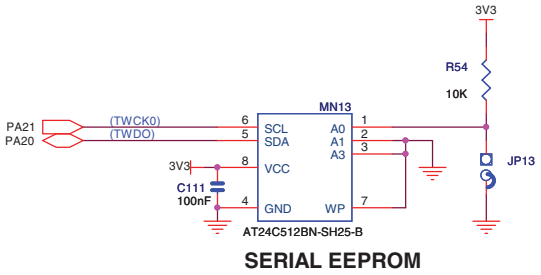
Figure 4-14. SPI



4.2.11 Two Wire Interface (TWI)

The SAM9G45 has a full speed (400 kHz) master/slave I2C Serial Controller. The controller is fully compatible with the industry standard I2C and SMBus Interfaces. This port is used to interface with the on-board Serial DataFlash, ISI and TV encoder interface.

Figure 4-15. TWI



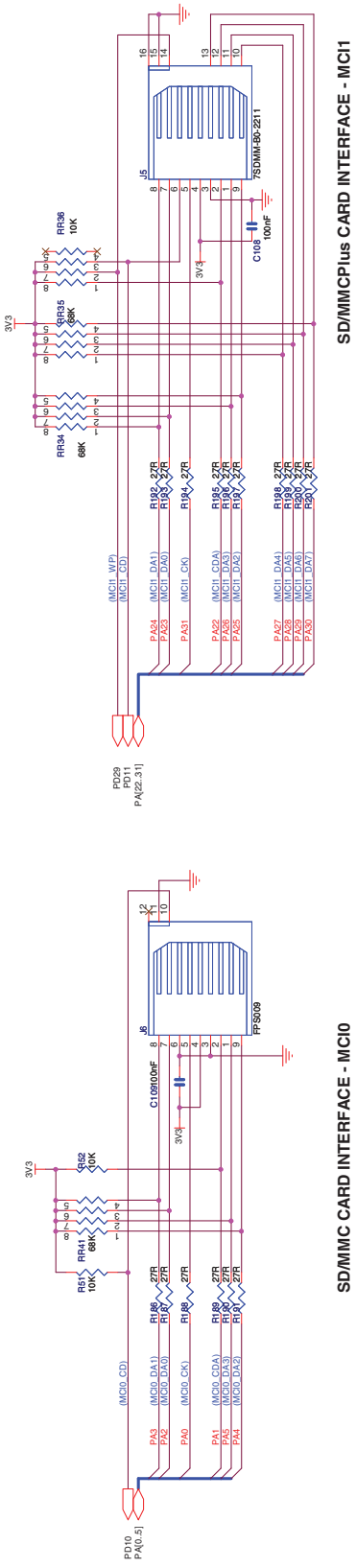
4.2.12 SD/MMC Interface

The SAM9G45-EKES has two high-speed 8-bit multimedia interfaces MMC/MMCPlus v4.1. The first interface is used as an 8-bit interface (MCI1), connected to a CE-ATA connector footprint and an 8-bit SD/MMC card slot. The second interface is used as a 4-bit interface (MCI0), connected to a 4-bit SD/MMC card slot.

The users must provide their own compatible cards for use with these connectors.

Please note that the power is connected to VCC, which is 3.3 volts.

Figure 4-16. SD/MMC0-MMC1



4.2.13 TFT LCD with Touch Panel

The SAM9G45 features an LCD controller. A 4.3" 480x272 Portrait Mode LCD provides the SAM9G45-EKES with a low power LCD display, back light unit and a touch panel, similar to that used on commercial PDAs.

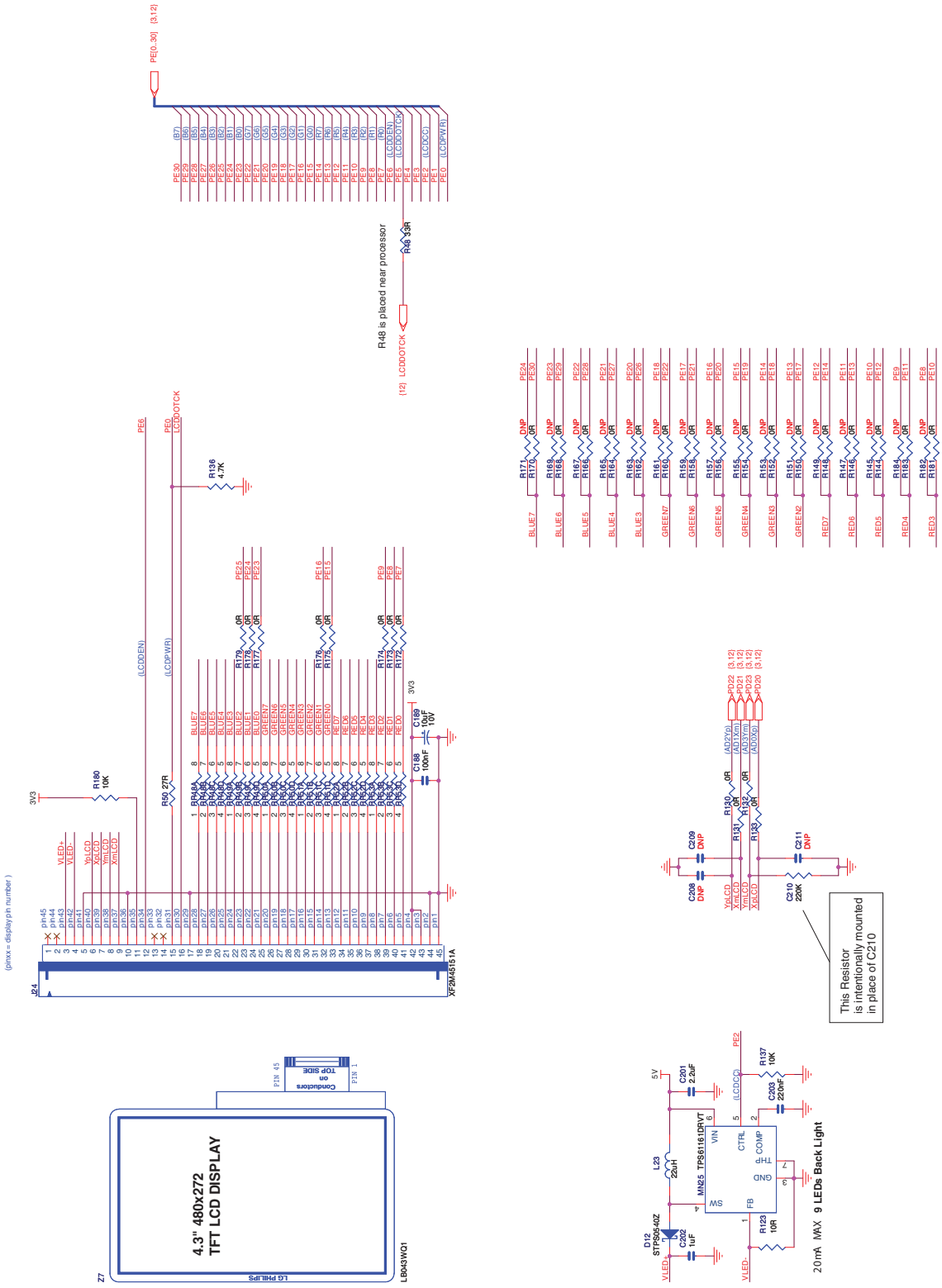
The TFT LCD component is an LG®/PHILIPS®, model number LB043WQ1.

Graphics and text can be displayed on the dot matrix panel with up to 16 million colors by supplying 24-bit data signals (8bitxRGB by default) or 16-bit data signals (5+6+5bitxRGB in option). This allows the user to develop graphical user interfaces for a wide variety of end applications.

Warning: never connect/disconnect the LCD display from the board while the power supply is on. Doing so may damage both units and is not covered by warranty.

The back light voltage is generated from a TPS61161 boost converter. It is powered directly by the VIN 5 VCC power (the control for the back light voltages is separated from the main board voltages due to the specific voltage requirements of the LCD panel).

Figure 4-17. TFT LCD

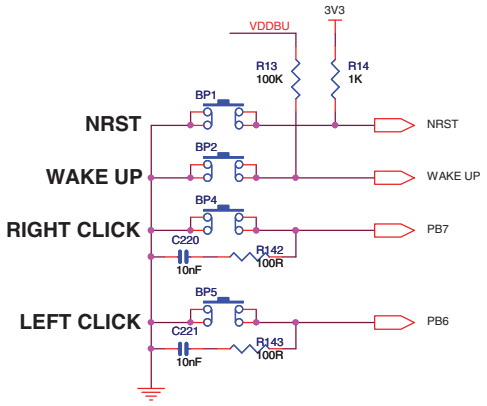


4.2.14 Push Buttons

The SAM9G45-EKES is equipped with two system push buttons, two user push buttons and one joystick. The push buttons consist of momentary push button switches mounted directly to the board. When any switch is depressed, a low (zero) appears at the associated input pin.

- System push buttons:
  - Reset, perform system reset
  - Wakeup, perform system wake up
- User push button:
  - Right click
  - Left click
- Joystick:
  - One touch, 5-way switching,
  - Normally open momentary contacts,
  - Push down to select in any position.

Figure 4-18. Push Buttons

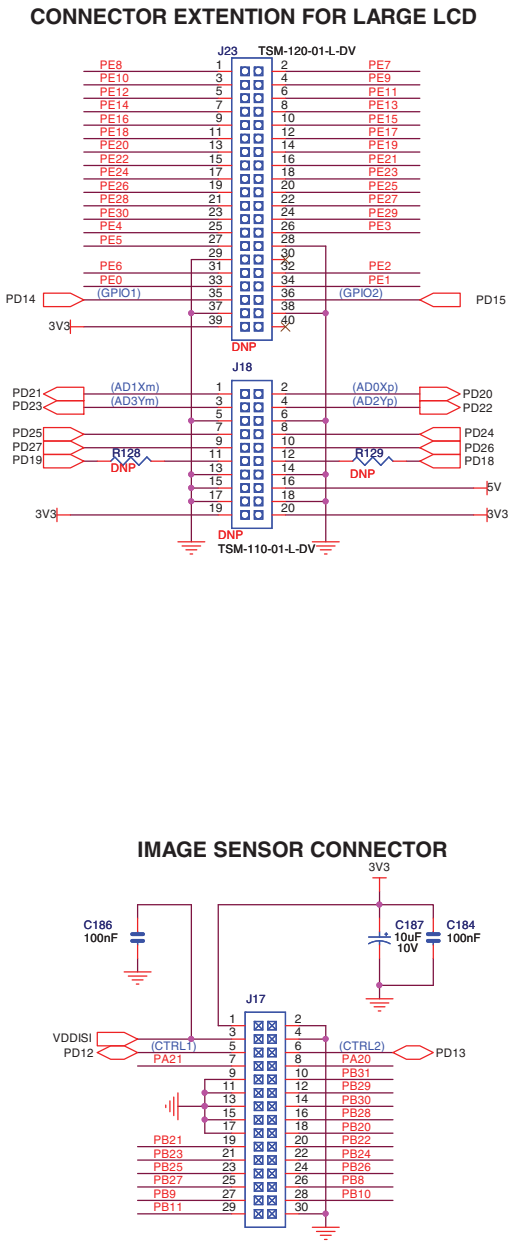


4.2.15 Expansion Slot

- GPIO1 & GPIO2, LCD signals (PIO E) are routed to the connectors extension J23
- All I/Os of the SAM9G45 Image Sensor Interface are routed to connectors J17
- Touch screen signals and analog I/O are connected to J18

This allows the developer to extend the features of the board by adding external hardware components or boards.

Figure 4-19. Expansion Slot



Section 5
Configuration

5.1 JTAG/ICE Configuration

Table 5-1. JTAG/ICE Configuration

Designation	Default Setting	Feature
R84	Not populated	Disables the ICE NTRST input
R85	Soldered	Enables the ICE RTCK return. R87 must be opened
R86	Soldered	Enables the ICE NRST input
R87	Not populated	Disables TCK <-> RTCK local loop

5.2 ETHERNET Configuration

RMII is the factory default mode.

To evaluate the MII mode, the user has to unsolder R92 and solder R93, R98 to R104, R107.

Two types of jumpers are used on the SAM9G45-EKES board:

- 2-pin jumpers with two possible settings:
  - Fitted: the circuit is closed, and
  - Not fitted: the circuit is open
- 3-pin jumpers with two possible positions, for which settings are presented in the following tables.

5.3 Jumpers Configuration

Table 5-2. Jumpers Configuration

Designation	Default Setting	Feature			
J1 (combined jumper array)	Closed	J1-1	1-2	VDDUTMII	3V3
	Closed	J1-2	3-4	VDDUTIMC	1V
	Closed	J1-3	5-6	VDDCORE	1V
	Closed	J1-4	7-8	VDDPLLUTMI	1V
JP1	1-2	JP1	1-2	VDDIOP0	3V3
			2-3	External power to VDDIOP0	3V3 nominal
JP2	1-2	JP2	1-2	VDDIOP1	3V3
			2-3	External power to VDDIOP1	3V3 nominal
JP3	1-2	JP3	1-2	VDDIOP2	3V3
			2-3	External power to VDDIOP2	3V3 nominal
JP4	Opened	Forces power on. To use the software shutdown control, JP4 must be opened. 3V battery backup must be present and JP7 jumper set in position 1-2			
JP5	1-2	JP5	1-2	VDDIOM0	1V8
			2-3	External power to VDDIOM0	1V8 nominal
JP6	1-2	JP6	1-2	VDDIOM1	1V8
			2-3	External power to VDDIOM1	1V8 nominal
JP7	1-2	JP7	1-2	VDDBU	Lithium 3V Battery
			2-3	VDDBU	3.3V from regulator
JP8	Opened	BMS Enables Boot on the internal ROM; closed selects the boot from the external device connected to NCS0			
JP9	Closed	Enables chip select access, Boot on the NCS0 (MN10 Flash)			
JP10	Closed	Enables chip select access, Boot on the NCS3 (MN12 NAND Flash)			
JP11	Test point	JP11.1: SO		JP11.2: SI	JP11.3: SCK
JP12	Closed	Enables chip select access, Boot on the SPIO_NPCS0 (Serial Data Flash MN14)			
JP13	Opened	Set address A0 low (MN13 Serial EEPROM), enable Boot access.			
JP14		JP14.1 = Line_Out_L		JP14.3 = Line_Out_R	
JP15		Used to connect a Loudspeaker			
JP16	Closed	DISMDIX (MN22)			

5.4 Miscellaneous Configuration Items

N.P = not populated

P = populated

Table 5-3. Miscellaneous Configuration

Designation	Default Setting	Feature
R20	N.P	JTAGSEL
R21	P	Connect TSADVREF to VDDANA (may be used for specific filtering)
R22	P	Connect GNDANA to GND (may be used for specific filtering)
R24	P	Force TST pin to GND (chip is set in non-test mode = normal operation mode)
R47	N.P	Write protect NAND Flash (mount a 0-ohm resistor to write-protect the NAND Flash device)
R55	N.P	Write protect serial Data Flash (mount a 0-ohm resistor to write-protect the serial Flash device)
R58, R59	N.P	Clock selection Audio AC97 (see mapping table in Section 7.1 ”Schematics”)
R60	N.P	External clock Audio AC97 (mount a 0-ohm resistor to connect it)
R75, R77	N.P	Change bias from VREFOUT (see Section 7.1 ”Schematics”)
R69, R70		Voice filter components
R84,R85 R86,R87		ICE interface reset and clocking schemes (see Section 5.1 ”JTAG/ICE Configuration”)
R92, R93, R94, R95, R98, R99 R100, R101 R102,R103 R104,R107 R112		Ethernet interface, MII mode (see Section 5.2 ”ETHERNET Configuration”)
Y6, R122, R124	N.P	External 13 MHz oscillator (option) for the on-board video composite encoder
TP1		GND Test point
TP2		GND Test point
TP3		GND Test point
TP4		GND Test point

5.5 PIO Configuration

5.5.1 Peripheral Signals Multiplexing on I/O Lines

The AT91SAMG45 product features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplex the I/O lines of the peripheral set. Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of peripherals A and B are multiplexed on the PIO Controllers.

5.5.2 Multiplexing on PIO Controller A (PIOA)

"R.Select" = connection selectable via an on-board resistor (default not populated)

Table 5-4. PIO Multiplexing Port A

I/O	Peripheral A	Peripheral B		Function and Comments		Power
PA0	MCI0_CK	TCLK3		MMCI0 Clock		VDDIOP0
PA1	MCI0_CDA	TIOA3		MMCI0 Command		VDDIOP0
PA2	MCI0_DA0	TIOB3		MMCI0 Data0		VDDIOP0
PA3	MCI0_DA1	TCKL4		MMCI0 Data1		VDDIOP0
PA4	MCI0_DA2	TIOA4		MMCI0 Data2		VDDIOP0
PA5	MCI0_DA3	TIOB4		MMCI0 Data3		VDDIOP0
PA6	MCI0_DA4	ETX2		Ethernet MII		VDDIOP0
PA7	MCI0_DA5	ETX3		Ethernet MII		VDDIOP0
PA8	MCI0_DA6	ERX2		Ethernet MII		VDDIOP0
PA9	MCI0_DA7	ERX3		Ethernet MII		VDDIOP0
PA10	ETX0			Ethernet RMII Transmit data 0		VDDIOP0
PA11	ETX1			Ethernet RMII Transmit data 1		VDDIOP0
PA12	ERX0			Ethernet RMII Receive data 0		VDDIOP0
PA13	ERX1			Ethernet RMII Receive data 1		VDDIOP0
PA14	ETXEN			Ethernet RMII Transmit enable		VDDIOP0
PA15	ERXDV			Ethernet RMII Receive data valid		VDDIOP0
PA16	ERXER			Ethernet RMII Receive Error		VDDIOP0
PA17	ETXCK			Ethernet RMII Transmit Clock		VDDIOP0
PA18	EMDC			Ethernet RMII Manag.Data Clock		VDDIOP0
PA19	EMDIO			Ethernet RMII Manag.Data In/Out		VDDIOP0
PA20	TWD0			Two Wire Interface Data		VDDIOP0
PA21	TWCK0			Two Wire Interface Clock		VDDIOP0
PA22	MCI1_CDA	SCK3		MMCI1 Command		VDDIOP0
PA23	MCI1_DA0	RTS3		MMCI1 Data0		VDDIOP0
PA24	MCI1_DA1	CTS3		MMCI1 Data1		VDDIOP0
PA25	MCI1_DA2	PWM3		MMCI1 Data2		VDDIOP0
PA26	MCI1_DA3	TIOB2		MMCI1 Data3		VDDIOP0
PA27	MCI1_DA4	ETXER	R.Select	MMCI1 Data4	Ethernet MII	VDDIOP0
PA28	MCI1_DA5	ERXCK	R.Select	MMCI1 Data5	Ethernet MII	VDDIOP0
PA29	MCI1_DA6	ECRS	R.Select	MMCI1 Data6	Ethernet MII	VDDIOP0
PA30	MCI1_DA7	ECOL	R.Select	MMCI1 Data7	Ethernet MII	VDDIOP0
PA31	MCI1_CK	PCK0		MMCI1_clock		VDDIOP0

5.5.3 Multiplexing on PIO Controller B (PIOB)

Table 5-5. PIO Multiplexing Port B

I/O	Peripheral A	Peripheral B		Function and Comments	Power
PB0	SPI0_MISO			SPI Slave Out AT45DB642	VDDIOP0
PB1	SPI0_MOSI			SPI Slave In AT45DB642	VDDIOP0
PB2	SPI0_SPCK			SPI Serial Clock AT45DB642	VDDIOP0
PB3	SPI0_NPCS0			SPI Chip Select AT45DB642	VDDIOP0
PB4	TXD1			USART1 Transmit Data	VDDIOP0
PB5	RXD1			USART1 Receive Data	VDDIOP0
PB6	TXD2			User Push Button Right click	VDDIOP0
PB7	RXD2			User Push Button Left click	VDDIOP0
PB8	TXD3	ISI_D8		Image Sensor Data 8	VDDIOP2
PB9	RXD3	ISI_D9		Image Sensor Data 9	VDDIOP2
PB10	TWD1	ISI_D10		Image Sensor Data 10	VDDIOP2
PB11	TWCK1	ISI_D11		Image Sensor Data 11	VDDIOP2
PB12	DRXD			DBGU Receive Data	VDDIOP0
PB13	DTXD			DBGU Transmit Data	VDDIOP0
PB14	SPI1_MISO			Joystick Left	VDDIOP0
PB15	SPI1_MOSI	CTS0		Joystick Right	VDDIOP0
PB16	SPI1_SPCK	SCK0		Joystick Up	VDDIOP0
PB17	SPI1_NPCS0	RTS0		Joystick Down	VDDIOP0
PB18	RXD0	SPI0_NPCS1		Joystick Push	VDDIOP0
PB19	TXD0	SPI0_NPCS2		UsbVbus	VDDIOP0
PB20	ISI_D0			Image Sensor Data 0	VDDIOP2
PB21	ISI_D1			Image Sensor Data 1	VDDIOP2
PB22	ISI_D2			Image Sensor Data 2	VDDIOP2
PB23	ISI_D3			Image Sensor Data 3	VDDIOP2
PB24	ISI_D4			Image Sensor Data 4	VDDIOP2
PB25	ISI_D5			Image Sensor Data 5	VDDIOP2
PB26	ISI_D6			Image Sensor Data 6	VDDIOP2
PB27	ISI_D7			Image Sensor Data 7	VDDIOP2
PB28	ISI_PCK			Image Sensor Data Clock	VDDIOP2
PB29	ISI_VSYNC			Image Sensor Vertical Synchro	VDDIOP2
PB30	ISI_HSYNC			Image Sensor Horizontal Synchro	VDDIOP2
PB31	ISI_MCK	PCK1		Image Sensor Reference Clock	VDDIOP2

5.5.4 Multiplexing on PIO Controller C (PIOC)

Table 5-6. PIO Multiplexing Port C

I/O	Peripheral A	Peripheral B		Function and Comments	Power
PC0	DQM2				VDDIOM1
PC1	DQM3				VDDIOM1
PC2	A19			Add19 Flash AT49SV322	VDDIOM1
PC3	A20			Add20 Flash AT49SV322	VDDIOM1
PC4	A21/NANDALE			ALE Flash AT49SV322	VDDIOM1
PC5	A22/NANDCLE			CLE Flash AT49SV322	VDDIOM1
PC6	A23				VDDIOM1
PC7	A24				VDDIOM1
PC8	CFCE1			Ready/Busy NAND Flash	VDDIOM1
PC9	CFCE2	RTS2			VDDIOM1
PC10	NCS4/CFCS0	TCLK2			VDDIOM1
PC11	NCS5/CFCS1	CTS2			VDDIOM1
PC12	A25/CFRNW				VDDIOM1
PC13	NCS2				VDDIOM1
PC14	NCS3/NANDCS			Chip select NAND Flash	VDDIOM1
PC15	NWAIT				VDDIOM1
PC16	D16				VDDIOM1
PC17	D17				VDDIOM1
PC18	D18				VDDIOM1
PC19	D19				VDDIOM1
PC20	D20				VDDIOM1
PC21	D21				VDDIOM1
PC22	D22				VDDIOM1
PC23	D23				VDDIOM1
PC24	D24				VDDIOM1
PC25	D25				VDDIOM1
PC26	D26				VDDIOM1
PC27	D27				VDDIOM1
PC28	D28				VDDIOM1
PC29	D29				VDDIOM1
PC30	D30				VDDIOM1
PC31	D31				VDDIOM1

5.5.5 Multiplexing on PIO Controller D (PIOD)

Table 5-7. PIO Multiplexing Port D

I/O	Peripheral A	Peripheral B		Function and Comments	Power
PD0	TK0	PWM3		Command LED2	VDDIOP0
PD1	TF0			Output ENA USB Host	VDDIOP0
PD2	TD0			Input FLGA USB Host	VDDIOP0
PD3	RD0			Output ENB USB Host	VDDIOP0
PD4	RK0			Input FLGB USB Host	VDDIOP0
PD5	RF0			Int. Ethernet 10/100 MDINTR	VDDIOP0
PD6	AC97RX			AC97 Receive Signal	VDDIOP0
PD7	AC97TX	TIOA5		AC97 Transmit Signal	VDDIOP0
PD8	AC97FS	TIOB5		AC97 Frame Sync Signal	VDDIOP0
PD9	AC97CK	TCLK5		AC97 Clock Signal	VDDIOP0
PD10	TD1			Card Detect MMCI0 MCI0_CD	VDDIOP0
PD11	RD1			Card Detect MMCI1 MCI1_CD	VDDIOP0
PD12	TK1	PCK0		CTRL1 Image Sensor Interface	VDDIOP0
PD13	RK1			CTRL2 Image Sensor Interface	VDDIOP0
PD14	TF1			GPIO1 Large LCD (connector)	VDDIOP0
PD15	RF1			GPIO2 Large LCD (connector)	VDDIOP0
PD16	RTS1			USART1 Request to Send	VDDIOP0
PD17	CTS1			USART1 Clear To Send	VDDIOP0
PD18	SPI1_NPCS2	IRQ			VDDIOP0
PD19	SPI1_NPCS3	FIQ			VDDIOP0
PD20	TIOA0		TSAD0	Touch screen X_Right	VDDANA
PD21	TIOA1		TSAD1	Touch screen X_Left	VDDANA
PD22	TIOA2		TSAD2	Touch screen Y_Up	VDDANA
PD23	TCLK0		TSAD3	Touch screen Y_Down	VDDANA
PD24	SPI0_NPCS1	PWM0	GPAD4	General purpose A/D4	VDDANA
PD25	SPI0_NPCS2	PWM1	GPAD5	General purpose A/D5	VDDANA
PD26	PCK0	PWM2	GPAD6	General purpose A/D6	VDDIOP0
PD27	PCK1	SPI0_NPCS3	GPAD7	General purpose A/D7	VDDIOP0
PD28	TSADTRG	SPI1_NPCS1		USB Plug-ID IDUSB	VDDIOP0
PD29	TCLK1	SCK1		MCI1_WP	VDDIOP0
PD30	TIOB0	SCK2		Command Power Led	VDDIOP0
PD31	TIOB1	PWM1		Command LED1	VDDIOP0

5.5.6 Multiplexing on PIO Controller E (PIOE)

Table 5-8. PIO Multiplexing Port E

I/O	Peripheral A	Peripheral B		Function and Comments	Power
PE0	LCDPWR	PCK0		LCD Panel Pow.Enab.Ctrl	VDDIOP1
PE1	LCDMOD			LCD Modulation Signal	VDDIOP1
PE2	LCDCC			LCD Contrast Control	VDDIOP1
PE3	LCDVSYNC			LCD Vertical Synch.	VDDIOP1
PE4	LCDHSYNC			LCD Horizontal Synch.	VDDIOP1
PE5	LCDDOTCK			LCD Dot Clock	VDDIOP1
PE6	LCDDEN			LCD Data Enable	VDDIOP1
PE7	LCDD0	LCDD2		LCD-Red0	VDDIOP1
PE8	LCDD1	LCDD3		LCD-Red1	VDDIOP1
PE9	LCDD2	LCDD4		LCD-Red2	VDDIOP1
PE10	LCDD3	LCDD5		LCD-Red3	VDDIOP1
PE11	LCDD4	LCDD6		LCD-Red4	VDDIOP1
PE12	LCDD5	LCDD7		LCD-Red5	VDDIOP1
PE13	LCDD6	LCDD10		LCD-Red6	VDDIOP1
PE14	LCDD7	LCDD11		LCD-Red7	VDDIOP1
PE15	LCDD8	LCDD12		LCD-Green0	VDDIOP1
PE16	LCDD9	LCDD13		LCD-Green1	VDDIOP1
PE17	LCDD10	LCDD14		LCD-Green2	VDDIOP1
PE18	LCDD11	LCDD15		LCD-Green3	VDDIOP1
PE19	LCDD12	LCDD18		LCD-Green4	VDDIOP1
PE20	LCDD13	LCDD19		LCD-Green5	VDDIOP1
PE21	LCDD14	LCDD20		LCD-Green6	VDDIOP1
PE22	LCDD15	LCDD21		LCD-Green7	VDDIOP1
PE23	LCDD16	LCDD22		LCD-Blue0	VDDIOP1
PE24	LCDD17	LCDD23		LCD-Blue1	VDDIOP1
PE25	LCDD18			LCD-Blue2	VDDIOP1
PE26	LCDD19			LCD-Blue3	VDDIOP1
PE27	LCDD20			LCD-Blue4	VDDIOP1
PE28	LCDD21			LCD-Blue5	VDDIOP1
PE29	LCDD22			LCD-Blue6	VDDIOP1
PE30	LCDD23			LCD-Blue7	VDDIOP1
PE31	PWM2	PCK1		AC97 External Clock	VDDIOP1

Section 6

Connectors

6.1 Power Supply

The AT91SAMG45-EKES evaluation board can be powered from a DC 5V power supply via the external power supply jack (J2) shown in Figure 10 1. The positive pole must be on J2 center pin.

Figure 6-1. Power Supply Connector J2

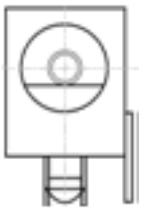


Table 6-1. Power Supply Connector J2 Signal Description

Pin	Mnemonic	Signal description
1	Center	+5 VCC
2	Gnd	

6.2 RS232 Connector with RTS/CTS Handshake Support

Connector J11 is the COM1 connector.

Figure 6-2. RS232 COM1 Connector J11

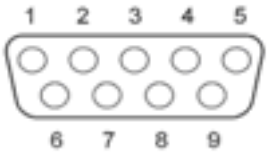


Table 6-2. Serial COM1 Connector J11 Signal Descriptions

Pin	Mnemonic	Signal description
1, 4, 6, 9	NC	NO CONNECTION
2	TXD TRANSMITTED DATA	RS232 serial data output signal
3	RXD RECEIVED DATA	RS232 serial data input signal
5	GND	GROUND
7	RTS READY TO SEND	Active-positive RS232 input signal
8	CTS CLEAR TO SEND	Active-positive RS232 output signal

6.3 DBGU

Connector J10 is the DBGU connector.

Figure 6-3. RS232 DBGU Connector J10

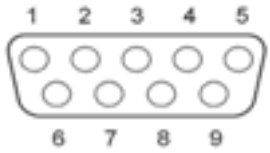


Table 6-3. RS232 DBGU Connector J10 Signal Descriptions

Pin	Mnemonic	Signal description
1, 4, 6, 7, 8, 9	NC	NO CONNECTION
2	TXD TRANSMITTED DATA	RS232 serial data output signal
3	RXD RECEIVED DATA	RS232 serial data input signal
5	GND	GROUND

6.4 Ethernet

Connector J15 is the RJ-45 Ethernet Connector.

Figure 6-4. Ethernet RJ45 Connector J15

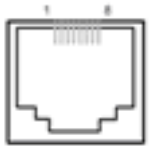


Table 6-4. Ethernet RJ45 Connector J15 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
1	TxData+ DIFFERENTIAL OUTPUT PLUS	2	Txdata- DIFFERENTIAL OUTPUT MINUS
3	RxData+ DIFFERENTIAL INPUT PLUS	4	Shield
5	Shield	6	RxData- DIFFERENTIAL INPUT MINUS
7	Shield	8	Shield

6.5 USB Host

Connector J12 is the USB Host connector.

Figure 6-5. USB Host type A connector J12

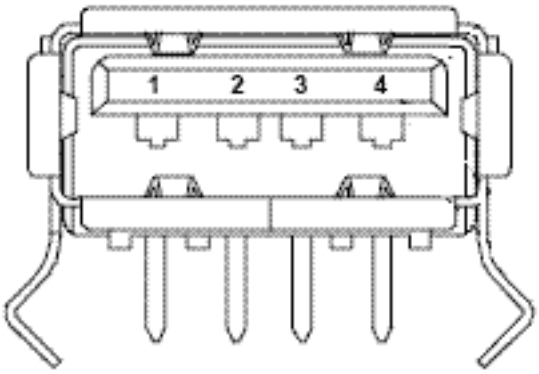


Table 6-5. USB Host Type A Connector J12 Signal Descriptions

Pin	Mnemonic	Signal description
1	Vbus	5v power
2	DM	Data minus
3	DP	Data plus
4	Gnd	Ground
5	Shield	Shield

6.6 USB Host/Device

Connector J14 is the USB Host/Device connector.

Figure 6-6. USB Host/Device Micro AB connector J14

Table 6-6. USB Host/Device MicroAB Connector J14 Signal Descriptions

Pin	Mnemonic	Signal description
1	Vbus	5v power
2	DM	Data minus
3	DP	Data plus
4	ID	On the Go Identification
5	Gnd	Ground

6.7 JTAG Debugging Connector

Connector J13 is the JTAG/ICE connector.

A SAM-ICE connector is a 20-way Insulation Displacement Connector (IDC) keyed box header (2.54 mm male) that mates with IDC sockets mounted on a ribbon cable.

Figure 6-7. JTAG/ICE Connector J13

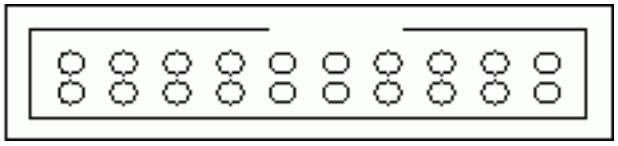


Table 6-7. JTAG/ICE Connector J13 Signal Descriptions

Pin	Mnemonic	Description
1	VTref. 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply. 3.3V power	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST TARGET RESET - Active-low output signal that resets the target	JTAG Reset. Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground
5	TDI TEST DATA INPUT - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground
7	TMS TEST MODE SELECT	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground
9	TCK TEST CLOCK - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
10	GND	Common ground
11	RTCK - Input Return test clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND
12	GND	Common ground
13	TDO JTAG TEST DATA OUTPUT - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground
15	nSRST RESET	Active-low reset signal. Target CPU reset signal
16	GND	Common ground
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Common ground
19	RFU	This pin is not connected in SAM-ICE
20	GND	Common ground

6.8 SD/MMC- MCI0

Connector J6 is the SD/MMC connector.

Figure 6-8. SD/MMC0 Connector J6

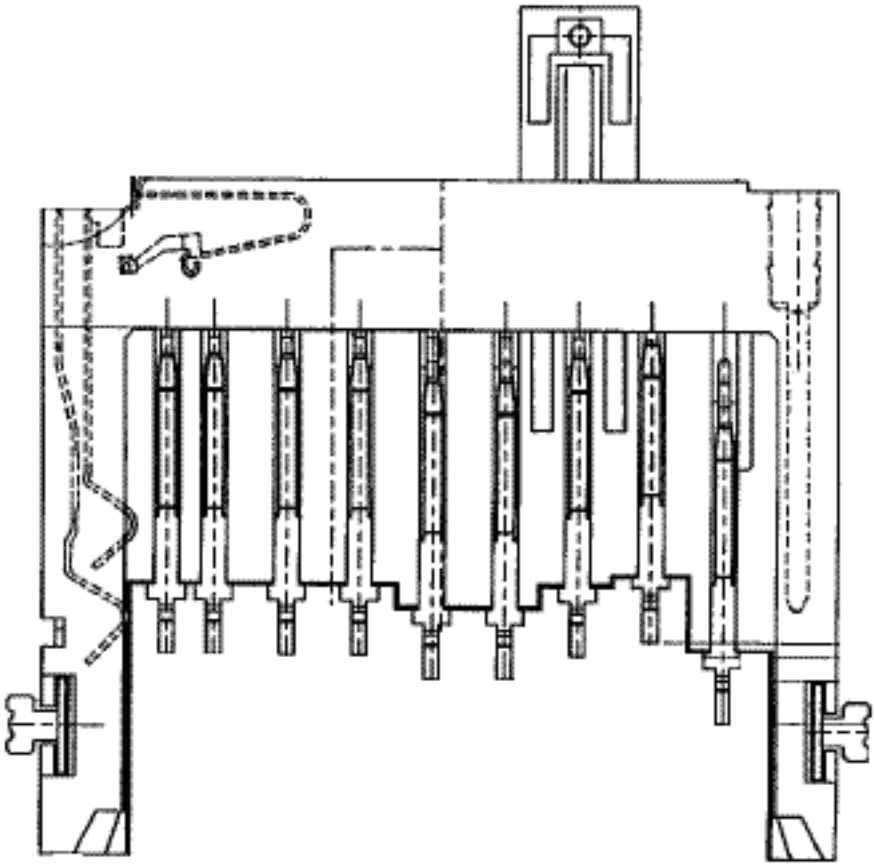


Table 6-8. SD/MMC0 Connector J6 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
1	RSV/DAT3	2	CDA
3	GND	4	VCC
5	CLK	6	GND
7	DAT0	8	DAT1
9	DAT2	10	Card Detect
11	GND	12	

6.9 SD/MMC- MCI1

Connector J5 is the SD/MMC connector.

Figure 6-9. SD/MMC1 Connector J5

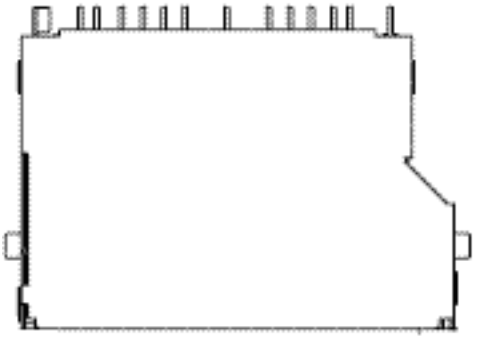


Table 6-9. SD/MMC1 Connector J5 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
1	RSV/DAT3	2	CMD
3	GND	4	VCC
5	CLK	6	
7	DAT0	8	DAT1
9	DAT2	10	DAT3
11	DAT4	12	DAT5
13	DAT6	14	DAT7

6.10 AC97

- Connector J7 is the Headphone connector.
- Connector J8 is the Line In connector.
- Connector J9 is the Line In connector.
- Connector JP15 is the Speaker Output connector

Figure 6-10. Audio Connector J7, J8, J9

Table 6-10. J7, J8, J9 Signal Description

Pin	Mnemonic
Central pin	Signal

Table 6-11. Speaker JP15 Signal Descriptions

Pin	Mnemonic
1	Speaker bridge output A
2	Speaker bridge output B

6.11 Image Sensor - ISI

Connector J17 is the ISI connector.

Figure 6-11. ISI Connector J17

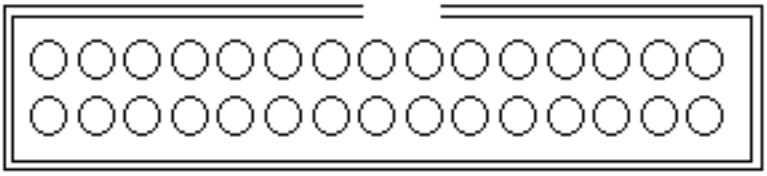


Table 6-12. ISI Connector J17 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
1	VCC 3v3	2	Gnd
3	VCC 3v3	4	Gnd
5	Ctrl1	6	Ctrl2
7	SCL	8	SDA
9	Gnd	10	ISI_MCK
11	Gnd	12	ISI_VSYNC
13	Gnd	14	ISI_HSYNC
15	Gnd	16	ISI_PCK
17	Gnd	18	ISI_Data0
19	ISI_Data1	20	ISI_Data2
21	ISI_Data3	22	ISI_Data4
23	ISI_Data5	24	ISI_Data6
25	ISI_Data7	26	ISI_Data8
27	ISI_Data9	28	ISI_Data10
29	ISI_Data11	30	Gnd

6.12 Video

Connector J20 is the Video connector

Figure 6-12. Video Connector J20

Table 6-13. Video Connector J20 Signal Description

Pin	Mnemonic	Signal description
1	Center	Composite video signal output

6.13 Display Devices

6.13.1 LG TFT LCD LG/PHILIPS

Connector J24 is the TFT-LCD connector.

Figure 6-13. TFT LCD Connector J24

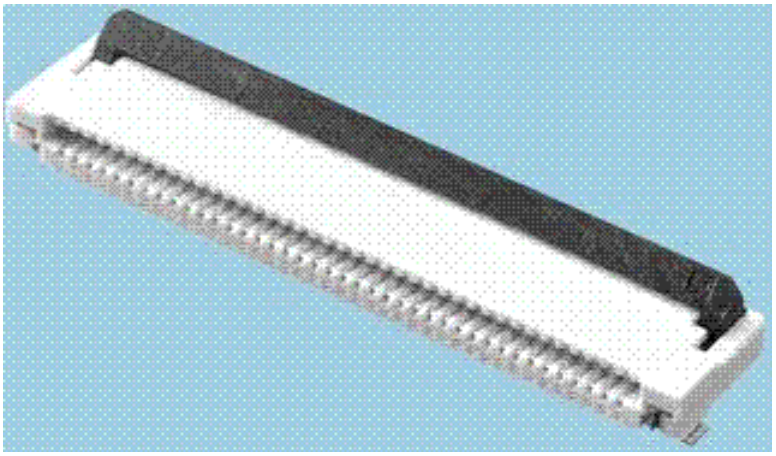


Table 6-14. LG TFT LCD Connector J24 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
1	GND	2	GND
3	VDD 3V3	4	VDD 3V3
5	R0	6	R1
7	R2	8	R3
9	R4	10	R5

Table 6-14. LG TFT LCD Connector J24 Signal Descriptions

Pin	Mnemonic	Pin	Mnemonic
11	R6	12	R7
13	G0	14	G1
15	G2	16	G3
17	G4	18	G5
19	G6	20	G7
21	B0	14	B1
23	B2	16	B3
25	B4	18	B5
27	B6	20	B7
29	GND	30	DCLK
31	DISPON	32	NO CONNECT
33	NO CONNECT	34	LCDEN
35	VDD PWR SEL	36	GND
37	X1	38	Y1
39	X2	40	Y2
41	GND	42	VLED-
43	VLED+	44	NO CONNECT
45	NO CONNECT		

6.14 Large LCD Extension

Connectors J23 and J18 are for an optional large LCD extension (not populated).

Table 6-15. Connector J23 Signal Description for a Large LCD Extension

Pin		Mnemonic	Pin		Mnemonic
1	PE8	RED Data Signal	2	PE7	RED Data Signal (LSB)
3	PE10	RED Data Signal	4	PE9	RED Data Signal
5	PE12	RED Data Signal	6	PE11	RED Data Signal
7	PE14	RED Data Signal (MSB)	8	PE13	RED Data Signal
9	PE16	GREEN Data Signal	10	PE15	GREEN Data Signal (LSB
11	PE18	GREEN Data Signal	12	PE17	GREEN Data Signal
13	PE20	GREEN Data Signal	14	PE19	GREEN Data Signal
15	PE22	GREEN Data Signal (MSB)	16	PE21	GREEN Data Signal
17	PE24	BLUE Data Signal	18	PE23	BLUE Data Signal (LSB)
19	PE26	BLUE Data Signal	20	PE25	BLUE Data Signal
21	PE28	BLUE Data Signal	22	PE27	BLUE Data Signal
23	PE30	BLUE Data Signal (MSB)	24	PE29	BLUE Data Signal

Table 6-15. Connector J23 Signal Description for a Large LCD Extension

Pin		Mnemonic	Pin		Mnemonic
25	PE4	LCDHSYNC	26	PE3	LCDVSYNC
27	PE5	LCDDOTCK	28	GND	(0V)
29	GND	(0V)	30	NC	
31	PE6	LCDDEN	32	PE2	LCDCC
33	PE0	DISPON	34	PE1	LCDMOD
35	PD14	GPIO1	36	PD15	GPIO2
37	GND	(0V)	38	GND	(0V)
39	VCC	+3V3 power source	40	NC	

Table 6-16. Connector J18 Signal Description for a Large LCD Extension

Pin		Mnemonic	Pin		Mnemonic
1	XM	AD1XM	2	XP	AD0XP
3	YM	AD3YM	4	YP	AD2YP
5	GND	(0V)	6	GND	(0V)
7	PD25	PD25	8	PD24	PD24
9	PD27	PD27	10	PD26	PD26
11	PD19	PD19	12	PD18	PD18
13	GND	(0V)	14	GND	(0V)
15	GND	(0V)	16		+5V
17	GND	(0V)	18	GND	(0V)
19	VCC	+3V3 power source	20	VCC	+3V3 power source

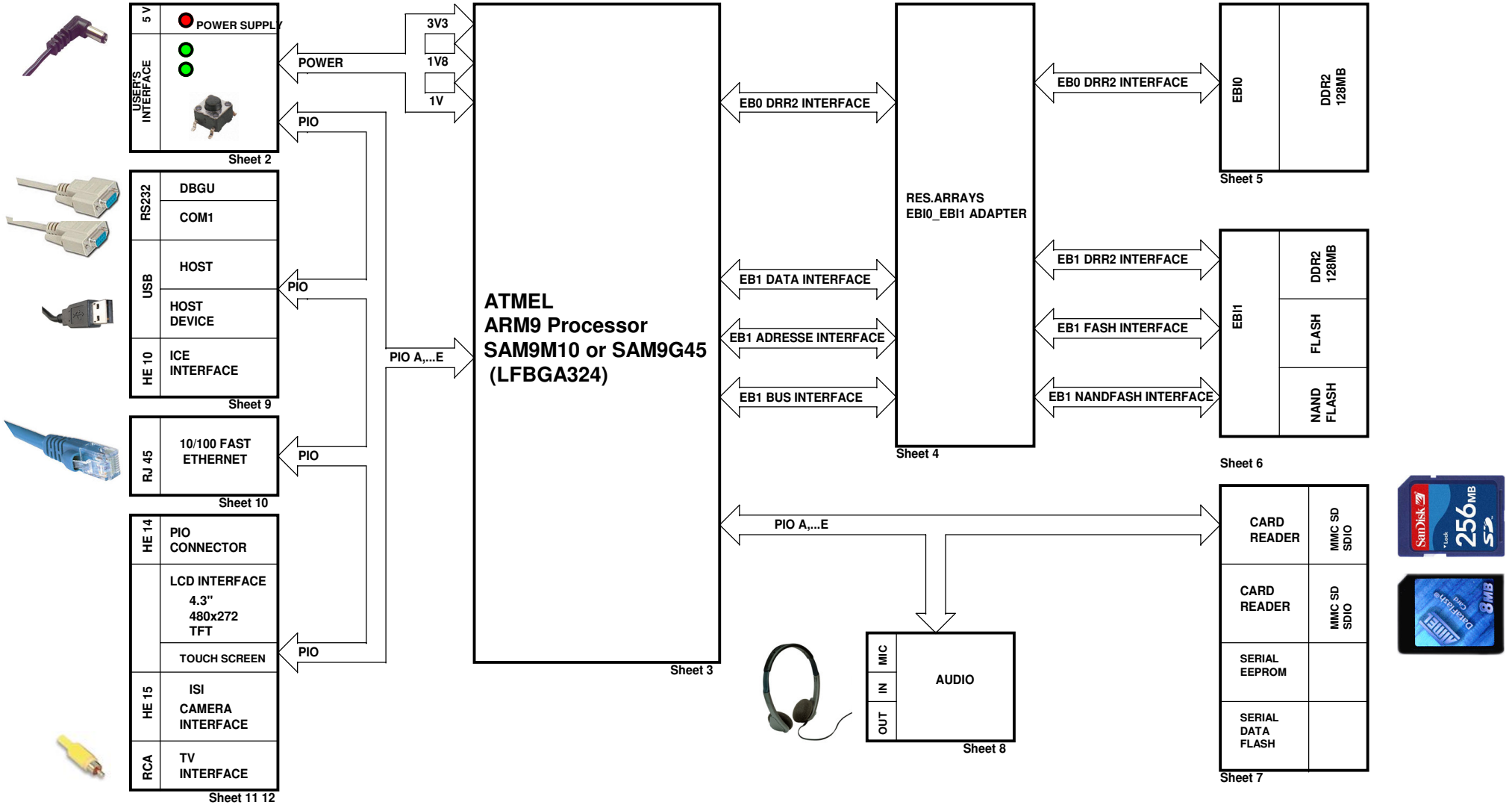
Section 7

Schematics

7.1 Schematics

This section contains the following schematics:

- Top Level view, block architecture of the design
- Power Supply
- SAM Processor
- Bus impedance adaptor
- Main memory
- EBI memory
- MCI & TWI
- Audio AC97
- Serial interfaces
- Ethernet
- LCD
- Video interfaces and LCD extension



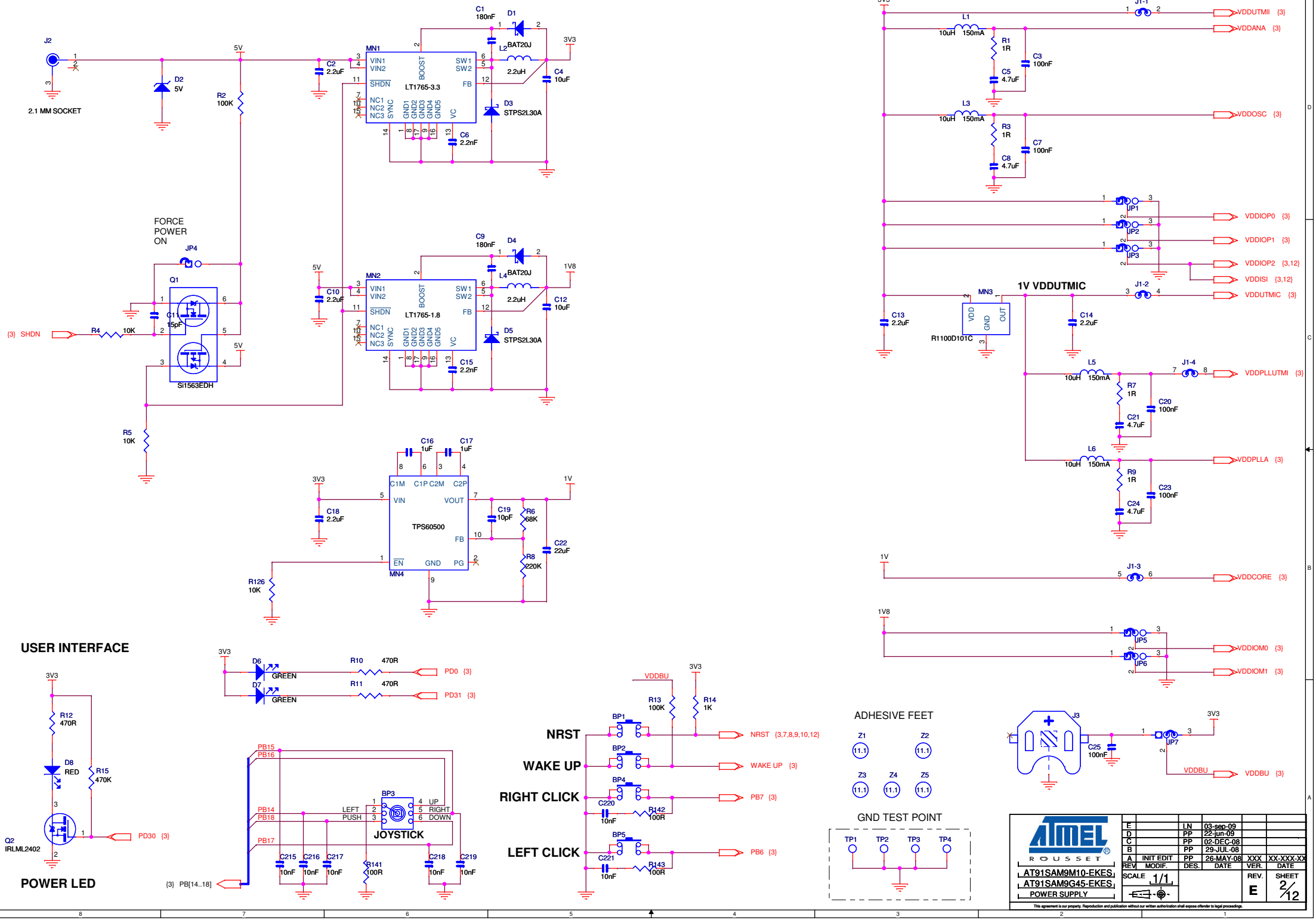
PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE	PIOD		PIOD		PIOE		PIOE	
PA0	MCI0_CK	PA16	RX_ER	PB0	SPI0_MISO	PB16	BP3_UP	PC0	NOT USED	PC16	NOT USED	PD0	USER_LED_D6	PD16	RTS1	PE0	LCDPWR	PE16	G1
PA1	MCI0_CDA	PA17	TX_CLK	PB1	SPI0_MOSI	PB17	BP3_DOWN	PC1	NOT USED	PC17	NOT USED	PD1	ENA	PD17	CTS1	PE1	LCDMOD	PE17	G2
PA2	MCI0_DA0	PA18	MDC	PB2	SPI0_SPCK	PB18	BP3_PUSH	PC2	A19	PC18	NOT USED	PD2	FLGA	PD18	J18_12	PE2	LCDCC	PE18	G3
PA3	MCI0_DA1	PA19	MDIO	PB3	SPI0_NPCS0	PB19	VBUS	PC3	A20	PC19	NOT USED	PD3	ENB	PD19	J18_11	PE3	VSYNC	PE19	G4
PA4	(MCI0_DA2)	PA20	TWDO	PB4	TXD1	PB20	ISI_D0	PC4	NANDALE / A21	PC20	NOT USED	PD4	FLGB	PD20	AD0Xp	PE4	HSYNC	PE20	G5
PA5	(MCI0_DA3)	PA21	TWCK0	PB5	RXD1	PB21	ISI_D1	PC5	NANDCLE	PC21	NOT USED	PD5	MDINTR	PD21	AD1Xm	PE5	LCDDOTCK	PE21	G6
PA6	TXD2	PA22	MCI1_CDA	PB6	BP5_LEFT	PB22	ISI_D2	PC6	NOT USED	PC22	NOT USED	PD6	AC97RX	PD22	AD2Yp	PE6	LCDDEN	PE22	G7
PA7	TXD3	PA23	MCI1_DA0	PB7	BP4_RIGHT	PB23	ISI_D3	PC7	NOT USED	PC23	NOT USED	PD7	AC97TX	PD23	AD3Ym	PE7	R0	PE23	B0
PA8	RXD2	PA24	MCI1_DA1	PB8	ISI_D8	PB24	ISI_D4	PC8	RDY/BSY	PC24	NOT USED	PD8	AC97FS	PD24	J18_8	PE8	R1	PE24	B1
PA9	RXD3	PA25	MCI1_DA2	PB9	ISI_D9	PB25	ISI_D5	PC9	NOT USED	PC25	NOT USED	PD9	AC97CK	PD25	J18_7	PE9	R2	PE25	B2
PA10	TXD0	PA26	MCI1_DA3	PB10	ISI_D10	PB26	ISI_D6	PC10	NOT USED	PC26	NOT USED	PD10	MCI0_CD	PD26	J18_10	PE10	R3	PE26	B3
PA11	TXD1	PA27	MCI1_DA4 / TX_ER	PB11	ISI_D11	PB27	ISI_D7	PC11	NOT USED	PC27	NOT USED	PD11	(MCI1_CD)	PD27	J18_9	PE11	R4	PE27	B4
PA12	RXD0	PA28	MCI1_DA5 / RX_CLK	PB12	DRXD	PB28	ISI_PCK	PC12	NOT USED	PC28	NOT USED	PD12	CTRL1	PD28	IDUSB	PE12	R5	PE28	B5
PA13	RXD1	PA29	MCI1_DA6 / CRS	PB13	DTXD	PB29	ISI_VSYNC	PC13	NOT USED	PC29	NOT USED	PD13	CTRL2	PD29	(MCI1_WP)	PE13	R6	PE29	B6
PA14	TX_EN	PA30	MCI1_DA7 / COL	PB14	BP3_LEFT	PB30	ISI_HSYNC	PC14	NCS3	PC30	NOT USED	PD14	GPIO1	PD30	POWER LED	PE14	R7	PE30	B7
PA15	RX_DV	PA31	MCI1_CK	PB15	BP3_RIGHT	PB31	ISI_MCK	PC15	NOT USED	PC31	NOT USED	PD15	GPIO2	PD31	USER_LED_D7	PE15	G0	PE31	EXT_CLK

NOTE
"DNP" means the component is not populated by default

REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

ATMEL ROUSSET
AT91SAM9M10-EKES
AT91SAM9G45-EKES
TOP LEVEL
SCALE 1/1
REV. E
SHEET 1/12


2.1 MM SOCKET
D2 5V
R2 100K
FORCE POWER ON
JP4
Q1
Si1563EDH
R4 10K
{3} SHDN
R5 10K
MN1 LT1765-3.3
C1 180nF
D1
L2 BAT20J 2.2uH
C2 2.2uF
C4 10uF
D3 STPS2L30A
C6 2.2nF
MN2 LT1765-1.8
C9 180nF
D4
L4 BAT20J 2.2uH
C10 2.2uF
C12 10uF
D5 STPS2L30A
C15 2.2nF
MN4 TPS60500
C16 1uF
C17 1uF
C18 2.2uF
C19 10pF
R6 68K
R8 220K
C22 22uF
R126 10K
3V3
5V
1V8
1V
1V VDDUTMIC
MN3 R1100D101C
L1 10uH 150mA
R1 1R
C3 100nF
C5 4.7uF
L3 10uH 150mA
R3 1R
C7 100nF
C8 4.7uF
C13 2.2uF
C14 2.2uF
L5 10uH 150mA
R7 1R
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C21 4.7uF
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J1-4
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VDDOSC {3}
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JP2
JP3
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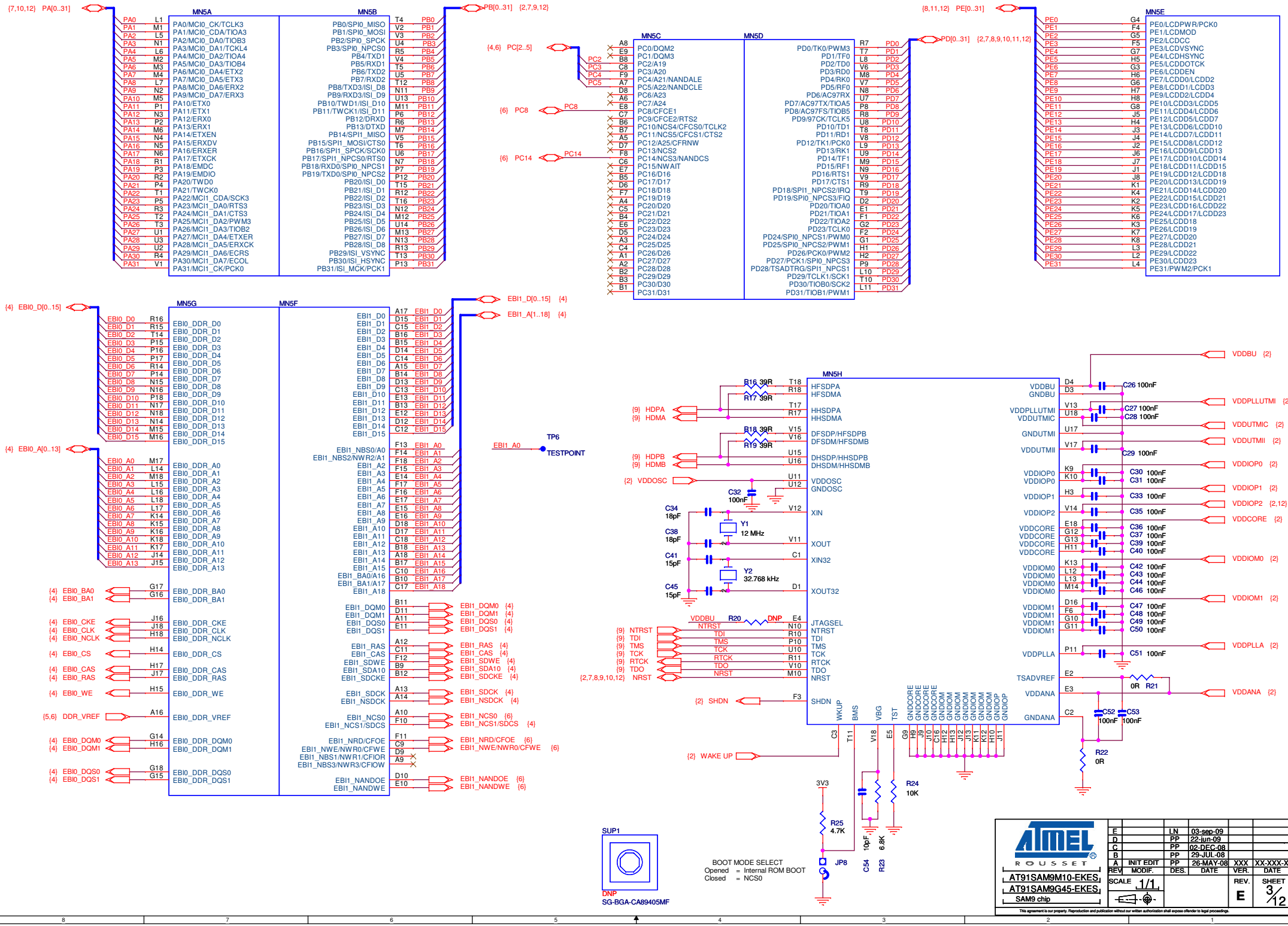
VDDIOP2 {3,12}
VDDISI {3,12}
VDDUTMIC {3}
VDDPLLUTMI {3}
VDDPLLA {3}
VDDCORE {3}
JP5
JP6
VDDIOM0 {3}
VDDIOM1 {3}
USER INTERFACE
D6 GREEN
D7 GREEN
R10 470R
R11 470R
PD0 {3}
PD31 {3}
R12 470R
D8 RED
R15 470K
Q2 IRLML2402
PD30 {3}
POWER LED
PB15
PB16
PB14
PB18
PB17
BP3
LEFT
PUSH
UP
RIGHT
DOWN
JOYSTICK
C215 10nF
C216 10nF
C217 10nF
C218 10nF
C219 10nF
R141 100R
{3} PB[14..18]
VDDBU
R13 100K
R14 1K
BP1
BP2
BP4
BP5
NRST
WAKE UP
RIGHT CLICK
LEFT CLICK
C220 10nF
R142 100R
C221 10nF
R143 100R
NRST {3,7,8,9,10,12}
WAKE UP {3}
PB7 {3}
PB6 {3}
ADHESIVE FEET
Z1
Z2
Z3
Z4
Z5
11.1
GND TEST POINT
TP1
TP2
TP3
TP4
J3
C25 100nF
JP7
VDDBU {3}
ATMEL ROUSSET
AT91SAM9M10-EKES
AT91SAM9G45-EKES
POWER SUPPLY
SCALE 1/1
REV. E
SHEET 2/12
E LN 03-sep-09
D PP 22-jun-09
C PP 02-DEC-08
B PP 29-JUL-08
A INIT EDIT PP 26-MAY-08 XXX XX-XXX-XX
REV. MODIF. DES. DATE VER. DATE


MN5A
MN5B
MN5C
MN5D
MN5E
MN5G
MN5F
MN5H
PA[0..31]
PB[0..31]
PC[2..5]
PC8
PC14
PD[0..31]
PE[0..31]
EBI0_D[0..15]
EBI0_A[0..13]
EBI1_D[0..15]
EBI1_A[1..18]
EBI1_A0
TP6
TESTPOINT
Y1
12 MHz
Y2
32.768 kHz
C32 100nF
C34 18pF
C38 18pF
C41 15pF
C45 15pF
R16 39R
R17 39R
R18 39R
R19 39R
R20 DNP
HDPA
HDMA
HDPB
HDMB
VDDOSC
NTRST
TDI
TMS
TCK
RTCK
TDO
NRST
SHDN
WAKE UP
VDDBU
VDDPLLUTMI
VDDUTMIC
VDDUTMII
VDDIOP0
VDDIOP1
VDDIOP2
VDDCORE
VDDIOM0
VDDIOM1
VDDPLLA
VDDANA
C26 100nF
C27 100nF
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C33 100nF
C35 100nF
C36 100nF
C37 100nF
C39 100nF
C40 100nF
C42 100nF
C43 100nF
C44 100nF
C46 100nF
C47 100nF
C48 100nF
C49 100nF
C50 100nF
C51 100nF
C52 100nF
C53 100nF
0R R21
R22 0R
R24 10K
R25 4.7K
C54 10pF
R23 6.8K
JP8
3V3
SUP1
DNP
SG-BGA-CA89405MF
BOOT MODE SELECT
Opened = Internal ROM BOOT
Closed = NCS0
ATMEL
ROUSSET
AT91SAM9M10-EKES
AT91SAM9G45-EKES
SAM9 chip
SCALE 1/1
REV. E
SHEET 3/12
E LN 03-sep-09
D PP 22-jun-09
C PP 02-DEC-08
B PP 29-JUL-08
A INIT EDIT PP 26-MAY-08 XXX XX-XXX-XX
REV. MODIF. DES. DATE VER. DATE
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EBI Bus Impedance Adaptor

EBI0

{3} EBI0_D[0..15] — DDR_D[0..15] {5}

EBI0_D0	2	RR4B	7	DDR_D0
EBI0_D1	4	RR2D	5	DDR_D1
EBI0_D2	2	RR2B	7	DDR_D2
EBI0_D3	1	RR4A	8	DDR_D3
EBI0_D4	3	RR4C	6	DDR_D4
EBI0_D5	4	RR4D	5	DDR_D5
EBI0_D6	1	RR2A	8	DDR_D6
EBI0_D7	3	RR2C	6	DDR_D7
EBI0_D8	2	RR6B	7	DDR_D8
EBI0_D9	4	RR8D	5	DDR_D9
EBI0_D10	4	RR6D	5	DDR_D10
EBI0_D11	2	RR8B	7	DDR_D11
EBI0_D12	1	RR8A	8	DDR_D12
EBI0_D13	3	RR6C	6	DDR_D13
EBI0_D14	1	RR6A	8	DDR_D14
EBI0_D15	3	RR8C	6	DDR_D15

{3} EBI0_A[0..13] — DDR_A[0..13] {5}

EBI0_A0	1	RR10A	8	DDR_A0
EBI0_A1	2	RR10B	7	DDR_A1
EBI0_A2	3	RR10C	6	DDR_A2
EBI0_A3	3	RR12C	6	DDR_A3
EBI0_A4	4	RR10D	5	DDR_A4
EBI0_A5	2	RR12B	7	DDR_A5
EBI0_A6	1	RR12A	8	DDR_A6
EBI0_A7	4	RR14D	5	DDR_A7
EBI0_A8	3	RR14C	6	DDR_A8
EBI0_A9	2	RR14B	7	DDR_A9
EBI0_A10	4	RR12D	5	DDR_A10
EBI0_A11	1	RR14A	8	DDR_A11
EBI0_A12	2	RR16B	7	DDR_A12
EBI0_A13	1	RR16A	8	DDR_A13
	3	RR26C	6	
	4	RR26D	5	

{3} EBI0_CKE	R26 27R		DDR_CKE {5}
{3} EBI0_CLK	R27 27R		DDR_CLK {5}
{3} EBI0_NCLK	R28 27R		DDR_NCLK {5}
{3} EBI0_BA0	4 RR16D 5		DDR_BA0 {5}
{3} EBI0_BA1	1 RR26A 8		DDR_BA1 {5}
{3} EBI0_WE	3 RR16C 6		DDR_WE {5}
{3} EBI0_CS	2 RR26B 7		DDR_CS {5}
{3} EBI0_RAS	3 RR29C 6		DDR_RAS {5}
{3} EBI0_CAS	4 RR29D 5		DDR_CAS {5}
{3} EBI0_DQM0	1 RR29A 8		DDR_DQM0 {5}
{3} EBI0_DQM1	2 RR29B 7		DDR_DQM1 {5}
{3} EBI0_DQS0	R32 27R		DDR_DQS0 {5}
{3} EBI0_DQS1	R33 27R		DDR_DQS1 {5}

{3} EBI1_D[0..15]

EBI1_D0	1	RR9A	8	EBI1_FLASH_D0
	2	RR9B	7	EBI1_NAND_FSH_D0
EBI1_D1	1	RR11A	8	EBI1_FLASH_D1
	2	RR11B	7	EBI1_NAND_FSH_D1
EBI1_D2	4	RR11D	5	EBI1_FLASH_D2
	3	RR11C	6	EBI1_NAND_FSH_D2
EBI1_D3	3	RR9C	6	EBI1_FLASH_D3
	4	RR9D	5	EBI1_NAND_FSH_D3
EBI1_D4	1	RR13A	8	EBI1_FLASH_D4
	2	RR13B	7	EBI1_NAND_FSH_D4
EBI1_D5	3	RR13C	6	EBI1_FLASH_D5
	4	RR13D	5	EBI1_NAND_FSH_D5
EBI1_D6	1	RR17A	8	EBI1_FLASH_D6
	2	RR17B	7	EBI1_NAND_FSH_D6
EBI1_D7	3	RR17C	6	EBI1_FLASH_D7
	4	RR17D	5	EBI1_NAND_FSH_D7
EBI1_D8	4	RR19D	5	EBI1_FLASH_D8
	3	RR19C	6	EBI1_NAND_FSH_D8
EBI1_D9	2	RR21B	7	EBI1_FLASH_D9
	1	RR21A	8	EBI1_NAND_FSH_D9
EBI1_D10	3	RR25C	6	EBI1_FLASH_D10
	4	RR25D	5	EBI1_NAND_FSH_D10
EBI1_D11	2	RR23B	7	EBI1_FLASH_D11
	1	RR23A	8	EBI1_NAND_FSH_D11
EBI1_D12	1	RR25A	8	EBI1_FLASH_D12
	2	RR25B	7	EBI1_NAND_FSH_D12
EBI1_D13	3	RR23C	6	EBI1_FLASH_D13
	4	RR23D	5	EBI1_NAND_FSH_D13
EBI1_D14	4	RR21D	5	EBI1_FLASH_D14
	3	RR21C	6	EBI1_NAND_FSH_D14
EBI1_D15	2	RR19B	7	EBI1_FLASH_D15
	1	RR19A	8	EBI1_NAND_FSH_D15

EBI1_FLASH_D[0..15] {6}

EBI1_D0	4	RR1D	5	EBI1_DDR_D0
EBI1_D1	1	RR1A	8	EBI1_DDR_D1
EBI1_D2	2	RR1B	7	EBI1_DDR_D2
EBI1_D3	3	RR1C	6	EBI1_DDR_D3
EBI1_D4	2	RR3B	7	EBI1_DDR_D4
EBI1_D5	1	RR3A	8	EBI1_DDR_D5
EBI1_D6	4	RR3D	5	EBI1_DDR_D6
EBI1_D7	3	RR3C	6	EBI1_DDR_D7
EBI1_D8	3	RR5C	6	EBI1_DDR_D8
EBI1_D9	1	RR7A	8	EBI1_DDR_D9
EBI1_D10	2	RR5B	7	EBI1_DDR_D10
EBI1_D11	4	RR7D	5	EBI1_DDR_D11
EBI1_D12	1	RR5A	8	EBI1_DDR_D12
EBI1_D13	3	RR7C	6	EBI1_DDR_D13
EBI1_D14	2	RR7B	7	EBI1_DDR_D14
EBI1_D15	4	RR5D	5	EBI1_DDR_D15

EBI1_DDR_D[0..15] {6}
EBI1_NAND_FSH_D[0..15] {6}

EBI1_NAND_FSH_D0
EBI1_NAND_FSH_D1
EBI1_NAND_FSH_D2
EBI1_NAND_FSH_D3
EBI1_NAND_FSH_D4
EBI1_NAND_FSH_D5
EBI1_NAND_FSH_D6
EBI1_NAND_FSH_D7
EBI1_NAND_FSH_D8
EBI1_NAND_FSH_D9
EBI1_NAND_FSH_D10
EBI1_NAND_FSH_D11
EBI1_NAND_FSH_D12
EBI1_NAND_FSH_D13
EBI1_NAND_FSH_D14
EBI1_NAND_FSH_D15

EBI1_FLASH_A[1..21] {6}

EBI1_FLASH_A1
EBI1_FLASH_A2
EBI1_FLASH_A3
EBI1_FLASH_A4
EBI1_FLASH_A5
EBI1_FLASH_A6
EBI1_FLASH_A7
EBI1_FLASH_A8
EBI1_FLASH_A9
EBI1_FLASH_A10
EBI1_FLASH_A11
EBI1_FLASH_A12
EBI1_FLASH_A13
EBI1_FLASH_A14
EBI1_FLASH_A15
EBI1_FLASH_A16
EBI1_FLASH_A17
EBI1_FLASH_A18
EBI1_FLASH_A19
EBI1_FLASH_A20
EBI1_FLASH_A21

EBI1

EBI1_DDR_A[2..15] {6}

EBI1_A1	2	RR30B	7	
	3	RR30C	6	EBI1_FLASH_A1
EBI1_A2	4	RR18D	5	EBI1_DDR_A2
	1	RR18A	8	EBI1_FLASH_A2
EBI1_A3	2	RR28B	7	EBI1_DDR_A3
	3	RR28C	6	EBI1_FLASH_A3
EBI1_A4	4	RR30D	5	EBI1_DDR_A4
	1	RR15A	8	EBI1_FLASH_A4
EBI1_A5	2	RR18B	7	EBI1_DDR_A5
	3	RR18C	6	EBI1_FLASH_A5
EBI1_A6	2	RR20B	7	EBI1_DDR_A6
	1	RR20A	8	EBI1_FLASH_A6
EBI1_A7	1	RR22A	8	EBI1_DDR_A7
	2	RR22B	7	EBI1_FLASH_A7
EBI1_A8	1	RR30A	8	EBI1_DDR_A8
	4	RR28D	5	EBI1_FLASH_A8
EBI1_A9	4	RR24D	5	EBI1_DDR_A9
	1	RR28A	8	EBI1_FLASH_A9
EBI1_A10	3	RR20C	6	EBI1_DDR_A10
	4	RR20D	5	EBI1_FLASH_A10
EBI1_A11	1	RR27A	8	EBI1_DDR_A11
	2	RR27B	7	EBI1_FLASH_A11
SDA10	3	RR22C	6	EBI1_DDR_A12 (SDA10)
EBI1_A12	4	RR22D	5	EBI1_FLASH_A12
EBI1_A13	4	RR27D	5	EBI1_DDR_A13
	3	RR27C	6	EBI1_FLASH_A13
EBI1_A14	3	RR15C	6	EBI1_DDR_A14
	2	RR24B	7	EBI1_FLASH_A14
EBI1_A15	4	RR15D	5	EBI1_DDR_A15
	3	RR24C	6	EBI1_FLASH_A15
EBI1_A16	2	RR31B	7	EBI1_FLASH_A16
EBI1_A17	4	RR31D	5	EBI1_FLASH_A17
EBI1_A18	1	RR24A	8	EBI1_FLASH_A18
{3} PC2	(A19)	2	RR32B	7 EBI1_FLASH_A19
{3} PC3	(A20)	3	RR32C	6 EBI1_FLASH_A20
{3,6} PC4	(A21)	4	RR32D	5 EBI1_FLASH_A21

{3} EBI1_A[1..18]

{3} EBI1_SDCKE	R29 27R		CKE_EBI1 {6}
{3} EBI1_SDCK	R30 27R		CLK_EBI1 {6}
{3} EBI1_NSDCK	R31 27R		NCLK_EBI1 {6}
EBI1_A16	1 RR31A 8		BA0_EBI1 {6}
EBI1_A17	3 RR31C 6		BA1_EBI1 {6}
{3} EBI1_NCS1/SDCS	2 RR33B 7		CS_EBI1 {6}
{3} EBI1_SDWE	1 RR33A 8		WE_EBI1 {6}
{3} EBI1_RAS	2 RR15B 7		RAS_EBI1 {6}
{3} EBI1_CAS	3 RR33C 6		CAS_EBI1 {6}
{3} EBI1_DQM0	4 RR33D 5		DQM0_EBI1 {6}
{3} EBI1_DQM1	1 RR32A 8		DQM1_EBI1 {6}
{3} EBI1_DQS0	R34 27R		DQS0_EBI1 {6}
{3} EBI1_DQS1	R35 27R		DQS1_EBI1 {6}
{3} EBI1_SDA10	SDA10		

CAUTION
Pin assignemts at PCB layout time

REV	MODIF.	DES.	DATE	VER.	DATE
E			LN	03-sep-09	
D			PP	22-jun-09	
C			PP	02-DEC-08	
B			PP	29-JUL-08	
A	INIT EDIT		PP	26-MAY-08	XXX XX-XXX-XX

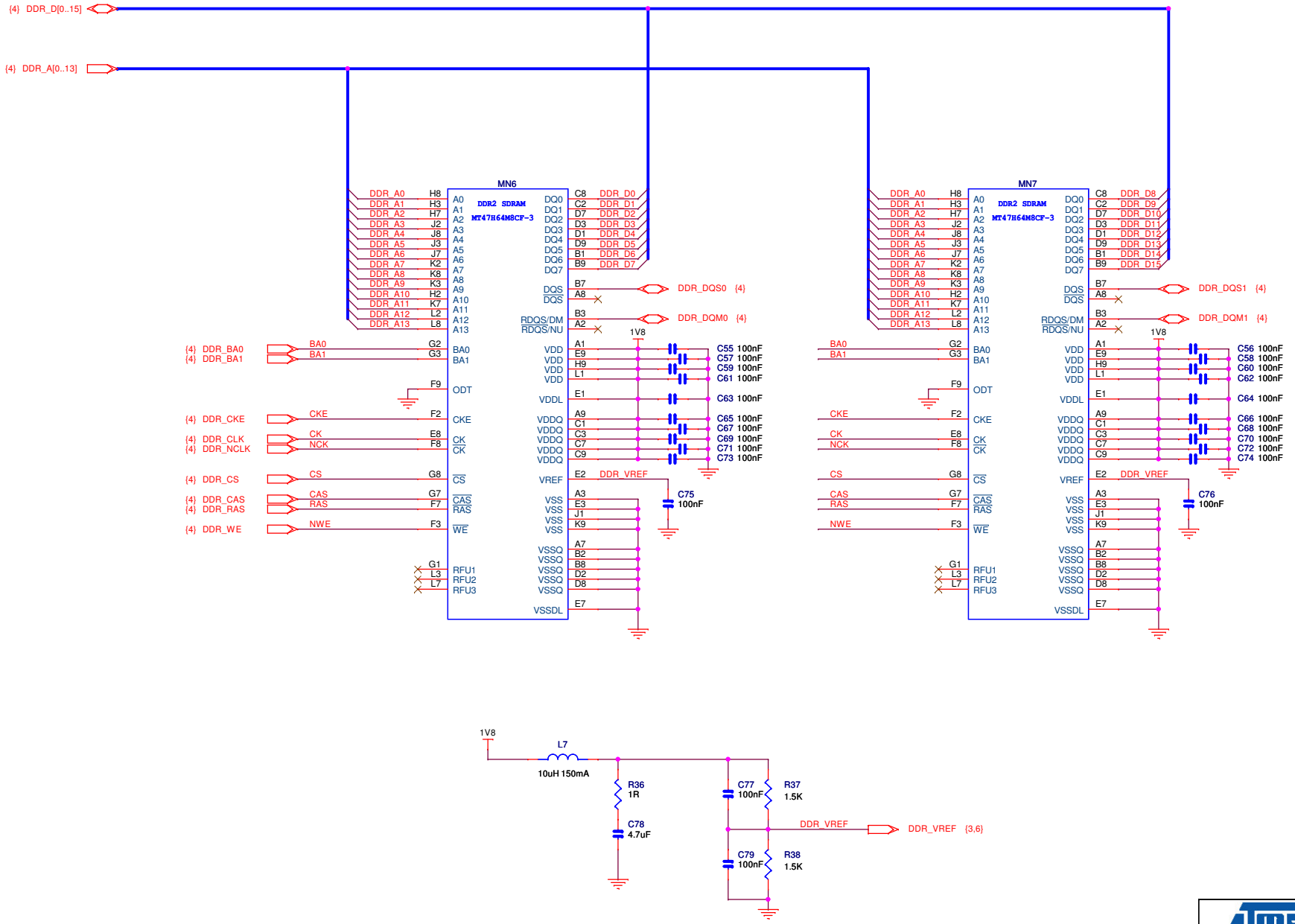
ATMEL ROUSSET

AT91SAM9M10-EKES
AT91SAM9G45-EKES
RES.ARRAYS-EBI0_EBI1

SCALE 1/1

REV. E

SHEET 4/12



REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

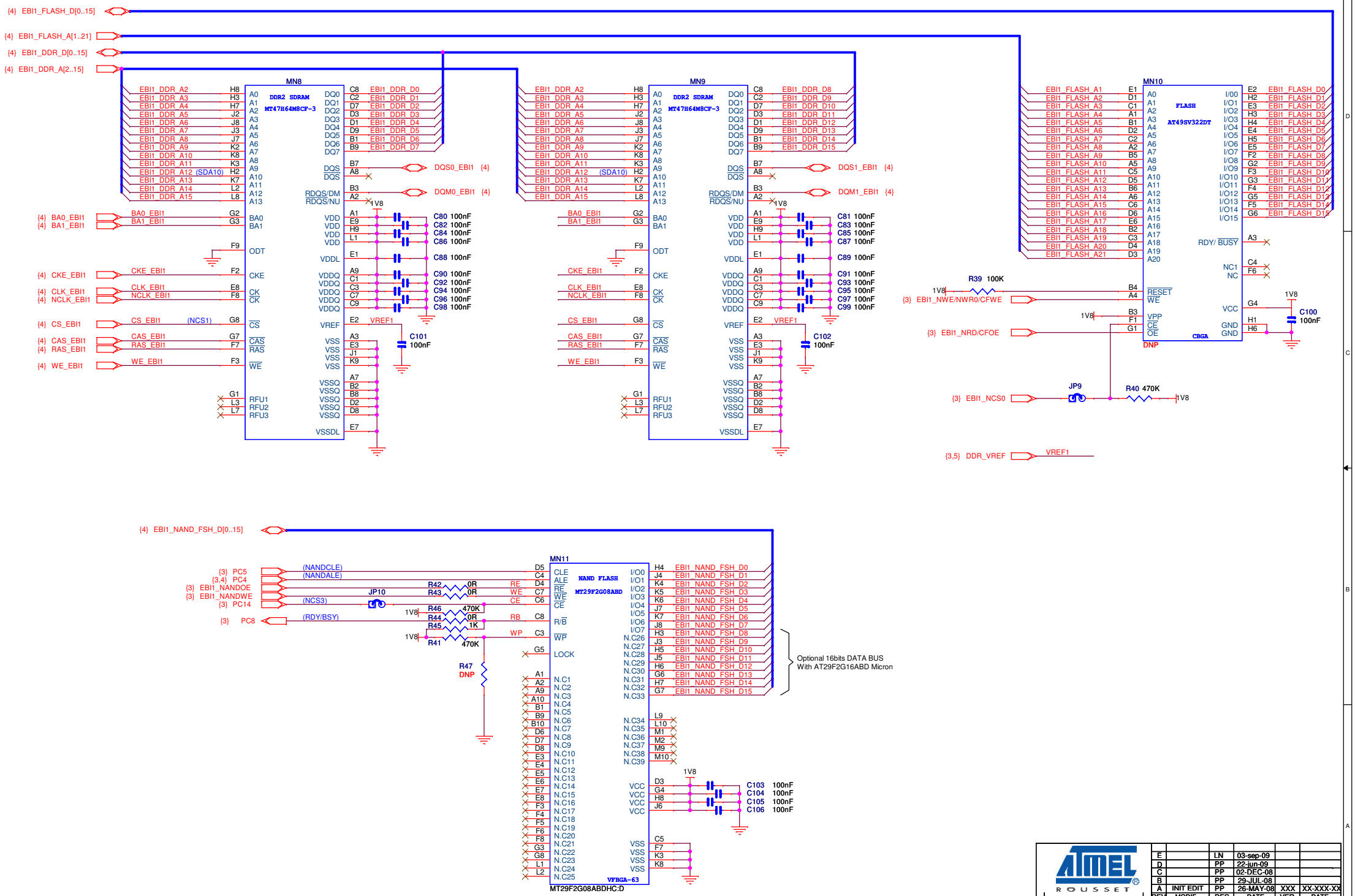
ATMEL ROUSSET

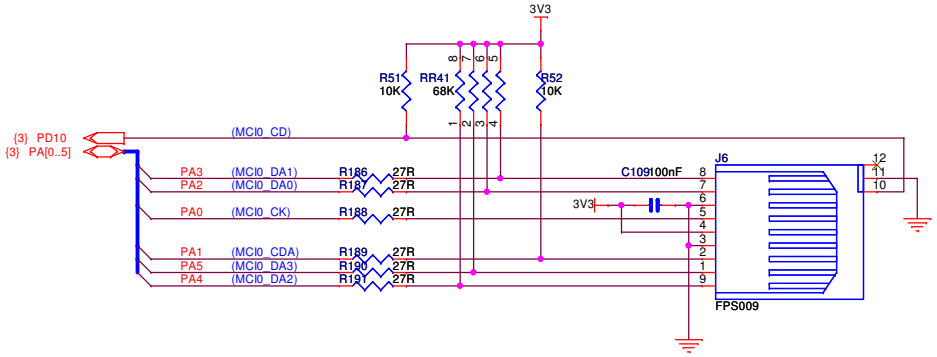
AT91SAM9M10-EKES
AT91SAM9G45-EKES
EBI0_DDR2

SCALE 1/1

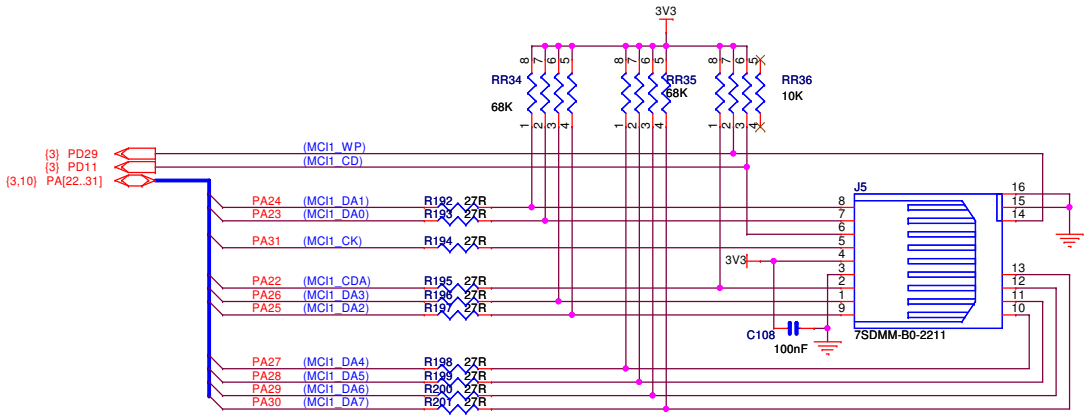
REV. E

SHEET 5/12

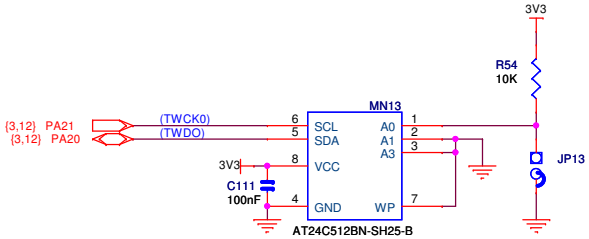

{4} EBI1_FLASH_D[0..15]
{4} EBI1_FLASH_A[1..21]
{4} EBI1_DDR_D[0..15]
{4} EBI1_DDR_A[2..15]
MN8
DDR2 SDRAM
MT47H64M8CF-3
MN9
DDR2 SDRAM
MT47H64M8CF-3
MN10
FLASH
AT49SV322DT
CBGA
DNP
R39 100K
JP9
R40 470K
{3} EBI1_NWE/NWR0/CFWE
{3} EBI1_NRD/CFOE
{3} EBI1_NCS0
{3,5} DDR_VREF
VREF1
{4} EBI1_NAND_FSH_D[0..15]
MN11
NAND FLASH
MT29F2G08ABD
VFBGA-63
MT29F2G08ABDHC:D
JP10
R41 470K
R42 0R
R43 0R
R44 0R
R45 1K
R46 470K
R47 DNP
Optional 16bits DATA BUS
With AT29F2G16ABD Micron
AT91SAM9M10-EKES
AT91SAM9G45-EKES
EBI1_MEMORY
REV. E
SHEET 6/12



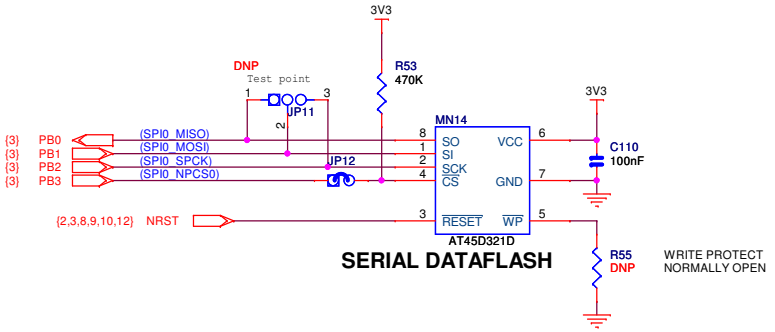
SD/MMC CARD INTERFACE - MCI0



SD/MMCPlus CARD INTERFACE - MCI1



SERIAL EEPROM



SERIAL DATAFLASH

REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

AT91SAM9M10-EKES
AT91SAM9G45-EKES
MCI & TWI

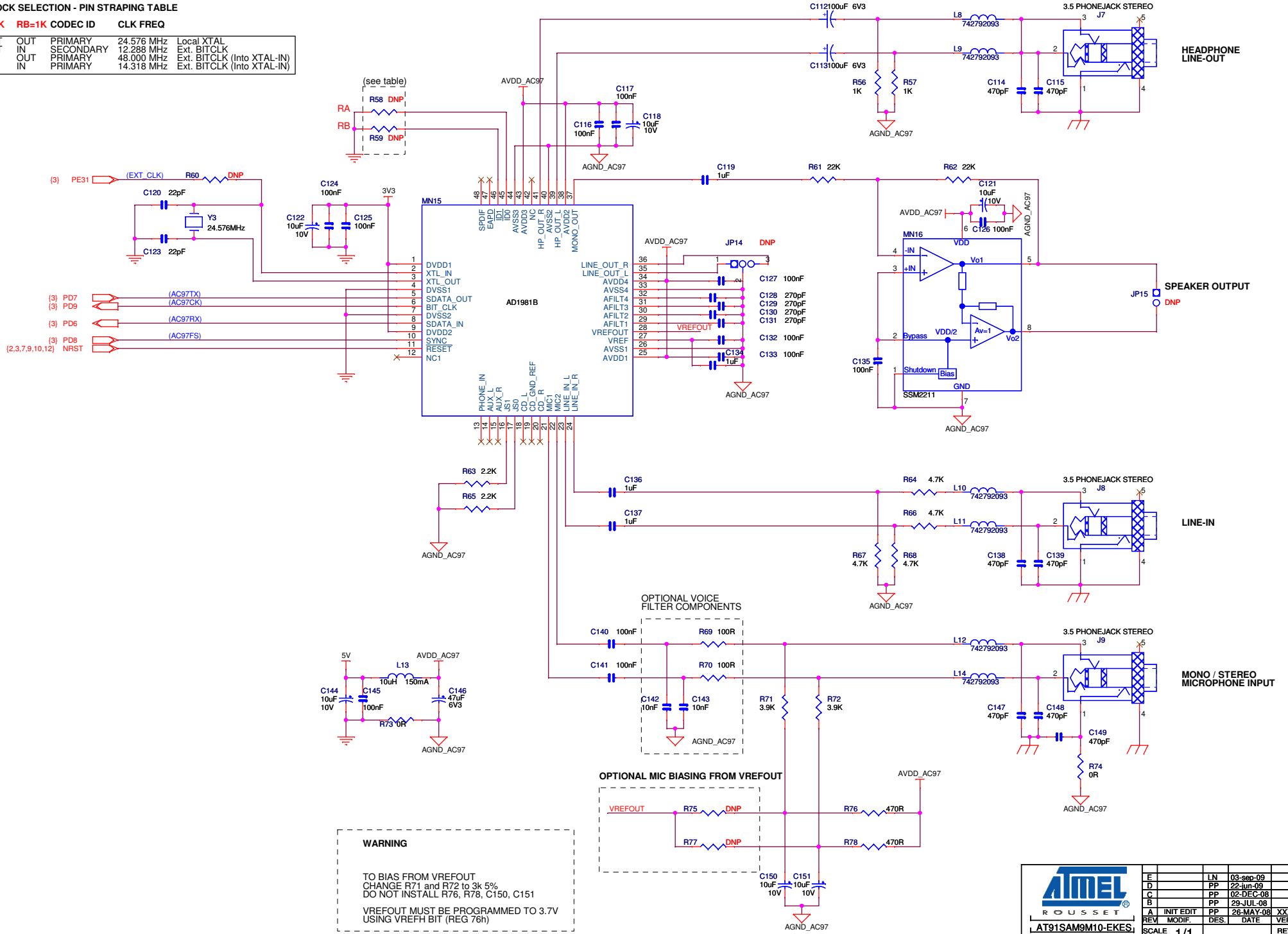
SCALE 1/1

REV. E

SHEET 7/12

CLOCK SELECTION - PIN STRAPING TABLE

RA=1K	RB=1K	CODEC ID	CLK FREQ	
OUT	OUT	PRIMARY	24.576 MHz	Local XTAL
OUT	IN	SECONDARY	12.288 MHz	Ext. BITCLK
IN	OUT	PRIMARY	48.000 MHz	Ext. BITCLK (Into XTAL-IN)
IN	IN	PRIMARY	14.318 MHz	Ext. BITCLK (Into XTAL-IN)



REV.	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

ATMEL ROUSSET

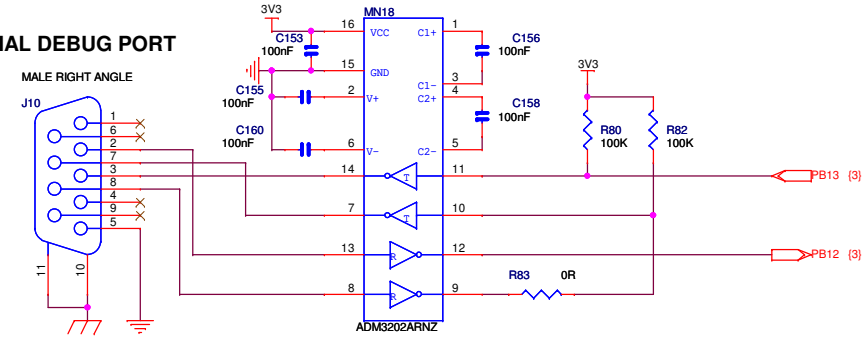
AT91SAM9M10-EKES
AT91SAM9G45-EKES
AUDIO AC97

SCALE 1/1

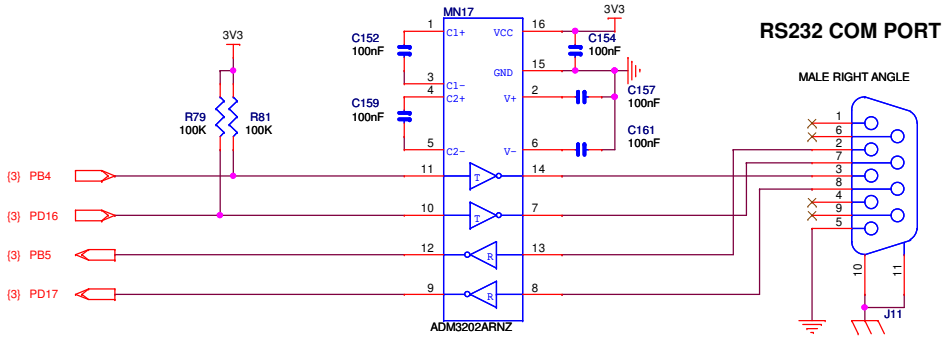
REV. E

SHEET 8/12

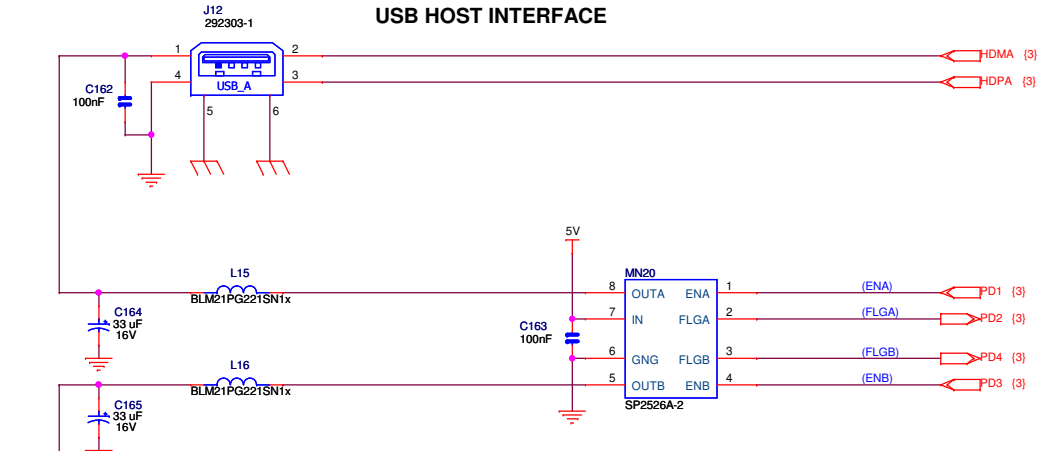
SERIAL DEBUG PORT



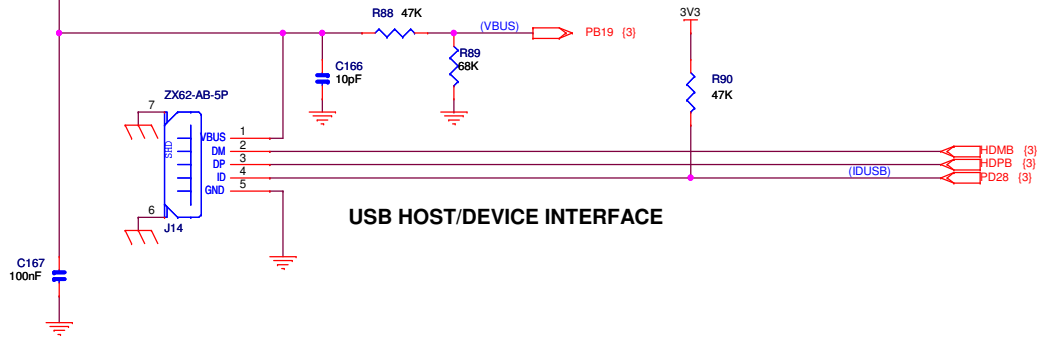
RS232 COM PORT



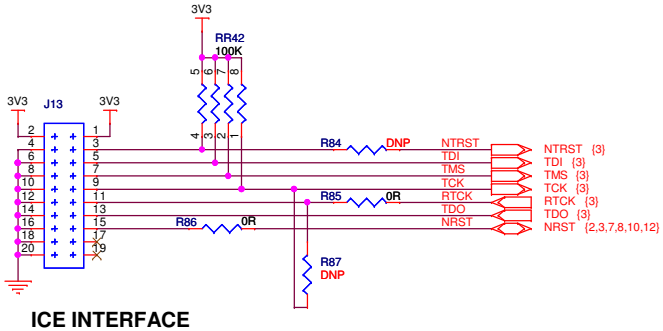
USB HOST INTERFACE



USB HOST/DEVICE INTERFACE



ICE INTERFACE



Take note of layout directive
"High speed USB platform design.PDF"

REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-Jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

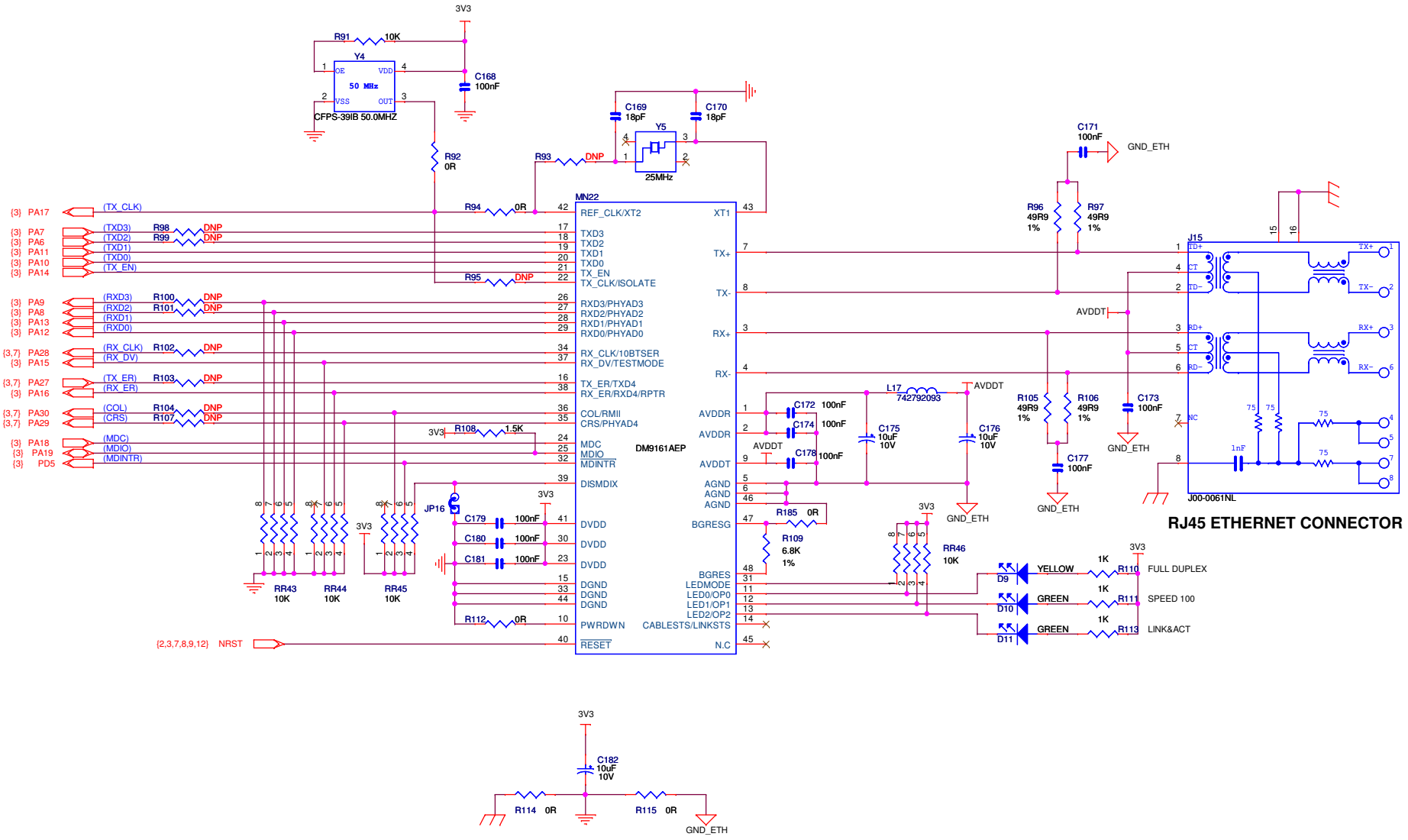
ATMEL ROUSSET

AT91SAM9M10-EKES
AT91SAM9G45-EKES
SERIAL INTERFACES

SCALE 1/1

REV. E

SHEET 9/12



RJ45 ETHERNET CONNECTOR

Take note of layout directive "DM9161-LG-V11-011401S.PDF"

REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

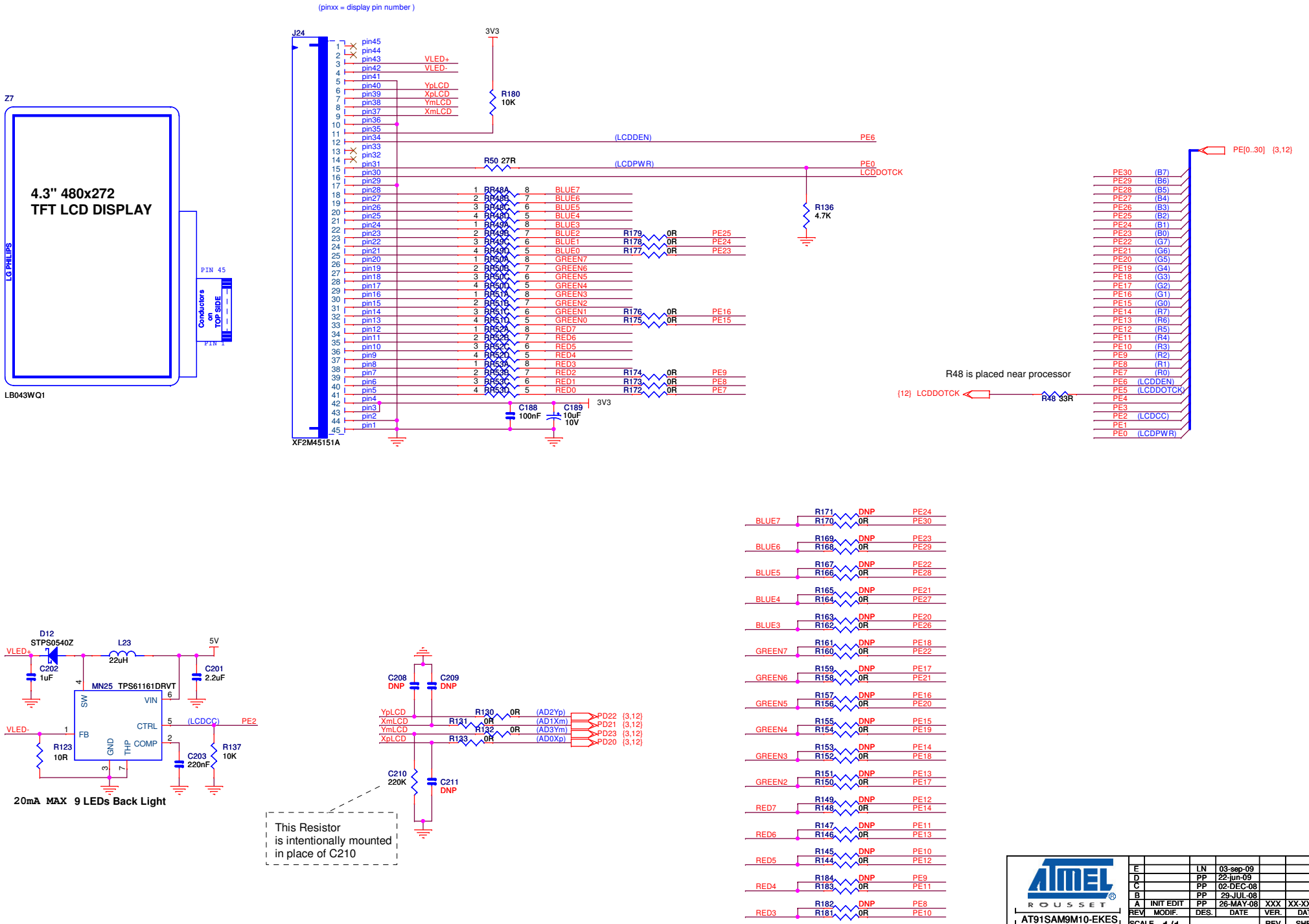
ATMEL ROUSSET

AT91SAM9M10-EKES
AT91SAM9G45-EKES
RMII ETHERNET

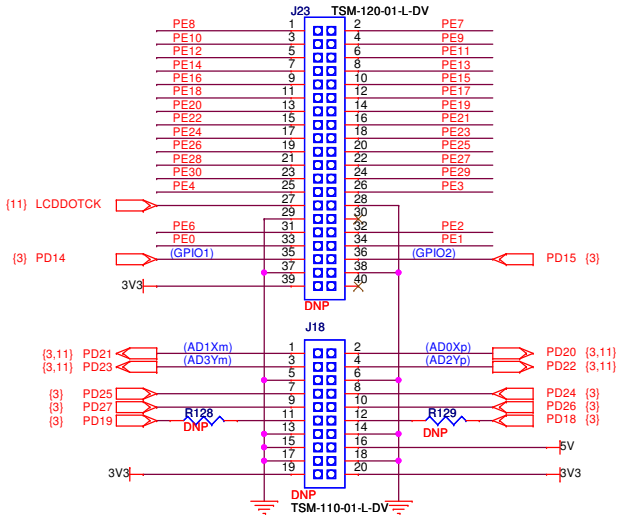
SCALE 1/1

REV. E

SHEET 10/12


(pinxx = display pin number)
Z7
4.3" 480x272
TFT LCD DISPLAY
LG PHILIPS
PIN 45
Conductors on TOP SIDE
PIN 1
LB043WQ1
J24
XF2M45151A
3V3
R180
10K
VLED+
VLED-
YpLCD
XpLCD
YmLCD
XmLCD
(LCDDEN)
PE6
R50 27R
(LCDPWR)
PE0
LCDDOTCK
R136
4.7K
BLUE7
BLUE6
BLUE5
BLUE4
BLUE3
GREEN7
GREEN6
GREEN5
GREEN4
GREEN3
GREEN2
GREEN1
GREEN0
RED7
RED6
RED5
RED4
RED3
RED2
RED1
RED0
R179 0R PE25
R178 0R PE24
R177 0R PE23
R176 0R PE16
R175 0R PE15
R174 0R PE9
R173 0R PE8
R172 0R PE7
C188
100nF
C189
10uF
10V
PE[0..30] {3,12}
PE30 (B7)
PE29 (B6)
PE28 (B5)
PE27 (B4)
PE26 (B3)
PE25 (B2)
PE24 (B1)
PE23 (B0)
PE22 (G7)
PE21 (G6)
PE20 (G5)
PE19 (G4)
PE18 (G3)
PE17 (G2)
PE16 (G1)
PE15 (G0)
PE14 (R7)
PE13 (R6)
PE12 (R5)
PE11 (R4)
PE10 (R3)
PE9 (R2)
PE8 (R1)
PE7 (R0)
PE6 (LCDDEN)
PE5 (LCDDOTCK)
PE4
PE3
PE2 (LCDCC)
PE1
PE0 (LCDPWR)
R48 is placed near processor
{12} LCDDOTCK
R48 33R
D12
STPS0540Z
L23
22uH
5V
C202
1uF
C201
2.2uF
MN25 TPS61161DRVT
SW
VIN
CTRL
FB
GND
THP
COMP
VLED-
R123
10R
C203
220nF
R137
10K
(LCDCC)
PE2
20mA MAX 9 LEDs Back Light
C208
DNP
C209
DNP
YpLCD
XmLCD
YmLCD
XpLCD
R130 0R (AD2Yp)
R131 0R (AD1Xm)
R132 0R (AD3Ym)
R133 0R (AD0Xp)
PD22 {3,12}
PD21 {3,12}
PD23 {3,12}
PD20 {3,12}
C210
220K
C211
DNP
This Resistor
is intentionally mounted
in place of C210
R171 DNP PE24
R170 0R PE30
R169 DNP PE23
R168 0R PE29
R167 DNP PE22
R166 0R PE28
R165 DNP PE21
R164 0R PE27
R163 DNP PE20
R162 0R PE26
R161 DNP PE18
R160 0R PE22
R159 DNP PE17
R158 0R PE21
R157 DNP PE16
R156 0R PE20
R155 DNP PE15
R154 0R PE19
R153 DNP PE14
R152 0R PE18
R151 DNP PE13
R150 0R PE17
R149 DNP PE12
R148 0R PE14
R147 DNP PE11
R146 0R PE13
R145 DNP PE10
R144 0R PE12
R184 DNP PE9
R183 0R PE11
R182 DNP PE8
R181 0R PE10
ATMEL
ROUSSET
AT91SAM9M10-EKES
AT91SAM9G45-EKES
LCD & ISI & VIDEO INTERFACE
E LN 03-sep-09
D PP 22-jun-09
C PP 02-DEC-08
B PP 29-JUL-08
A INIT EDIT PP 26-MAY-08 XXX XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. E
SHEET 11/12

CONNECTOR EXTENTION FOR LARGE LCD



{3,11} PE[0..30]

PE30 (B7)
PE29 (B6)
PE28 (B5)
PE27 (B4)
PE26 (B3)
PE25 (B2)
PE24 (B1)
PE23 (B0)
PE22 (G7)
PE21 (G6)
PE20 (G5)
PE19 (G4)
PE18 (G3)
PE17 (G2)
PE16 (G1)
PE15 (G0)
PE14 (R7)
PE13 (R6)
PE12 (R5)
PE11 (R4)
PE10 (R3)
PE9 (R2)
PE8 (R1)
PE7 (R0)
PE6 (LCDDEN)
PE5 (LCDDOTCK)
PE4 (HSYNC)
PE3 (VSYNC)
PE2 (LCDCC)
PE1 (LCDMOD)
PE0 (LCDPWR)

MN23

PE23 42 D0
PE24 43 D1
PE25 44 D2
PE26 45 D3
PE27 46 D4
PE28 47 D5
PE29 48 D6
PE30 1 D7
PE15 2 D8
PE16 3 D9
PE17 4 D10
PE18 5 D11
PE19 6 D12
PE20 7 D13
PE21 8 D14
PE22 9 D15
PE7 10 D16
PE8 11 D17
PE9 12 D18
PE10 13 D19
PE11 14 D20
PE12 15 D21
PE13 17 D22
PE14 19 D23

PE3 39 V
PE4 40 H
41 XCLK
PE6 20 DE

23 RESET
24 NC
XI/FIN
XO

VDDIO 38
DVDD 16
DGND 18
AVDD_PLL 32
AGND_PLL 31
AVDD 33
AGND 36
AVDD_DAC 25
AGND_DAC 29
ISET 30
CVBS 28
Y 27
C/CVBS 26
P-OUT 37

L18 742792093
L19 742792093
L20 742792093
L21 742792093
L22 742792093
L24 1.8uH

C190 100nF
C191 100nF
C192 10uF 10V
C193 10uF 10V
C194 100nF
C195 100nF
C196 10uF 10V
C197 100nF
C198 33pF
C199 100pF
C200 270pF

R116 1.2K 1%
R119 75R
R120 75R
R121 75R

3V3
1V8

R49 is placed near processor
PE5
R49 33R
PE6

3V3
R117 4.7K
R118 4.7K
{3,7} PA20 (TWDO)
{3,7} PA21 (TWCK0)
21 SPD
22 SPC
{2,3,7,8,9,10} NRST

R122 DNP
Y6
1 OE
VDD 4
13 MHz
2 VSS
OUT 3
SG-8002JC-13.0000M-PCB
DNP
C205 DNP
R124 DNP

34
R125 0R
35
CH7024B-DF-TR
TP5

Y7
4
3
1
2
13MHz
C207 10pF
C206 10pF

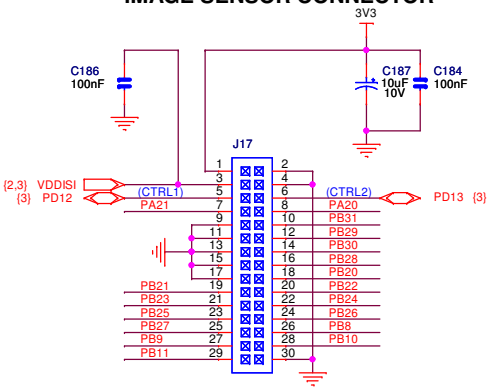
D13 BAT54SLT1G
J20
Composite Video Output

The frequency accuracy must be +-20ppm or higher.

{3} PB[8..11]
PB8 (ISI_D8)
PB9 (ISI_D09)
PB10 (ISI_D10)
PB11 (ISI_D11)

{3} PB[20..31]
PB20 (ISI_D0)
PB21 (ISI_D1)
PB22 (ISI_D2)
PB23 (ISI_D3)
PB24 (ISI_D4)
PB25 (ISI_D5)
PB26 (ISI_D6)
PB27 (ISI_D7)
PB28 (ISI_PCK)
PB29 (ISI_VSYNC)
PB30 (ISI_HSYNC)
PB31 (ISI_MCK)

IMAGE SENSOR CONNECTOR



REV	MODIF.	DES.	DATE	VER.	DATE
E		LN	03-sep-09		
D		PP	22-jun-09		
C		PP	02-DEC-08		
B		PP	29-JUL-08		
A	INIT EDIT	PP	26-MAY-08	XXX	XX-XXX-XX

ATMEL ROUSSET

AT91SAM9M10-EKES
AT91SAM9G45-EKES
LCD & ISI & VIDEO INTERFACE

SCALE 1/1

REV. E

SHEET 12/12

Section 8

Revision History

8.1 Revision History

Table 8-1.

Document	Comments	Change Request Ref.
6481A	First issue.	
6481B	Figure 4-17, " TFT LCD" updated. Section 7.1 "Schematics" updated.	6833

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