Z90233, Z90234, and Z90231
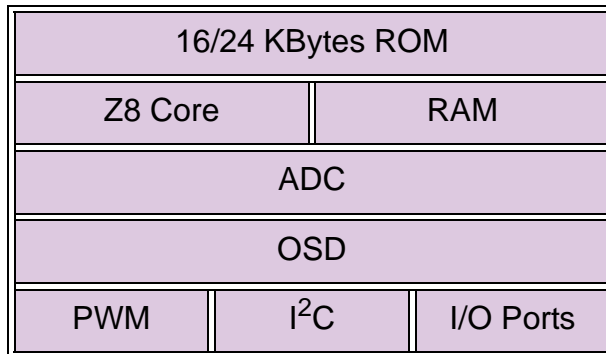
eZVision 200 Television Controller with On-Screen Display

Product Brief

Product Block Diagram

| 16/24 KBytes ROM |
| Z8 Core | RAM |
| ADC |
| OSD |
| PWM | I²C | I/O Ports |

On-Screen Display (OSD) Features

- Displays of up to 10 rows by 24 columns with 256 characters

- Provides character cell resolution of 14 pixels by 18 scan lines

- Offers variable inter-row spacing from 0–15 horizontal scan lines

- Uses color palette table to program foreground and background of character

Microcontroller Features

- Incorporates Z8® MCU core at 6 MHz

- Z90233 and Z90234 have 16K and 24K masked ROM, respectively

- 236 bytes of system RAM

- Ten 6-bit pulse width modulators

- One 14-bit pulse width modulator

- On-chip infrared (IR) capture registers

- Four channels of 4-bit analog-to-digital converter

- 27 general-purpose I/O pins

- Provides I^2C master serial communication port

- 42-pin SDIP and 44-pin PQFP packages

- Can be emulated with 124-pin PGA package (Z90239)

General Description

The Z90233/Z90234 and Z90231 are the ROM and OTP versions of the eZVision 200 television controller with OSD. Based on ZiLOG's powerful Z8 architecture, the Z90233/Z90234 and Z90231 contain 24 KB of program memory. The following enhanced features are included:

- Flexible inter-row spacing

- Higher character cell resolution (14 x 18)

- Background mesh effect

- Dedicated infrared capture registers

- On-chip analog-to-digital converter

- Hardware master mode I^2C interface

The familiar Z8 architecture, in combination with these advanced features, makes the eZVision 200 an ideal choice for midrange televisions in both PAL and NTSC markets.

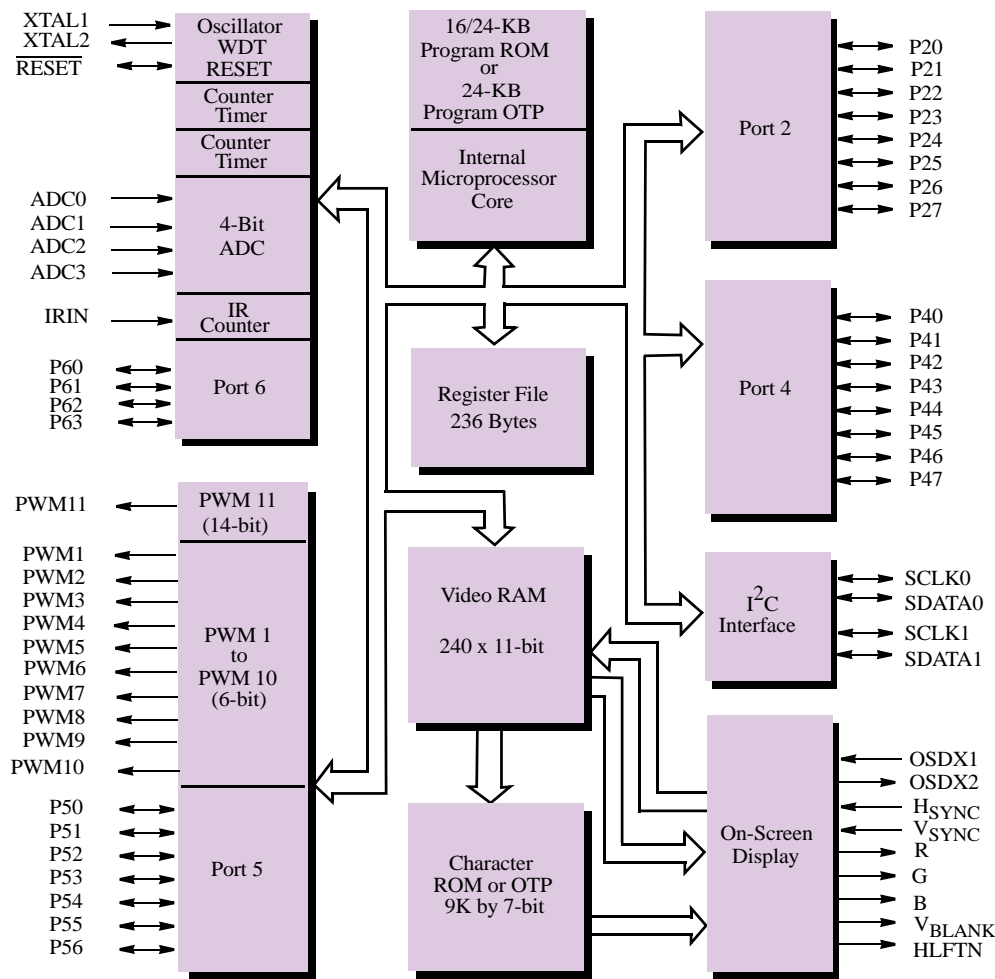The eZVision 200 family consists of three basic device types:

- The Z90233 and Z90234 masked ROM

- The Z90231 OTP

- The Z90239 In-Circuit Emulator (ICE) chip

The OTP supports a field-programmable 24 KB program ROM. The ICE chip is used in the Z90239

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emulator and protopak. The Z90233/Z90234 masked ROM supports a 16/32-KB system ROM (selectable through a mask option).

The eZVision 200 family takes full advantage of the Z8 microcontroller's expanded register file space to offer greater flexibility in OSD creations that simulate bitmap graphics, icons, and animation.

Block Diagram of eZVision 200

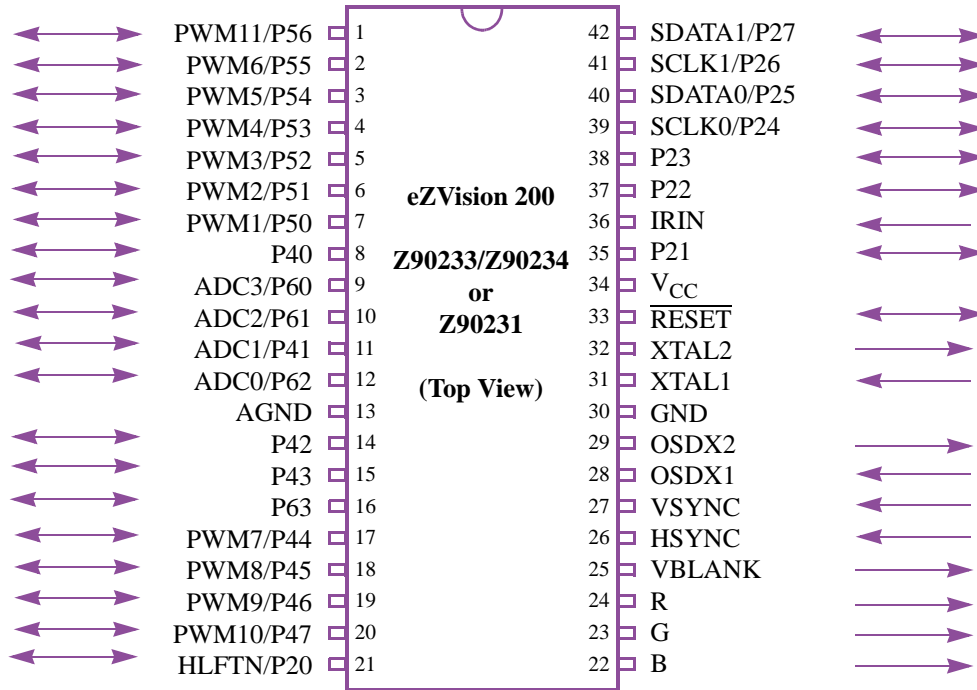| Input	Block	Block	Block	Output
XTAL1, XTAL2, $\overline{RESET}$	Oscillator WDT RESET			
	Counter Timer			
	Counter Timer	16/24-KB Program ROM or 24-KB Program OTP	Port 2	P20, P21, P22, P23, P24, P25, P26, P27
ADC0, ADC1, ADC2, ADC3	4-Bit ADC	Internal Microprocessor Core		
IRIN	IR Counter		Port 4	P40, P41, P42, P43, P44, P45, P46, P47
P60, P61, P62, P63	Port 6	Register File 236 Bytes		
PWM11	PWM 11 (14-bit)		I^2C Interface	SCLK0, SDATA0, SCLK1, SDATA1
PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8, PWM9, PWM10	PWM 1 to PWM 10 (6-bit)	Video RAM 240 x 11-bit		
P50, P51, P52, P53, P54, P55, P56	Port 5	Character ROM or OTP 9K by 7-bit	On-Screen Display	OSDX1, OSDX2, H_{SYNC}, V_{SYNC}, R, G, B, V_{BLANK}, HLFTN

PB006903-0903

Pin-Outs and Pin Direction

PWM11/P56	1	42 SDATA1/P27
PWM6/P55	2	41 SCLK1/P26
PWM5/P54	3	40 SDATA0/P25
PWM4/P53	4	39 SCLK0/P24
PWM3/P52	5	38 P23
PWM2/P51	6	37 P22
PWM1/P50	7	36 IRIN
P40	8	35 P21
ADC3/P60	9	34 V$_{CC}$
ADC2/P61	10	33 $\overline{RESET}$
ADC1/P41	11	32 XTAL2
ADC0/P62	12	31 XTAL1
AGND	13	30 GND
P42	14	29 OSDX2
P43	15	28 OSDX1
P63	16	27 VSYNC
PWM7/P44	17	26 HSYNC
PWM8/P45	18	25 VBLANK
PWM9/P46	19	24 R
PWM10/P47	20	23 G
HLFTN/P20	21	22 B

eZVision 200

Z90233/Z90234
or
Z90231

(Top View)

Figure 1.   42-Pin Shrink DIP
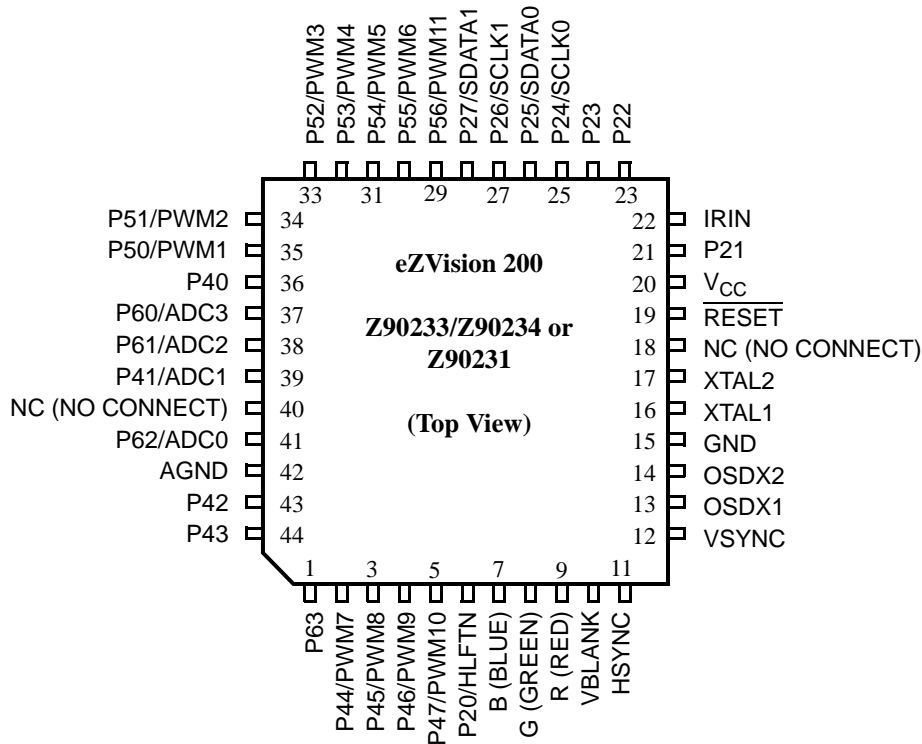
Figure 2.   44-Pin Plastic Quad Flatpack (PQFP)

Table 1   Pin Descriptions for the Z90233, Z90234, and Z90231

Name	42-Pin SDIP Pin Number	44-Pin PQFP Pin Number	Function	Direction	Reset State
V_{CC}	34	20	+5 Volts	PWR	PWR
GND, AGND	30, 13	15, 42	0 Volts	PWR	PWR
IRIN	36	22	Infrared remote capture input	I	I
PWM11	1	29	14-bit pulse width modulator output*	O	I
PWM10–PWM1	20, 19, 18, 17, 2, 3, 4, 5, 6, 7	5, 4, 3, 2, 30, 31, 32, 33, 34, 35	6-bit pulse width modulator output*	O	I

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Table 1   Pin Descriptions for the Z90233, Z90234, and Z90231 (Continued)

Name	42-Pin SDIP Pin Number	44-Pin PQFP Pin Number	Function	Direction	Reset State
P56–P50	7, 6, 5, 4, 3, 2, 1	29, 30, 31, 32, 33, 34, 35	Bit-programmable input/output ports	I/O	I
P27–P20	42, 41, 40, 39, 38, 37, 35, 21	28, 27, 26, 25, 24, 23, 21, 6	Bit-programmable input/output ports	I/O	I
HLFTN	21	6	Half tone output	O	I
SDATA0, 1	40, 42	26, 28	I^2C data	I/O	I
SCLK0, 1	39, 41	25, 27	I^2C clock	I/O	I
P63–P60	16, 12, 10, 9	1, 41, 38, 37	Bit-programmable input/output ports	I/O	I
P47–P40	20, 19, 18, 17, 15, 14, 11, 8	5, 4, 3, 2, 44, 43, 39, 36	Bit-programmable input/output ports	I/O	I
XTAL1	31	16	Crystal oscillator input	I	I
XTAL2	32	17	Crystal oscillator output	O	O
OSDX1	28	13	Dot clock oscillator input	I	I
OSDX2	29	14	Dot clock oscillator output	O	O
HSYNC	26	11	Horizontal sync	I	I
VSYNC	27	12	Vertical sync	I	I
VBLANK	25	10	Video blank	O	O
R, G, B	24, 23, 22	9, 8, 7	Video R, G, B	O	O
ADC3–ADC0	9, 10, 11, 12	37, 38, 39, 41	4-bit analog-to-digital converter input	AI	I
RESET	33	19	Device reset	I/O	I

Note: *These pins are input on POR. They must be configured to be output ports for PWM applications.
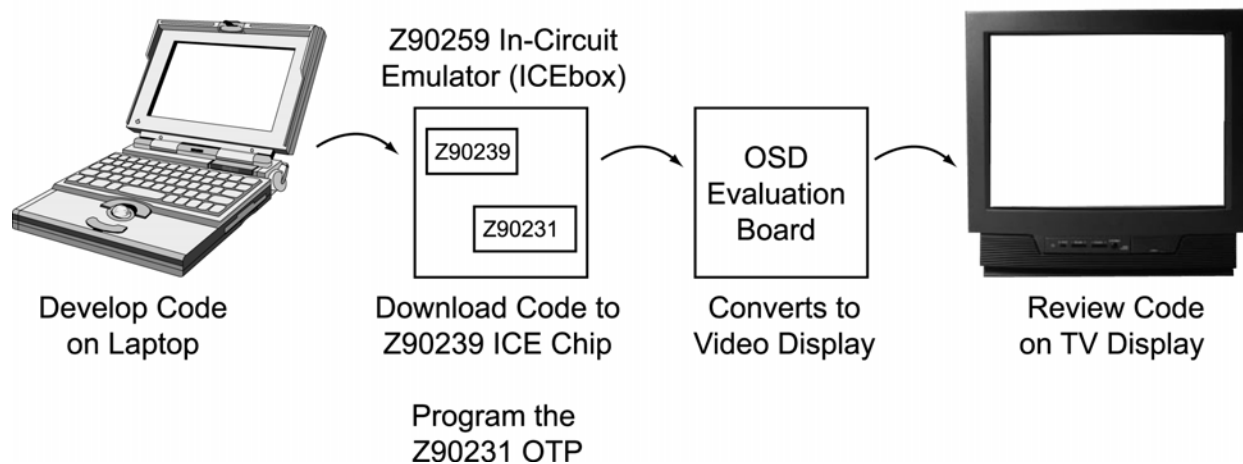
Development Tools and Support

Available in OTP and masked ROM versions, the Z90231 and Z90233/Z90234 fulfill prototype and production requirements. The Z90231 uses ICEbox^{TM} (In-Circuit Emulator) tools (Z9025900ZEM) to make programming and debugging applications easy and convenient.

The ZiLOG Developer Studio (ZDS) is a complete software program that provides easy code generation and program management.

For code development, ZiLOG offers its specialized application program interface (API) for OSD. The API deals directly with proper sequencing and timing when interfacing with hardware, shielding the user application programmer from tedious and error-prone details.

The Z8933200ZCO, an OSD evaluation board, is used to synchronize the emulator with a video display. Refer to the diagram below for a suggested code development environment.

ZiLOG also offers the Z9020900TSC Protopak to verify code on a television.

Develop Code on Laptop

Z90259 In-Circuit Emulator (ICEbox)

Z90239

Z90231

Download Code to Z90239 ICE Chip

Program the Z90231 OTP

OSD Evaluation Board

Converts to Video Display

Review Code on TV Display

Related Products

TV controllers and vertical blanking interval (VBI) decoders include the following:

Z9037x	eZVision 300 dual-scan TV controller for progressive scan and standard interlaced scan
Z9036x	eZVision 300 advanced TV controller with 32 KWords of ROM
Z86129	eZSelect closed caption decoder (CCD)
Z86229	eZSelect CCD with second I^2C address select
Z86131	eZSelect auto time set
Z86130	eZSelect smart V-chip
Z86230	eZSelect smart V-chip with second I^2C address select

Electrical Features Summary

- 40 mA maximum supply current
- 4.50 V to 5.50 V operating range

eZVision 200 Device Selection

Device	Application	ROM (Bytes)	RAM (Bytes)	Pkg	I^2C	IR Capture	ADC	Bit I/O (max)	PWM (6/14-bit)
Z90233	TV receiver controller	16K	236	42-pin SDIP 44-pin PQFP	Yes	Yes	4 Ch.	27	10/2
Z90234	TV receiver controller	24K	236	42-pin SDIP 44-pin PQFP	Yes	Yes	4 Ch.	27	10/2
Z90231	TV receiver controller	24K OTP	236	42-pin SDIP 44-pin PQFP	Yes	Yes	4 Ch.	27	10/2
Z90255	TV receiver controller	32K	300	42-pin SDIP	Yes	Yes	4 Ch.	27	10/2
Z90251	TV receiver controller	32K OTP	300	42-pin SDIP	Yes	Yes	4 Ch.	27	10/2

Ordering Information

Part	PSI	Description
Z90233	Z9023306PSC Rxxxx* Z9023306FSC Rxxxx*	16 KB masked ROM 42 SDIP 16 KB masked ROM 44 PQFP
Z90234	Z9023406PSC Rxxxx* Z9023406FSC Rxxxx*	24 KB masked ROM 42 SDIP 24 KB masked ROM 44 PQFP
Z90231	Z9023106PSC Z9023106FSC	24 KB OTP 42 SDIP 24 KB OTP 44 PQFP
Z90251	Z9025106PSC	32 KB OTP TV controller
Z90255	Z9025506PSC Rxxxx*	32 KB masked ROM TV controller
Z9025900ZEM	Z9025900ZEM	Emulator/programmer
Z9020900TSC	Z9020900TSC	Protopak
Z8933200ZCO	Z8933200ZCO	OSD evaluation board

* xxxx is a unique ROM number assigned to each customer code.

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