Product sheet

ADAC250

High-speed dual A/D and D/A FMC module

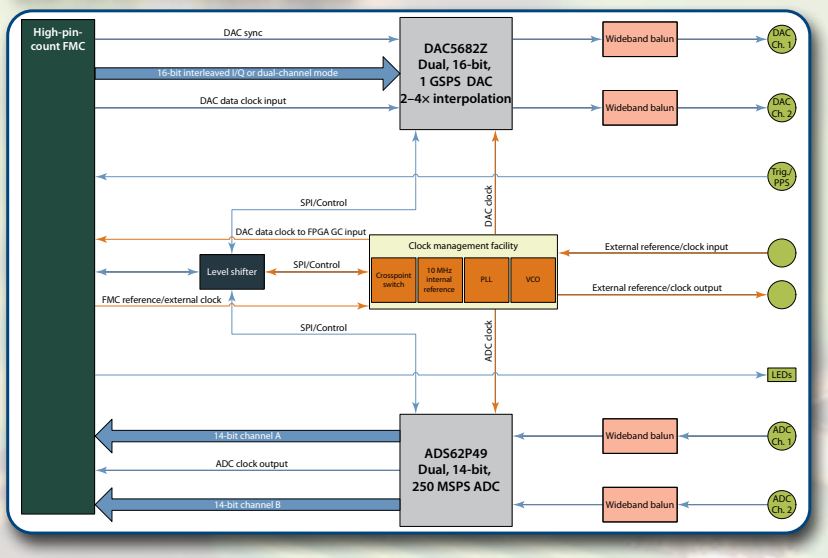
- Two, 250 MSPS, 14-bit ADCs
- Two, 1 GSPS, 16-bit DACs
- Supports multiple clock and reference configurations
- Versatile and industry-standard VITA 57.1 FMC module
- Plug & Play with Lyrtech's µTCA Perseus AMCs

RoHS compliant

The ADAC250 FPGA mezzanine card (FMC) is designed around the high-performance A/D and D/A conversion technology from Texas Instruments — it integrates one dual, 14-bit, 250 MSPS analog-to-digital converter (ADS62P49) and a dual, 16-bit, 1 GSPS digital-to-analog converter (DAC5682Z; also capable of a 2–4× interpolation mode). Combined with multiple clocks and synchronization modes, the ADAC250 is at its best in DSP applications such as software-defined radio (SDR), advanced telecommunications (MIMO systems, cognitive radios, beamformers, LTE, WiMAX), signal intelligence (SIGINT), radar, sonar, and medical imaging applications.

The ADAC250 uses the VITA 57.1 standard, widely used in the digital signal processing industry, which makes it easier for developers to integrate FPGAs into their embedded system designs. The FMC is completely Plug & Play with our µTCA Perseus AMCs, but the ADAC250 can as easily be used on any FMC carrier out there.

ADAC250 functional block diagram



Hardware architecture

The VITA 57.1 (FMC) standard comes to the rescue of complex designs with its unprecedented mechanical and electrical flexibility — VITA 57.1 provides a standard specification for small mezzanine modules designed to adapt an FPGA-based carrier card to different I/O requirements.

Features

- 2× 14-bit, 250 MSPS ADC (ADS62P49)
- 2× 16-bit, 1 GSPS DAC (DAC5682Z)
- Integrated programmable gains on both converters
- Wideband, AC-coupled I/Os
- DAC capable of 2–4× interpolation modes (low pass/ high pass), coarse mixing, offset adjustments, and delay adjustments.
- Equipped with an onboard, low-jitter reference clock and synchronization PLL (AD9511).
- Supports external or FMC-driven reference clocks for synchronized multiboard/multichannel applications.
- Supports external or FMC-driven sampling clocks (AD9511 with the PLL bypassed) for phase-coherent multiboard/ multichannel applications.
- Supports external triggers for event-based acquisition.

Clock management facility

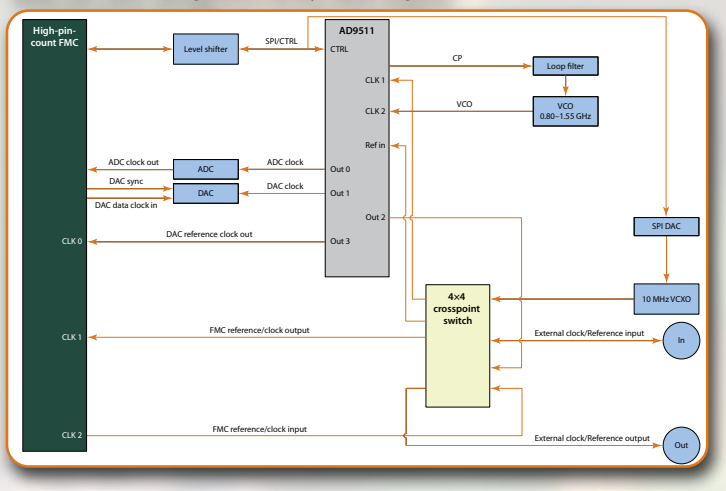
The ADAC250's clock management facility is designed around the AD9511 from Analog Devices, which offers low phase noise clock distribution, a bypassable PLL core, bypassable dividers, and the possibility to adjust the phase of five clock outputs. Combining the clock management facility to the very-low-jitter 4×4 crosspoint switch makes it possible to generate the sampling clock of the ADAC250 several different ways:

Infinite possibilities...

LYRTECH

- From an external clock or reference connected to the ADAC250's front panel
- From a clock or reference supplied by the ADAC250's carrier FMC
- From the ADAC250's onboard, low-jitter 10 MHz reference

ADAC250 clock management facility block diagram



A PPS signal can be sent to the carrier's FPGA to dynamically adjust the ADAC250's onboard VCXO through its SPI DAC — something especially useful where a GPS-disciplined clock is needed to drive sampling clocks. For details about the GPS-disciplined FPGA core, contact info@lyrtech.com.

Performances

Analog-to-digital converters

- Analog input bandwidth (–3dB): 470 MHz
- Conditions: F_s = 250 MSPS, F_{in} (MHz) = 30 70 150
  - Full-scale input (dBm): 11.0 11.0 11.0
  - SNR (dB): 70.5 70.0 65.0
  - 2nd harmonic (dBc): –81.0 –91.0 –84.0
  - 3rd harmonic (dBc): –75.0 –85.0 –73.0
  - SFDR (dBc): 75.0 85.0 74.0
  - Noise floor (dBFS): –115.0 –115.0 –109.0
  - THD (dBc): –74.0 –84.0 –74.0

Digital-to-analog converters

- Analog output bandwidth: 500 MHz
- Conditions: F_s = 1 GSPS, F_{out} (MHz) = 30 70 150
  - Power (dBm): –21.0–2.5 –21.0–2.5 –22.0–1.0
  - 2nd harmonic (dBc): 63.0 –57.0 54.0
  - 3rd harmonic (dBc): 69.0 –61.0 –52.0
  - SFDR (dBc): 72.0 58.0 50.0
  - Phase noise (10 kHz; –dBc/Hz): 110.0 108.0 107.0
  - Phase noise (100 kHz; –dBc/Hz): 120.0 119.0 119.0
  - Phase noise (1 MHz; –dBc/Hz): 125.0 122.0 121.0

Specifications

ADAC250 on Perseus

FMC connectivity

- High-pin-count connector
- LA (00–33), HA (00–11)
- CLK (0–2)
  - CLK0, CLK1: M2C clocks
  - CLK2: C2M clock

Front panel

- MMCX connectors
  - ADC and DAC channels A/B
  - External trigger/PPS
  - External reference/clock input and output
- ADC/DAC/PLL status LED × 4

Mechanical

- Dimensions: 69 mm × 10 mm × 84 mm (W×H×D)
- Rugged FMC form factor — designed for conduction cooling, but not tested or implemented. Contact info@lyrtech.com for details.

Standards compliance

- VITA 57.1

Electrical

- 12 V
- 3.3 V
- V_{adj} to 2.5 V necessary to power ADAC250 ICs

Power consumption

The power consumption below was calculated at FS_{ADC} = 250 MHz, FS_{DAC} = 1 GHz (4× interpolation), with all converters at maximum gain. The ADAC250's power consumption will vary according to converter settings.

- 7 W (maximum)

Environmental

Contact Lyrtech for details about this specification.

Purchase information

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