Technical Data

MC44C401
Rev. 1.1 02/2004

MC44C401
MTS Stereo Encoder

MC44C401

Ordering Information		
Device	**Temp. Range**	**Package**
MC44C401FA	0°C to 70°C	32TQFP

Contents

The MC44C401 Multi-Channel Television Sound (MTS) Stereo Encoder is the industry's first, single-chip, CMOS implementation of a Broadcast Television Systems Committee (BTSC)-compatible stereo encoder.
The MC44C401 MTS Stereo Encoder is designed for use in set-top boxes, VCRs, DVD players/recorders, game stations, and other applications that are required to output high-quality stereo sound through a single RF coaxial cable.
The digital audio processing used in the MC44C401 preserves the full fidelity of surround sound and other audio coding schemes while ensuring overall system performance is not impacted by copy protection technologies.
The MC44C401 is engineered to process right and left analog audio signals and baseband composite video to generate a stereophonic composite signal in accordance with BTSC system standards. The MC44C401 is designed to output this signal to a Motorola RF modulator, which in turn produces a stereo encoded RF channel for use with any BTSC stereo television receiver.

1 Features

- Integrated A/D input and D/A output circuitry
- CEX™ digital audio processing encodes and transports stereo signals
- Surround sound and Macrovision™ compatible
- Extended low frequency response (The MC44C401 frequency response extends below 25 Hz)

- Simple passive interface to Motorola's MC44BC374 (UHF/VHF) and MC44BC375 (VHF) modulators
- Preservation of original surround sound fidelity
- System performance not impacted by copy protection technologies
- Enables lower system component count, smaller board size, and significantly lower overall system cost
- Eliminates manual alignment of filters, phase controls, and composite signal amplitude

2 Reference Documentation

- "Multichannel Television Sound Transmission and Audio Processing Requirements for the BTSC System", FCC OET Bulletin No. 60, February 1986.

3 Block Diagrams

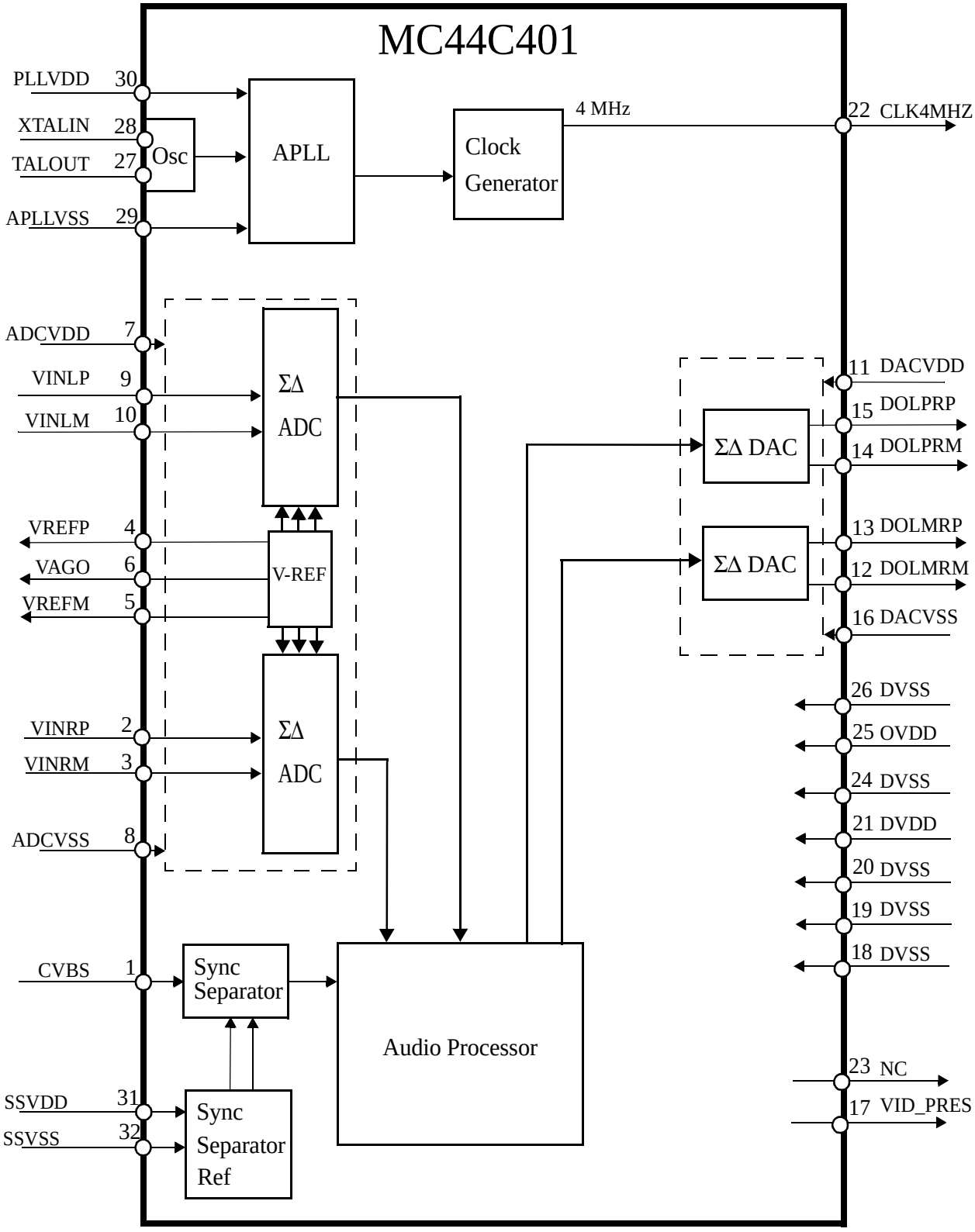


Figure 1. MC44C401 Block Diagram

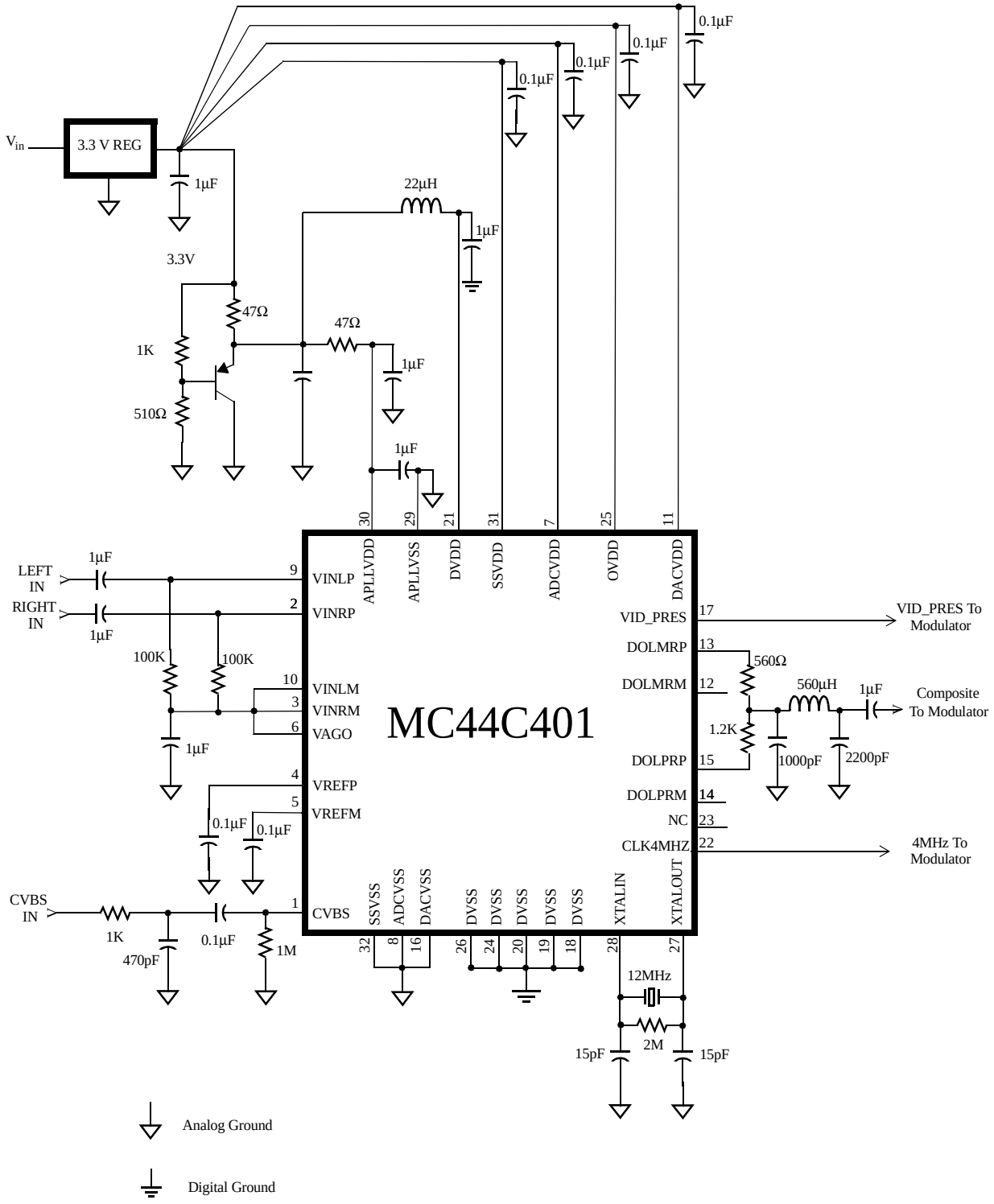


Figure 2. MC44C401 Recommended Usage

4 I/O Description

4.1 Signal List

The Stereo Modulator I/O signals are described in Table 1.

Table 1. MC44C401 Signal Descriptions

Signal	Pin #	Description
Analog		
VINLP	9	Left channel input voltage plus
VINLM	10	Left channel input voltage minus
VREFP	4	Left & Right ADC ref. input voltage plus
VAGO	6	Left & Right ADC analog virtual ground
VREFM	5	Left Right ADC ref. input voltage minus
VINRP	2	Right channel input voltage plus
VINRM	3	Right channel input voltage minus
CVBS	1	Composite video input
Digital		
DOLPRP	15	Left+Right channel output voltage plus
DOLPRM	14	Left+Right channel output voltage minus
DOLMRP	13	Left-Right channel output voltage plus
DOLMRM	12	Left-Right channel output voltage minus
VID_PRES	17	Video present flag, 0 = no video, hi-z = video present
NC	23	NC
Clocks		
XTALIN	28	Crystal input
XTALOUT	27	Crystal output
CLK4MHZ	22	4 MHz clock for Audio/Video modulator IC
Power Supply		
APLLVDD	30	APLL analog supply voltage, 1.8 V
APLLVSS	29	APLL analog ground
SSVDD	31	Sync Separator analog supply voltage, 3.3 V

Table 1. MC44C401 Signal Descriptions (Continued)

Signal	Pin #	Description
SSVSS	32	Sync Separator analog ground
ADCVDD	7	ADC analog supply voltage, 3.3 V
ADCVSS	8	ADC analog ground
DACVDD	11	DAC I/O supply voltage, 3.3 V
DACVSS	16	DAC I/O ground
DVDD	21	Digital Logic supply voltage, 1.8 V
DVSS	18, 19, 20, 24, 26	Digital Logic/I/O ground
OVDD	25	I/O supply voltage, 3.3 V

5 Electrical Specifications

5.1 DC Characteristics

Table 1. MC44C401 DC Characteristics (Preliminary)

PIN	Symbol	Parameter	Min	Typ	Max	Unit
DVDD	—	1.8 V Digital Logic	1.62	1.80	1.98	V
DVDD	—	1.8 V Digital Logic	—	18.0	22.0	mA
OVDD	—	3.3 V Digital Output	2.97	3.30	3.63	V
OVDD	—	3.3 V Digital Output	—	2.0	8.0	mA
DACVDD	—	3.3 V DAC Supply	2.97	3.30	3.63	V
DACVDD	—	3.3 V DAC Supply		7.0	9.0	mA
ADCVDD	—	3.3 V ADC Supply	2.97	3.30	3.63	V
ADCVDD	—	3.3 V ADC Supply	—	7.0	9.0	mA
SSVDD	—	3.3 V Sync. Sep Supply	2.97	3.3	3.63	V
SSVDD	—	3.3 V Sync. Sep Supply	—	2.0	—	mA
APLLVDD	—	1.8 V APLL Supply	1.62	1.8	1.98	V
APLLVDD	—	1.8 V APLL Supply	—	3.0	—	mA
VREFP	—	Voltage Ref. Bypass plus	—	2.0	—	V
VREFM	—	Voltage Ref. Bypass minus	—	1.0	—	V

Table 1. MC44C401 DC Characteristics (Preliminary) (Continued)

PIN	Symbol	Parameter	Min	Typ	Max	Unit
VAGO	—	Voltage Ref. Ground	—	1.5	—	V
VINXX	V_{il}	Signal Input	VREFM		VREFP	V
VINXX	V_{ih}	Signal Input	VREFM		VREFP	V
CVBS		Video input (See Figure 2)	—	1	—	V_{pp}
CLK4MHZ	V_{ol}	4 MHz Clock Output @ I =.6 mA	2.97	—	—	V
CLK4MHZ	V_{oh}	4 MHz Clock Output @ I =.6 mA	—	—	3.63	V
DOLPRP	V_{ol} [a]	Output Left-plus-Right plus	—	2.2	—	V_{pp}
DOLPRP	V_{oh} [b]	Output Left-plus-Right plus	—	2.2	—	V_{pp}

a. V_{ol} is measured at I_{load}= 6 mA (see test circuit Figure 2)
b. V_{oh} is measured at I_{load}= 6 mA (see test circuit Figure 2)

5.2 AC Characteristics

Table 1. MC44C401 AC Characteristics (Preliminary) (See Figure 2)

SIGNALS	Symbol	Parameter [a]	Min	Typ	Max	Unit
LEFT/RIGHT IN	—	Input Level	—		1.0	V_{pp}
LEFT/RIGHT IN	—	Input Impedance	—	22	—	kΩ
COMPOSITE	—	Composite Output Level [b]	v	2.2	—	V_{pp}
COMPOSITE	—	Mono SNR [c]	65	75	—	dB
COMPOSITE	—	Stereo SNR [c]	55	65	—	dB
COMPOSITE	—	THD		0.1	0.3	%
COMPOSITE	—	-1 db Bandwidth	20	—	14000	Hz
CVBS IN	—	Video Level	0.5	—	2.0	V_{pp}
CVBS	Zin	Video Input Impedance	—	1000	v	Ω
—	—	Stereo Separation 500Hz–5KHz	25	35	—	dB
—	—	Stereo Separation 100Hz–10KHz	20	30	—	dB

a. See Figure 2 for test setup
b. Test conditions 1 kHz 0 dB
c. Measured in 20 Hz to 13.5 kHz bandwidth

6 Package Data

6.1 MC44C401 Package

The MC44C401 pin-outs (32TQFP package) are shown in Figure 3.

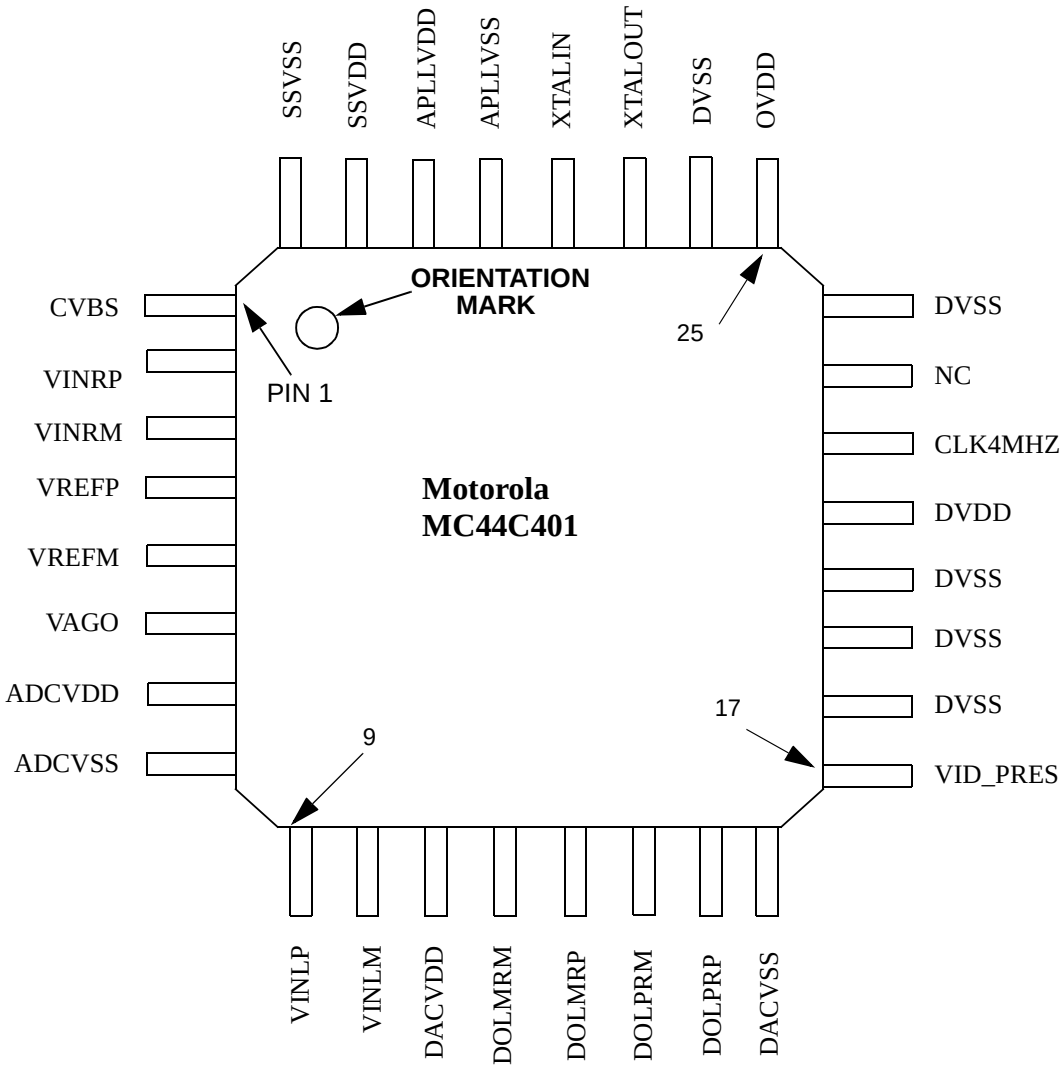
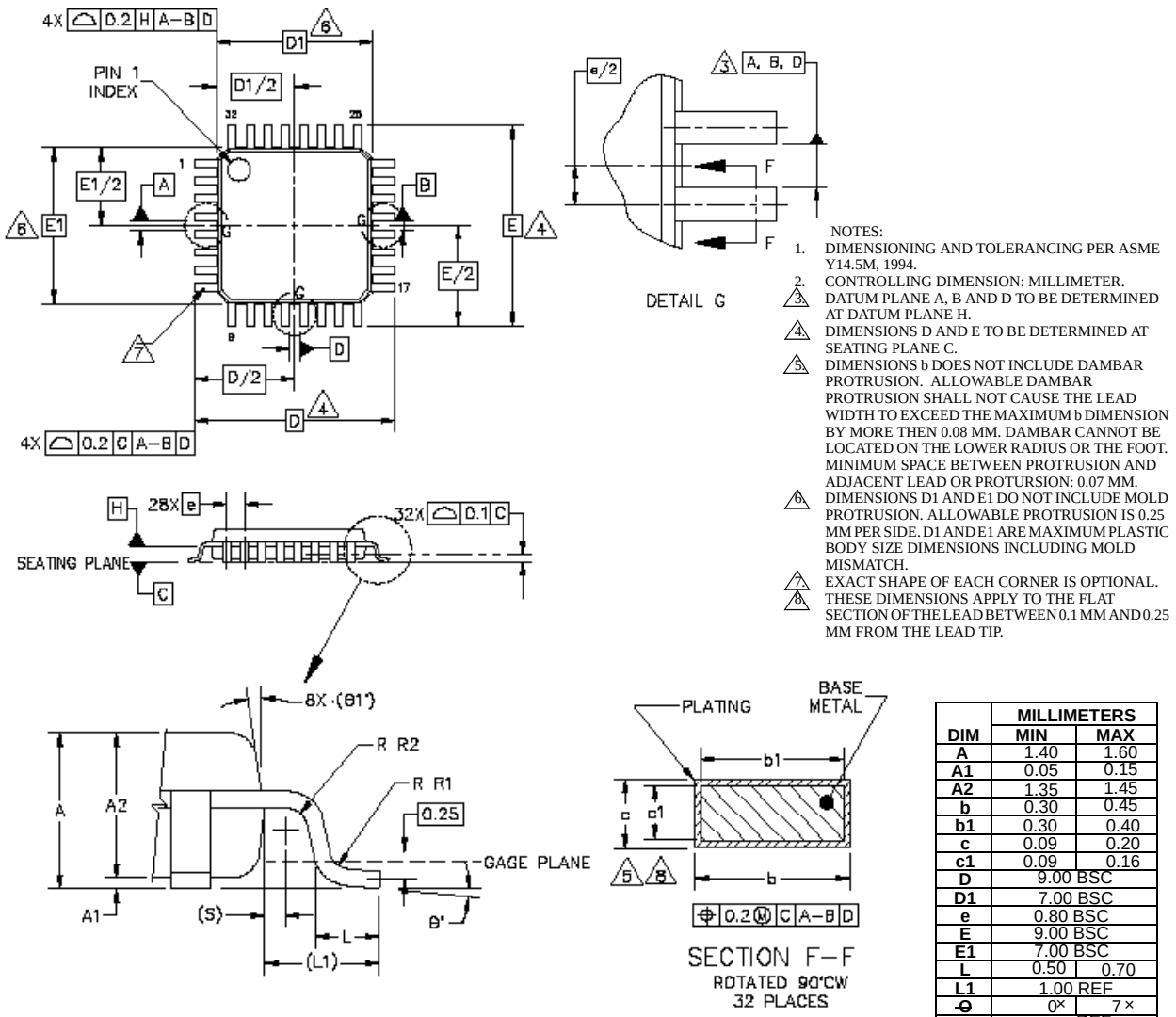


Figure 3. MC44C401 32TQFP Package

6.2 Mechanical Data



DIM	MILLIMETERS MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
θ	0°	7°
θ1	12° REF	
R1	0.08	0.20
R2	0.08	—
S	0.20 REF	

Figure 4. Package Mechanical Information

7 Functional Description

The following sections provide brief descriptions of the MC44C401 modules.

7.1 Phase Locked Loop (APLL)

The APLL locks to the reference frequency of 12 MHz and generates the master clock.

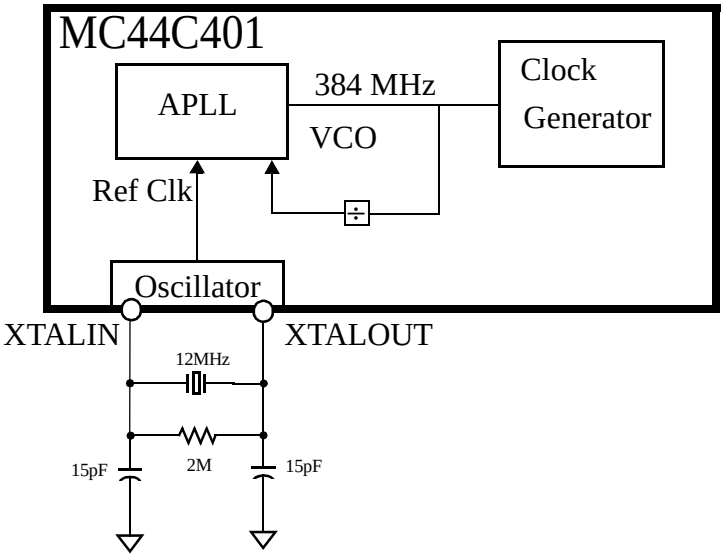


Figure 5. APLL and Clock Generator

7.2 Sync Separator

The Sync Separator, shown in Figure 6, extracts the composite sync from the incoming composite video signal.

The composite sync is used by the Audio Processor to generate the 15.734 kHz pilot tone and the 31.468 kHz carrier to modulate the Left-Right channel. The nominal output level of composite video signal sources is 1 V_{pp} on 75 Ω and the sync amplitude is 0.3 V.

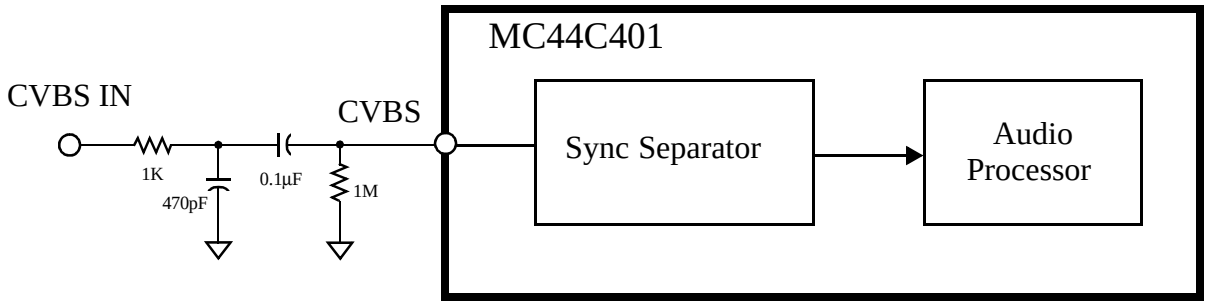


Figure 6. Sync Separator

8 Calibration

The following sections show methods for setting various output levels for optimum system performance.

8.1 Modulator Sensitivity

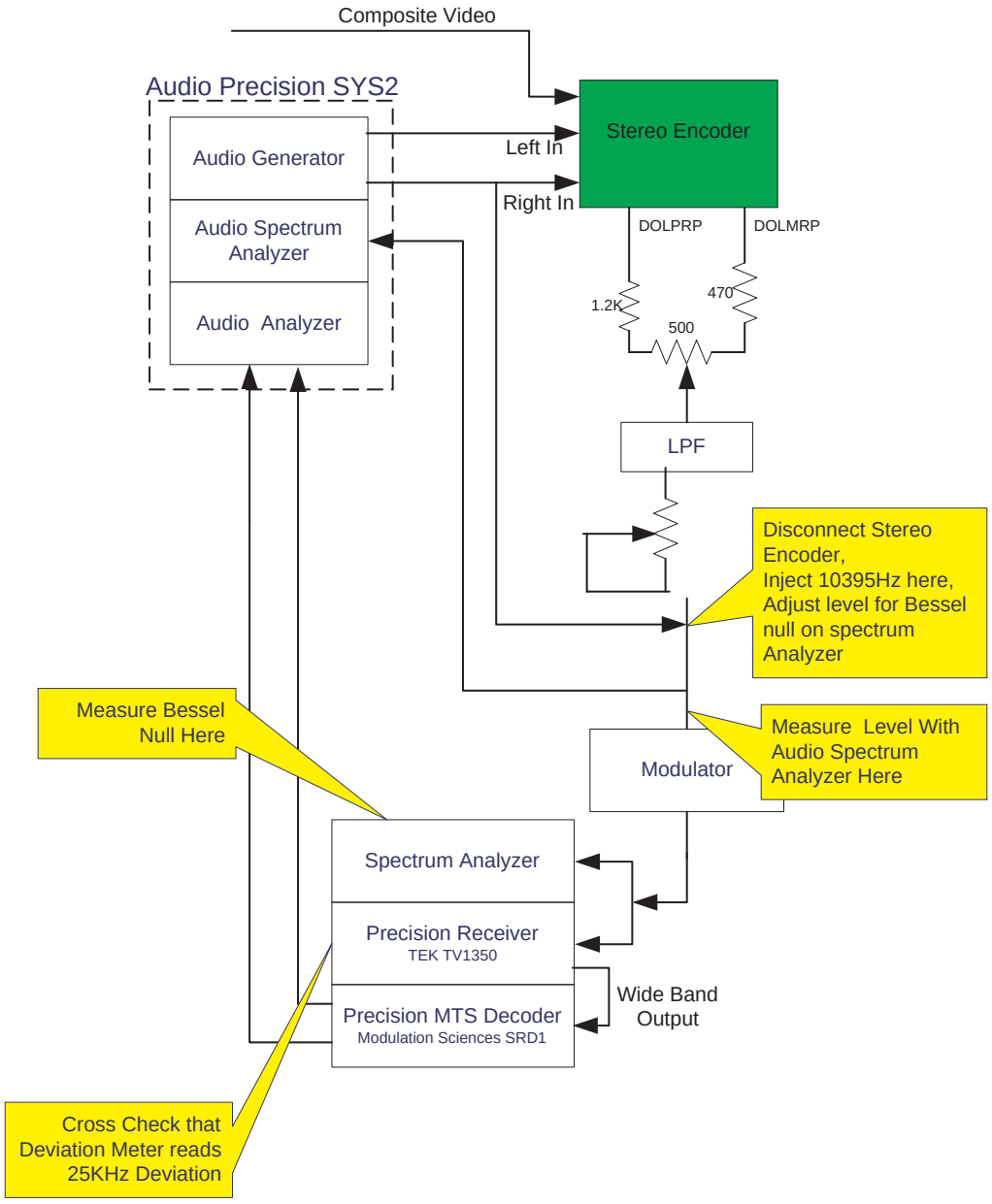


Figure 7. Measuring Modulator Sensitivity

8.2 Setting Output Levels

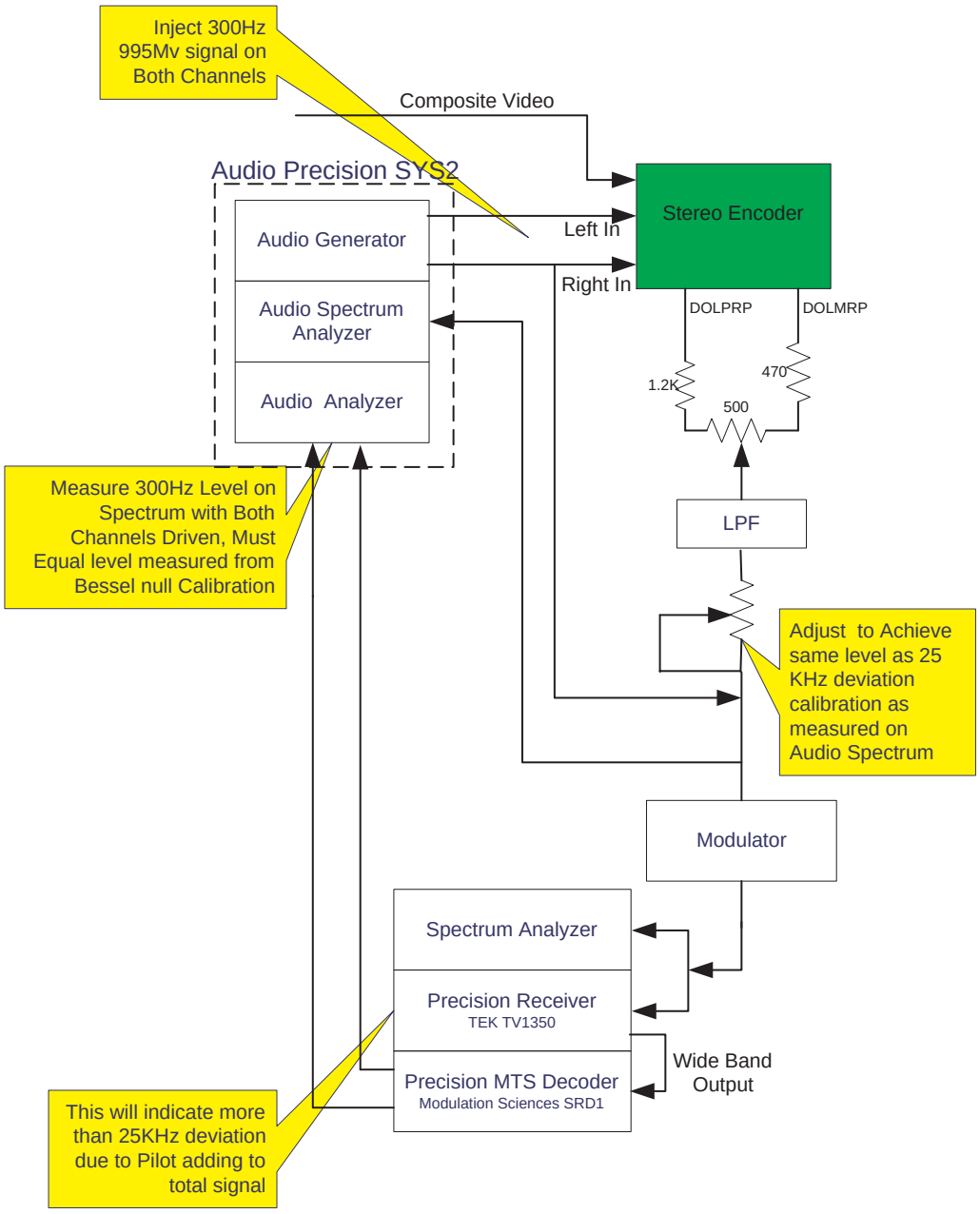


Figure 8. Setting Output Levels

8.3 Setting Sum/Difference Channels

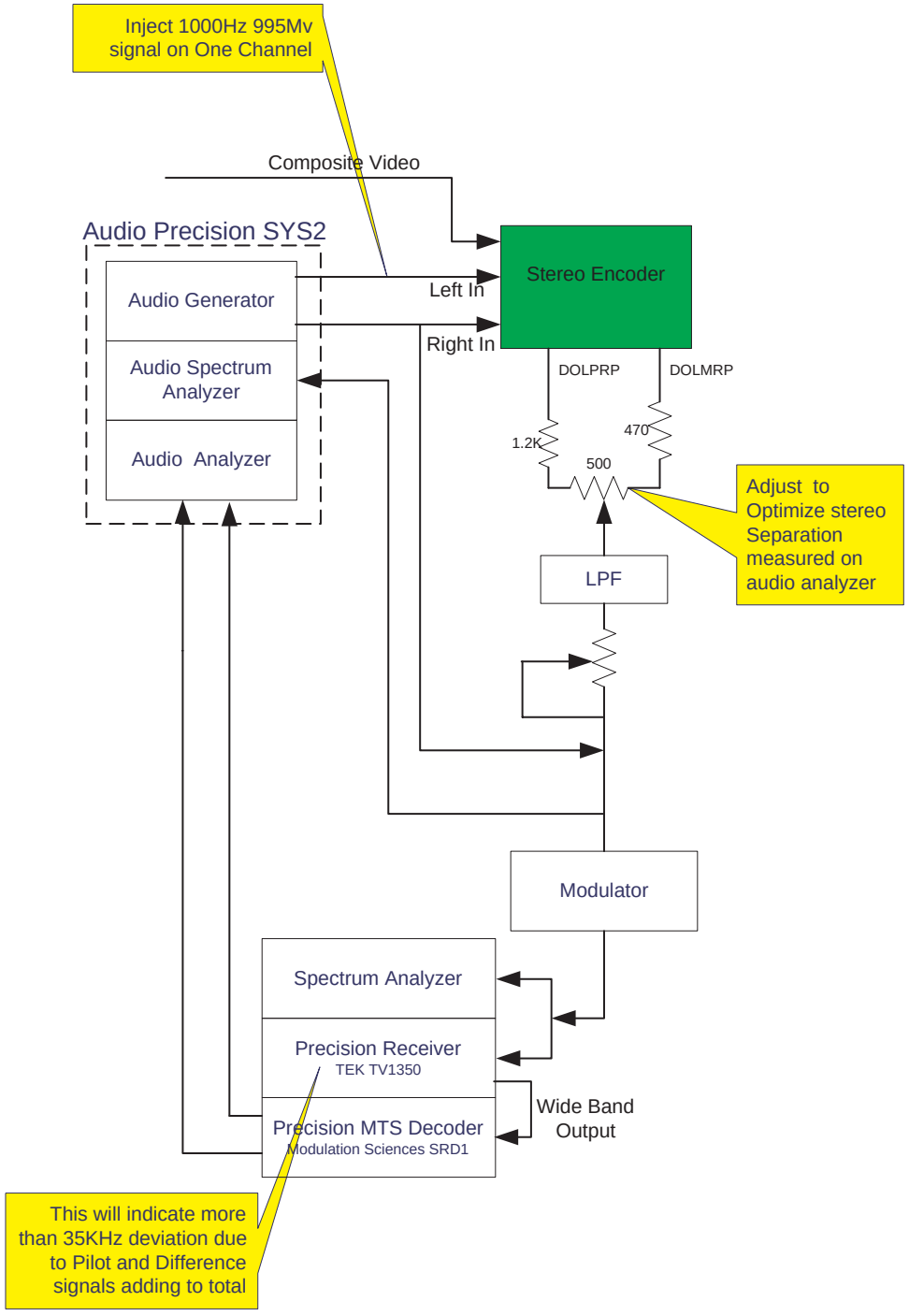


Figure 9. Setting Sum/Difference Channel Balance

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