19-0614; Rev 0; 8/06

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

General Description

The MAX4919B/MAX4920B/MAX4921B overvoltage protection controllers protect low-voltage systems against high-voltage faults up to +28V. An internal 1.8A (min) pFET with low R_{ON} (100mΩ) switches a battery to the load and also protects the battery against short-circuit faults. When a short circuit occurs, the current through the internal pFET is limited for a blanking period. If the short condition is present after the blanking period, the switch is latched off and remains off until one of the input signals (IN, HP_PWR, PWR_ON) is cycled. The pFET is turned on by a logic-high voltage at PWR_HOLD, HP_PWR, PWR_ON, or IN .

The overvoltage thresholds (OVLO) are preset to +6.38V (MAX4919B), +5.80V (MAX4920B), and +4.65V (MAX4921B). When the input voltage drops below the undervoltage lockout (UVLO) threshold, the devices enter a low-current standby mode. In shutdown mode, the current is reduced to 0.4µA. The MAX4919B/MAX4920B have a +4.27V UVLO threshold, and the MAX4921B has a +2.35V UVLO threshold.

The MAX4919B/MAX4920B/MAX4921B are offered in a small 14-pin TDFN package (3mm x 3mm) with an exposed paddle and are specified over the extended -40°C to +85°C temperature range.

Applications

Cell Phones

Digital Still Cameras

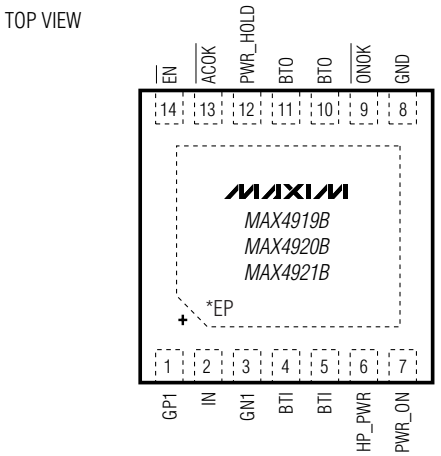
PDAs and Palmtop Devices

MP3 Players

Features

- **Input Overvoltage Protection Up to +28V**
- **Preset Overvoltage Protection Trip Level**
  - **6.38V (MAX4919B)**
  - **5.80V (MAX4920B)**
  - **4.65V (MAX4921B)**
- **Adapter/Car-Kit Auto-Selector**
- **Low-Current Undervoltage Lockout Mode**
- **Internal 1.8A (min) Battery Switchover FET**
- **Integrated Low-Battery Detect**
- **Battery Short-Circuit Protection**
- **Low-Cost External nMOS Overvoltage FET**
- **14-Pin TDFN Package (3mm x 3mm)**

Pin Configuration



TDFN (3mm x 3mm)
*EXPOSED PADDLE
+DENOTES LEAD-FREE PACKAGE

Ordering Information/Selector Guide

PART	PIN-PACKAGE	OVLO (V)	UVLO (V)	TOP MARK	PKG CODE
MAX4919BETD+T	14 TDFN-EP*	6.38	4.27	ABY	T1433-2
MAX4920BETD+T	14 TDFN-EP*	5.80	4.27	ABZ	T1433-2
MAX4921BETD+T	14 TDFN-EP*	4.65	2.35	ACA	T1433-2

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes lead-free package.
**EP = Exposed paddle.*

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
GP1, GN1 to GND .....-0.3V to +12V
IN to GP1 .....-0.3V to +20V
BTO to GND .....-0.3V to +6.1V
BTI to BTO .....-0.3V to +6V
BTI, $\overline{ACOK}$, PWR_ON, $\overline{EN}$ to GND .....-0.3V to +6V
HP_PWR, $\overline{ONOK}$, PWR_HOLD to GND .....-0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
14-Pin TDFN (derate 18.5mW/°C above +70°C) 1482mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V (MAX4919B/MAX4920B) or V_{IN} = 4.2V (MAX4921B), V_{BTI} = 4V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			1.2		28	V
Input Supply Current	I_{IN}	MAX4919B/MAX4920B			77	120	µA
		MAX4921B			75	110	
UVLO Supply Current	I_{UVL}	$V_{\overline{EN}}$ = 0V; V_{IN} = 3.9V; MAX4919B/MAX4920B			10	22	µA
		$V_{\overline{EN}}$ = 0V; V_{IN} = 2.1V; MAX4921B			8	18	
Shutdown Supply Current	I_{SHDN}	$V_{\overline{EN}}$ = 1.6V, V_{IN} = 3.6V			0.4	2	µA
IN Undervoltage Lockout	V_{UVLO}	V_{IN} falling	MAX4919B/MAX4920B	4.00	4.27	4.54	V
			MAX4921B	2.20	2.35	2.50	V
IN Undervoltage Lockout Hysteresis					1		%
Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	MAX4919B	6.00	6.38	6.76	V
			MAX4920B	5.44	5.80	6.17	
			MAX4921B	4.35	4.65	4.95	
IN Overvoltage Lockout Hysteresis					1		%
BATTERY SWITCHOVER							
BTI Input Range	V_{BTI}			2.30		5.50	V
BTI UVLO	V_{UVBTI}	V_{BTI} falling		2.0	2.15	2.3	V
BTI UVLO Hysteresis					1.5		%
BTI Low-Battery Threshold	V_{LVBTI}	V_{BTI} falling		2.65	2.82	3	V
BTI Low-Battery Hysteresis					1.5		%
BTI Supply Current		Adapter out, V_{PWR_HOLD} = high, $\overline{EN}$ = high				7	µA
BTI Shutdown Current		V_{BTO} = 0V	T_A = +25°C			2	µA
			T_A = -40°C to +85°C			2.8	
INTERNAL pFET							
Switch On-Resistance	R_{ON}	V_{BTI} = 2.7V, $I_{BTI\ to\ BTO}$ = 0.5A	T_A = +25°C			100	mΩ
			T_A = -40°C to +85°C			120	
Forward-Overload Current Limit	I_{LIM}	BTO shorted to GND		1.8			A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V (MAX4919B/MAX4920B) or V_{IN} = 4.2V (MAX4921B), V_{BTI} = 4V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVERS						
GN1 Turn-On Voltage	V_{GN1}	V_{GN1} referenced to GND, I_{GN1} sourcing 1µA; MAX4919B/MAX4920B	9		10	V
		V_{GN1} referenced to GND, I_{GN1} sourcing 1µA; MAX4921B	7.8		8.4	
GN1 Pulldown Current	I_{GPD}	V_{IN} > OVLO, V_{GN1} = 5.5V		30		mA
GP1 Clamp Voltage	V_{CLAMP}	V_{IN} - V_{GP1} when V_{IN} = 28V	12.5	16.5	19.5	V
GP1 Pulldown Resistor	R_{GPD}		31	51.5	72	kΩ
LOGIC INPUTS (PWR_HOLD, HP_PWR, PWR_ON, $\overline{EN}$)						
Input-High Voltage	V_{IH}	V_{BTI} = 5.50V	1.5			V
Input-Low Voltage	V_{IL}	V_{BTI} = 2.3V for PWR_HOLD, HP_PWR and $\overline{EN}$; V_{BTI} = 3V for PWR_ON			0.4	V
PWR_HOLD, $\overline{EN}$ Input Leakage Current	I_{LKG}	$\overline{EN}$, PWR_HOLD = GND or 5.5V	-1		+1	µA
PWR_ON, HP_PWR Pulldown Resistance	R_{IPD}		200			kΩ
LOGIC OUTPUTS ($\overline{ACOK}$, $\overline{ONOK}$)						
Output-Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output-High Leakage Current					1	µA
TIMING						
IN Debounce Time	t_{INDBC}	Time from UVLO < V_{IN} < OVLO to V_{GN1} > 0.3V, C_{GN1} = 500pF	10	25	40	ms
$\overline{ACOK}$ Blanking Time	t_{BLNKAC}	Time from V_{GN1} > 0.3V to $\overline{ACOK}$ low, C_{GN1} = 500pF	10	25	40	ms
HP_PWR Debounce Time	t_{HPDBC}	Time for internal pFET to turn on after V_{HP_PWR} > V_{IH}	10	25	40	ms
$\overline{ACOK}$ One-Shot Time	t_{1SHAC}	V_{PWR_HOLD} = 0V; time for internal pFET to turn off after $\overline{ACOK}$ < V_{OL} (Figure 1)	488	1220	1952	ms
HP_PWR One-Shot Time	t_{1SHHP}	V_{PWR_HOLD} = 0V; time for internal pFET to turn off after V_{HP_PWR} > V_{IH} (Figure 2)	488	1220	1952	ms
Current-Limit Blanking Time	t_{CLIM}	V_{BTI} = 2.7V; V_{BTO} shorted to GND; time for internal pFET current to reduce to 10mA	4	10	16	ms
GN1 Turn-On Time	t_{GON}	V_{GN1} = 0.3V to 8V (MAX4919B/MAX4920B), V_{GN1} = 0.3V to 7V (MAX4921B), C_{GN1} = 500pF		10		ms

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V (MAX4919B/MAX4920B) or V_{IN} = 4.2V (MAX4921B), V_{BTI} = 4V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

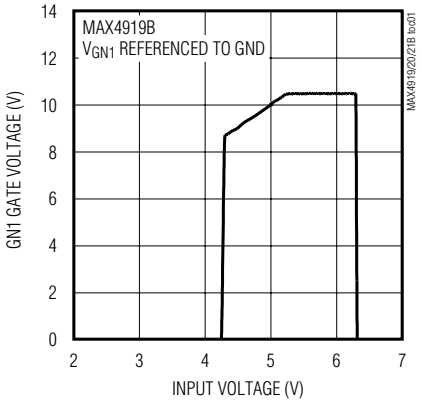
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GN1 Turn-Off Time	t_{GOFF}	V_{IN} rising at 1V/µs from 5V to 8V (MAX4919B/MAX4920B), or from 4V to 7V (MAX4921B); V_{GN1} = 0.3V, C_{GN1} = 500pF		6	20	µs
Initial Overvoltage Fault Delay	t_{OVLO}	V_{IN} rising at 1V/µs from 0V to 9V, time from V_{IN} = 5V to I_{GN1} = 80% of I_{GPD}		1.5		µs
$\overline{ACOK}$ Deassertion Delay	$t_{\overline{ACOK}}$	V_{IN} rising at 1V/µs from 5V to 8V (MAX4919B/MAX4920B), or from 4V to 7V (MAX4921B); $V_{\overline{ACOK}}$ pullup voltage = 3V; $R_{\overline{ACOK}}$ = 10kΩ (Figure 3)		5.8		µs
Disable Time	t_{DIS}	$V_{\overline{EN}}$ = 2.4V, V_{GN1} = 0.3V, C_{GN1} = 500pF		2		µs

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications over T_A = -40°C to +85°C are guaranteed by design.

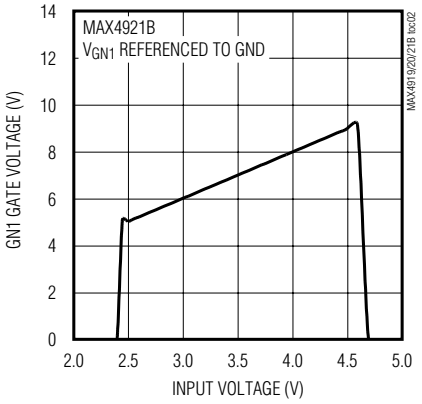
Typical Operating Characteristics

(V_{BTI} = 4V, T_A = +25°C, unless otherwise noted.)

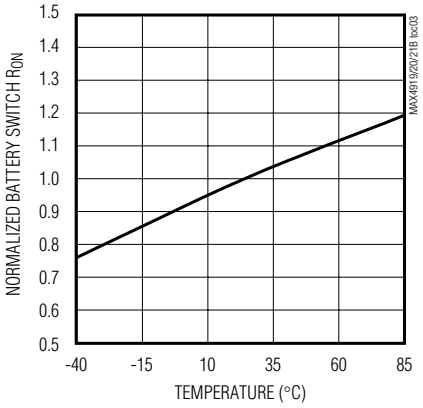
GN1 GATE VOLTAGE vs. INPUT VOLTAGE



GN1 GATE VOLTAGE vs. INPUT VOLTAGE



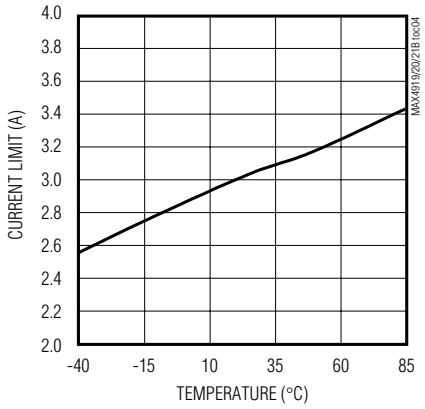
NORMALIZED BATTERY SWITCH R_{ON} vs. TEMPERATURE



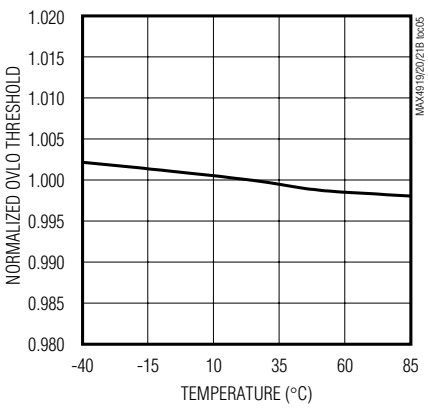
Typical Operating Characteristics (continued)

(V_{BTI} = 4V, T_A = +25°C, unless otherwise noted.)

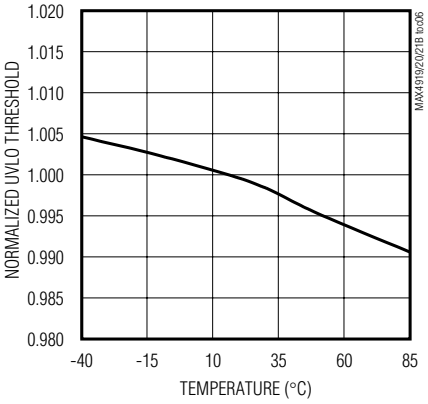
CURRENT LIMIT vs. TEMPERATURE



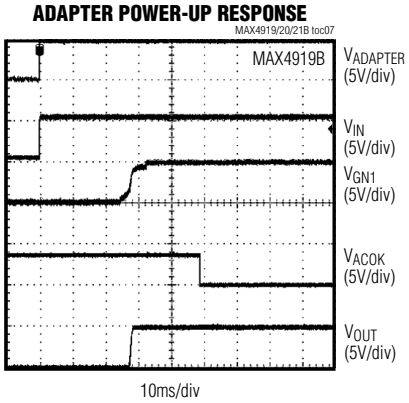
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



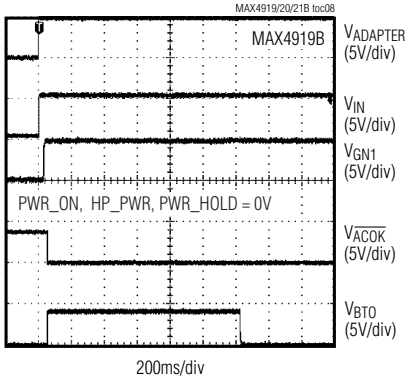
NORMALIZED UVLO THRESHOLD vs. TEMPERATURE



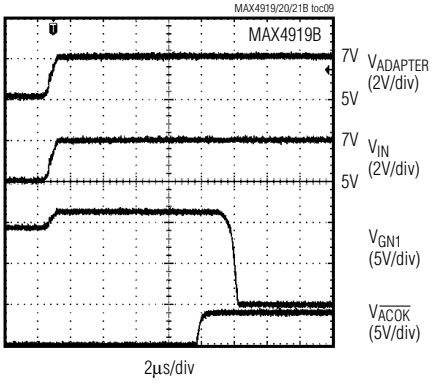
ADAPTER POWER-UP RESPONSE



ADAPTER POWER-UP RESPONSE



OVERVOLTAGE RESPONSE

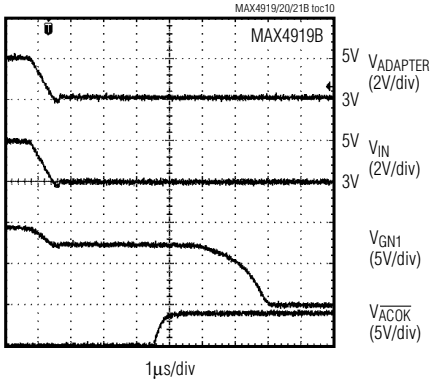


Battery Power-Up Logic with Overvoltage and Overcurrent Protection

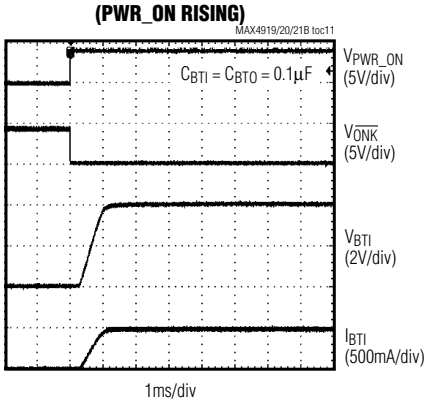
Typical Operating Characteristics (continued)

(V_{BTI} = 4V, T_A = +25°C, unless otherwise noted.)

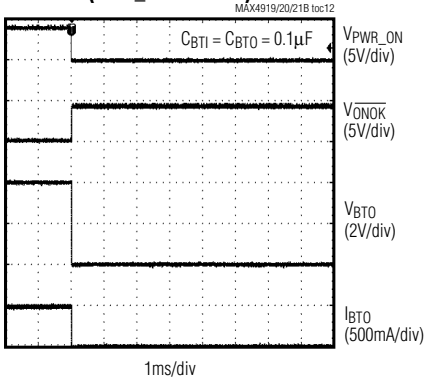
UNDERVOLTAGE RESPONSE



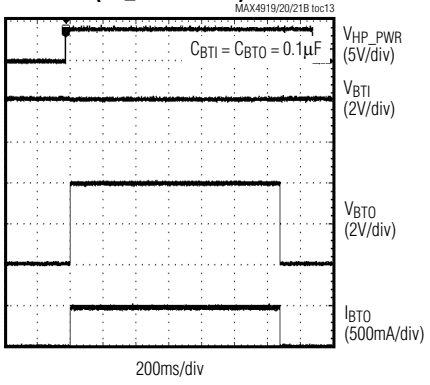
BATTERY-SWITCH TURN-ON RESPONSE (PWR_ON RISING)



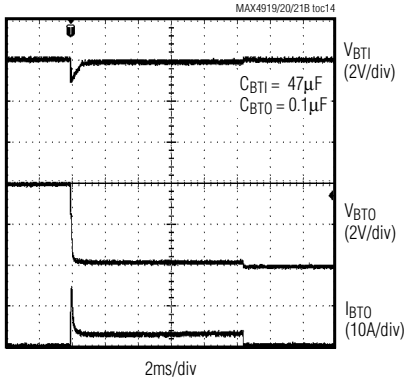
BATTERY-SWITCH TURN-OFF RESPONSE (PWR_ON FALLING)



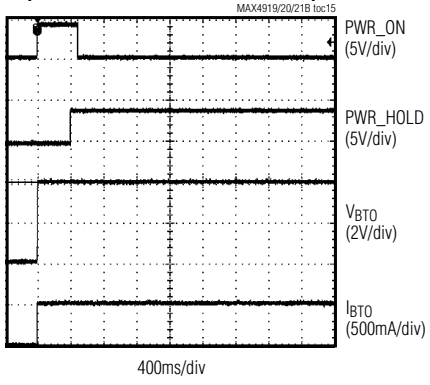
BATTERY-SWITCH TURN-ON RESPONSE (HP_PWR RISING)



SHORT-CIRCUIT RESPONSE



BATTERY SWITCH TURN-ON RESPONSE (PWR_ON AND PWR_HOLD RISING)



Pin Description

PIN	NAME	FUNCTION
1	GP1	p-Channel MOSFET Gate-Drive Output. GP1 pulls the external pFET gate down when the input is above ground.
2	IN	Voltage Input. IN powers the charge pump required to turn on GN1. When the correct adapter is plugged in, a one-shot turns on the internal pFET for 1.2s, allowing time for the microprocessor (µP) to power-up and drive PWR_HOLD high. Bypass IN with a minimum 1µF ceramic capacitor as close as possible to the device for ±15kV ESD protection. When operating the MAX4919B/MAX4920B/MAX4921B with an external pFET at GP1, place the 1µF capacitor to GND as close to the drain of the pFET as possible for the ±15kV ESD protection. If ±15kV ESD protection is not required, place a minimum 0.1µF capacitor at IN to GND.
3	GN1	n-Channel MOSFET Gate-Drive Output. GN1 is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$, GN1 is driven above the source voltage to turn on the external n-channel MOSFET.
4, 5	BTI	Battery Switch Input. BTI powers the internal circuitry. Bypass BTI with a 0.1µF capacitor. Both BTI inputs must be externally connected together.
6	HP_PWR	Car-Kit Detection Input**.** When a car kit is plugged into HP_PWR, a one-shot turns on the internal pFET for 1.2s, allowing time for the µP to power-up and drive PWR_HOLD high.
7	PWR_ON	Power-On Input. Drive PWR_ON high to turn on the internal pFET. The inverse of the PWR_ON logic state is represented at the $\overline{ONOK}$ logic output.
8	GND	Ground
9	$\overline{ONOK}$	Open-Drain PWR_ON Indicator Output. $\overline{ONOK}$ is a logic output with the inverse state of the PWR_ON input.
10, 11	BTO	Battery Switch Output. Both BTO outputs must be externally connected together.
12	PWR_HOLD	Power-Hold Input. Drive PWR_HOLD high to turn on internal pFET.
13	$\overline{ACOK}$	Open-Drain Adapter Voltage Indicator Output. $\overline{ACOK}$ pulls low when the adapter voltage is stable between UVLO and OVLO for 25ms. Connect a pullup resistor from $\overline{ACOK}$ to a logic supply.
14	$\overline{EN}$	Enable Input. Drive $\overline{EN}$ low for normal operation. Drive $\overline{EN}$ high to turn off the external MOSFETs and enter shutdown mode.
EP	—	Exposed Paddle. Connect EP to ground.

Detailed Description

Undervoltage Lockout (UVLO)

The MAX4919B/MAX4920B have a 4.27V (typ) undervoltage threshold (UVLO), while the MAX4921B has 2.35V (typ) UVLO threshold. When V_{IN} is less than UVLO, GN1 is held low and $\overline{ACOK}$ is high impedance.

Overvoltage Lockout Thresholds (OVLO)

The MAX4919B has a 6.38V (typ) overvoltage threshold (OVLO), the MAX4920B has a 5.8V (typ) typical OVLO, and the MAX4921B has a 4.65V (typ) OVLO. When V_{IN} is greater than OVLO, GN1 is held low and $\overline{ACOK}$ is high impedance.

Powering the MAX4919B/ MAX4920B/MAX4921B

BTI powers the MAX4919B/MAX4920B/MAX4921B internal circuitry. BTI also connects internally to a 1.8A (min) pFET that conducts an external load to the battery using the BTO output. See the *Battery Switchover* section.

GP1 Driver

When the input voltage goes above ground, GP1 pulls low and turns on the pFET. An internal clamp protects the pFET by insuring that the GP1 to IN voltage does not exceed 19.5V when the input (IN) rises to 28V.

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

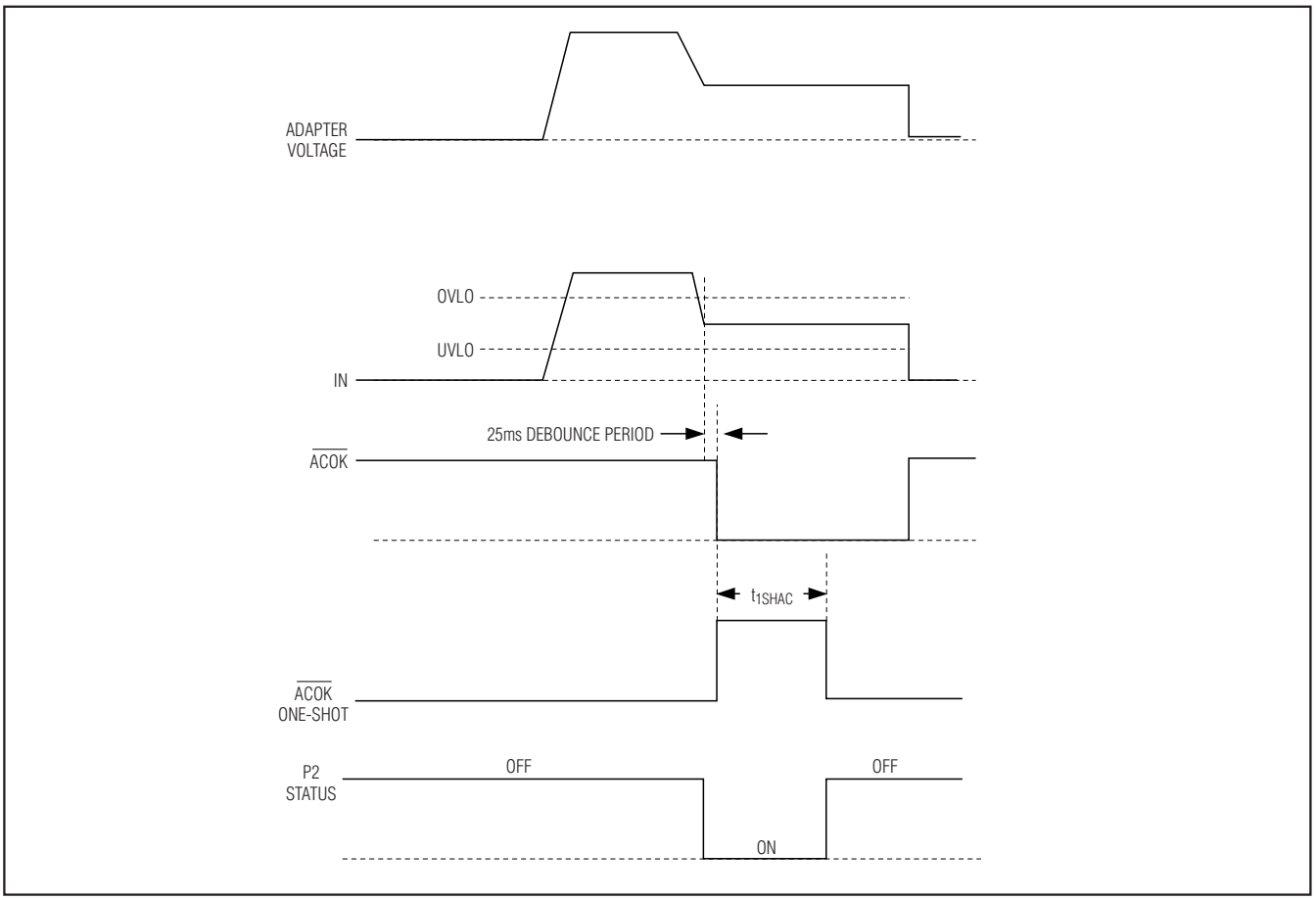


Figure 1. $\overline{ACOK}$ One-Shot Timing Diagram

GN1 Driver

An internal 5.5V supply powers the on-chip charge pump used to drive GN1 above IN, allowing the use of a low-cost nFET. The GN1 voltage is approximately two times V_{IN} until V_{IN} exceeds 5.5V, at which point, GN1 clamps to 9.5V (MAX4919B/MAX4920B) or 8.1V (MAX4921B).

$\overline{ACOK}$

$\overline{ACOK}$ is an active-low open-drain output that asserts when $V_{UVLO} < V_{IN} < V_{OVLO}$ for the 25ms debounce period. $\overline{ACOK}$ deasserts immediately to overvoltage and undervoltage faults. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system.

PWR_ON

PWR_ON is one of the logic inputs that enables the internal 1.8A switch. Drive PWR_ON high to turn on the internal switch. PWR_ON also controls the logic output $\overline{ONOK}$. The $\overline{ONOK}$ open-drain output is the inverse of the PWR_ON input state (see Figure 5). Note that $\overline{ONOK}$ is high impedance when $V_{IN} < V_{UVLO}$, and $V_{BTI} < 2.82V$ (typ). If V_{BTI} is greater than 2.15V (typ), but less than 2.82V (typ), PWR_ON and $\overline{ONOK}$ are disabled and $\overline{ONOK}$ pulls high. When BTI rises above 2.82V (typ) again, PWR_ON is again enabled and $\overline{ONOK}$ goes back to its previous logic level before a low condition at BTI (see Figure 6).

Battery Switchover

An internal 1.8A (min) pFET with a 100mΩ (typ) R_{ON} connects BTI to the load at BTO. The internal battery switchover FET turns on when either HP_PWR, PWR_ON, or PWR_HOLD is high. Note that when BTI < 2.15V, the internal switch remains inactive, regardless of the logic control signals.

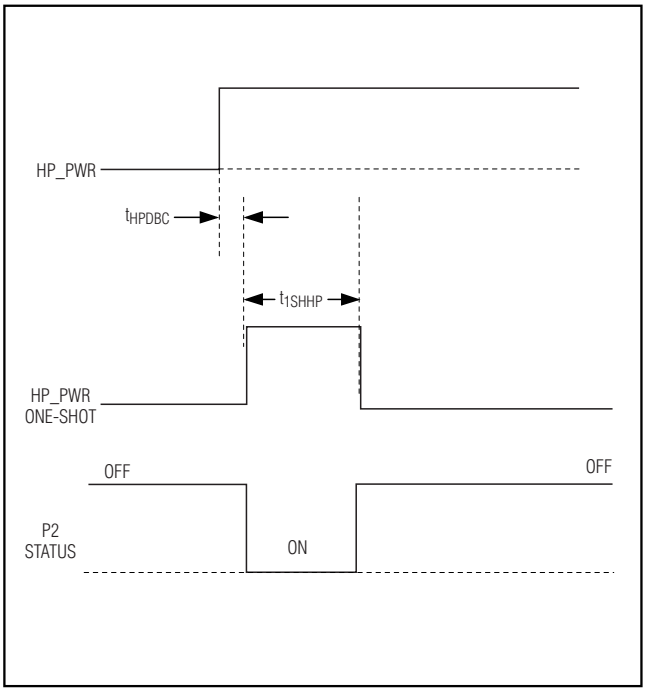


Figure 2. HP_PWR One-Shot Timing Diagram

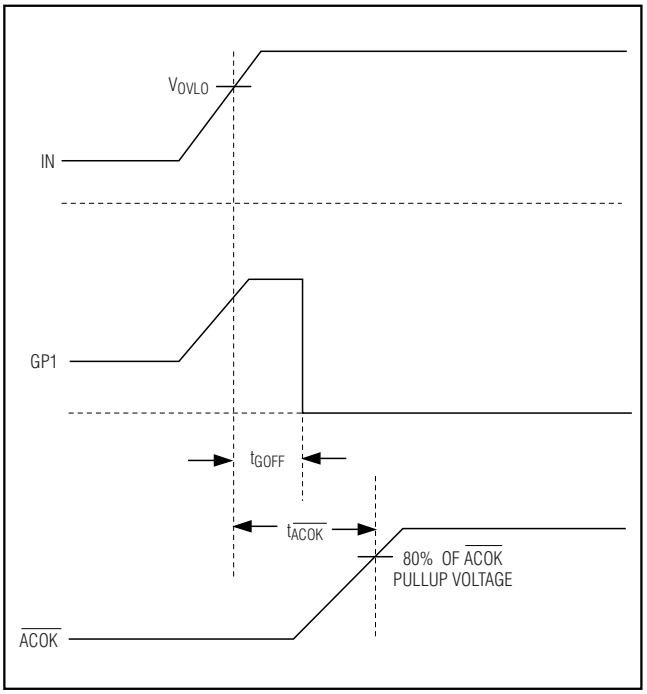


Figure 3. $\overline{ACOK}$ Assertion Delay Timing Diagram

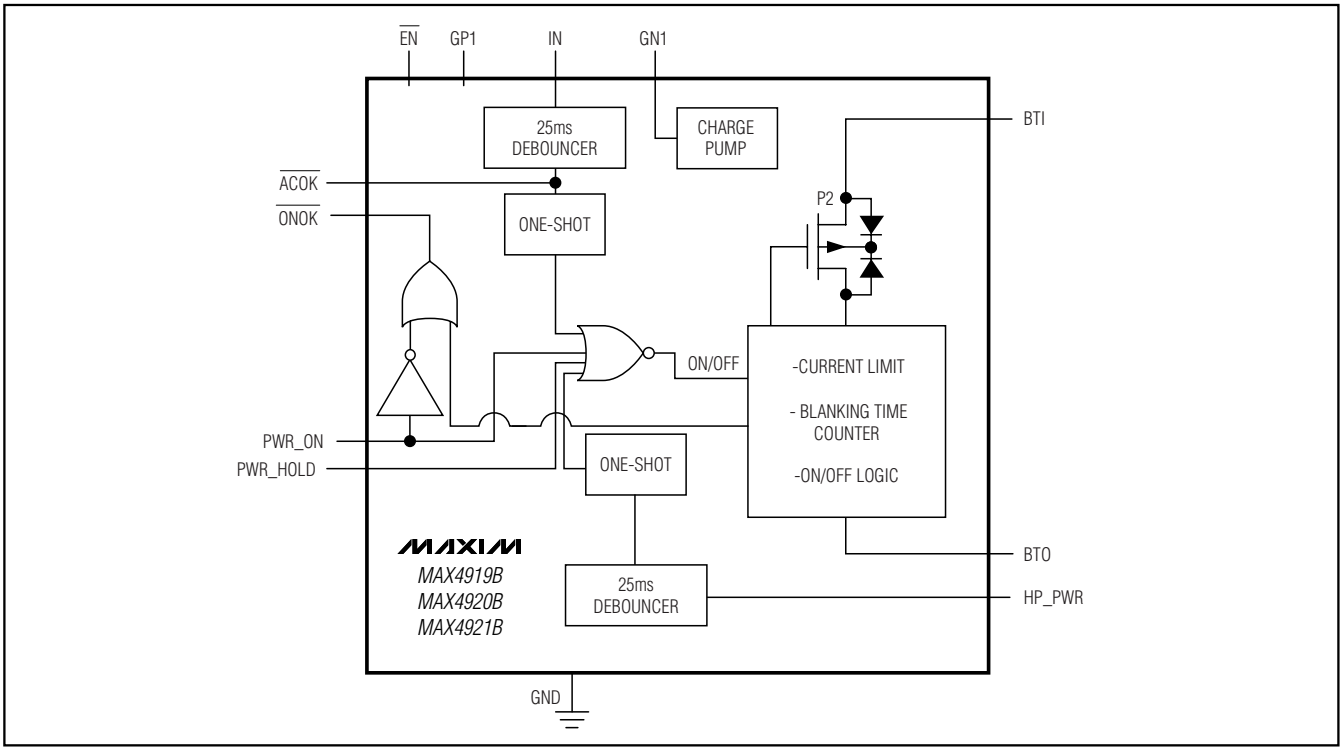


Figure 4. Functional Diagram

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

PWR_HOLD

PWR_HOLD controls the turn-on of the 1.8A (min) current-limit switch (P2). When a voltage is present at IN, and $V_{UVLO} < V_{IN} < V_{OVLO}$ for 25ms, $\overline{ACOK}$ pulls low and issues an internal one-shot pulse that turns on P2 temporarily for 1.2s (typ). During the 1.2s one-shot period, the MAX4919B/MAX4920B/MAX4921B must see a low-to-high transition at PWR_HOLD (and PWR_HOLD must remain high), for P2 to remain on (see Figure 7). P2 turns off when PWR_HOLD and PWR_ON are low, and when the HP_PWR and $\overline{ACOK}$ internal one-shot timers have expired.

When a voltage at IN is not present, HP_PWR controls the turn-on of P2. Upon a low-to-high transition at HP_PWR (and HP_PWR remaining high), the MAX4919B/MAX4920B/MAX4921B issue an internal HP_PWR one-shot signal that turns on P2 temporarily for 1.2s (typ). During the 1.2s one-shot period, the MAX4919B/MAX4920B/MAX4921B must see a low-to-high transition at PWR_HOLD (and PWR_HOLD must remain high) for P2 to remain on. P2 turns off when PWR_HOLD and PWR_ON are low, and when the HP_PWR and $\overline{ACOK}$ internal one-shot timers have expired (see Figure 8).

Current Limiting

The MAX4919B/MAX4920B/MAX4921B feature an internal 1.8A (min) current-limiting switch (P2) at BTO. The current limit remains in effect throughout BTI's input supply-voltage range.

The current limit takes care of two situations: when P2 is initially turned on, and when P2 is already on and a short circuit occurs (see Figure 9). When P2 is turned on, the current can be high because BTO = 0 and a large load capacitor needs to be charged. The protection circuit prevents the load current from exceeding the 1.8A (min) current-limit value, and BTO will have a smooth turn-on (the larger the capacitor, the slower the turn-on). The 10ms blanking time avoids a false fault assertion. At the end of the blanking time, if the device is still limiting, a fault is asserted and P2 immediately turns off. When the switch is already on and a short-circuit condition occurs at BTO, the device limits the current. If the fault condition duration is greater than the blanking time, P2 turns off.

Before P2 turns on again, any condition that is attempting to turn it on must be first removed, i.e. the one-shot (from IN or HP_PWR) must be completed, and PWR_ON and PWR_HOLD must be low. If the three conditions are satisfied, P2 turns on again only if either IN or PWR_HOLD is cycled OFF and ON.

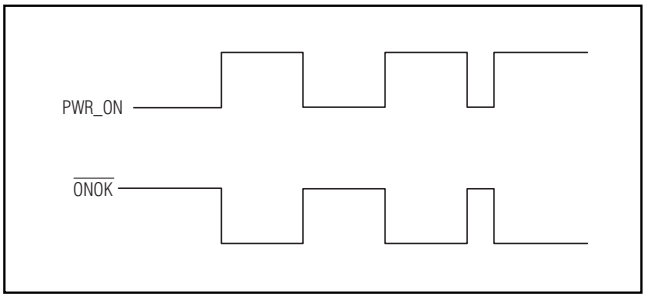


Figure 5. $\overline{ONOK}$ Timing Diagram

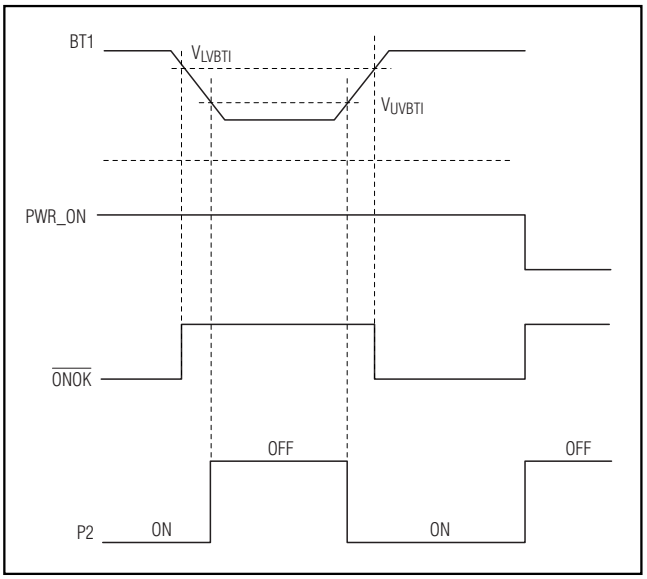


Figure 6. BTI Falling and Rising Above Its Thresholds

Low-Battery Operation

The MAX4919B/MAX4920B/MAX4921B operate in low-battery mode when the battery voltage at BTI is greater than 2.15V but less than 2.8V (typ). In low-battery operation, PWR_ON does not influence the behavior of the internal switch.

When an adapter and car kit are not present, the internal switch is typically controlled by PWR_HOLD. If PWR_ON is high ($\overline{ONOK}$ is low) and BTI falls below 2.8V, $\overline{ONOK}$ pulls high, but the internal switch remains on since PWR_HOLD is high. If PWR_ON is high and PWR_HOLD is low when V_{BTI} falls below the 2.8V threshold, the internal switch turns off immediately. Upon BTI rising above 2.8V again, PWR_ON is again enabled and $\overline{ONOK}$ goes back to its previous logic level before a low condition at BTI occurred.

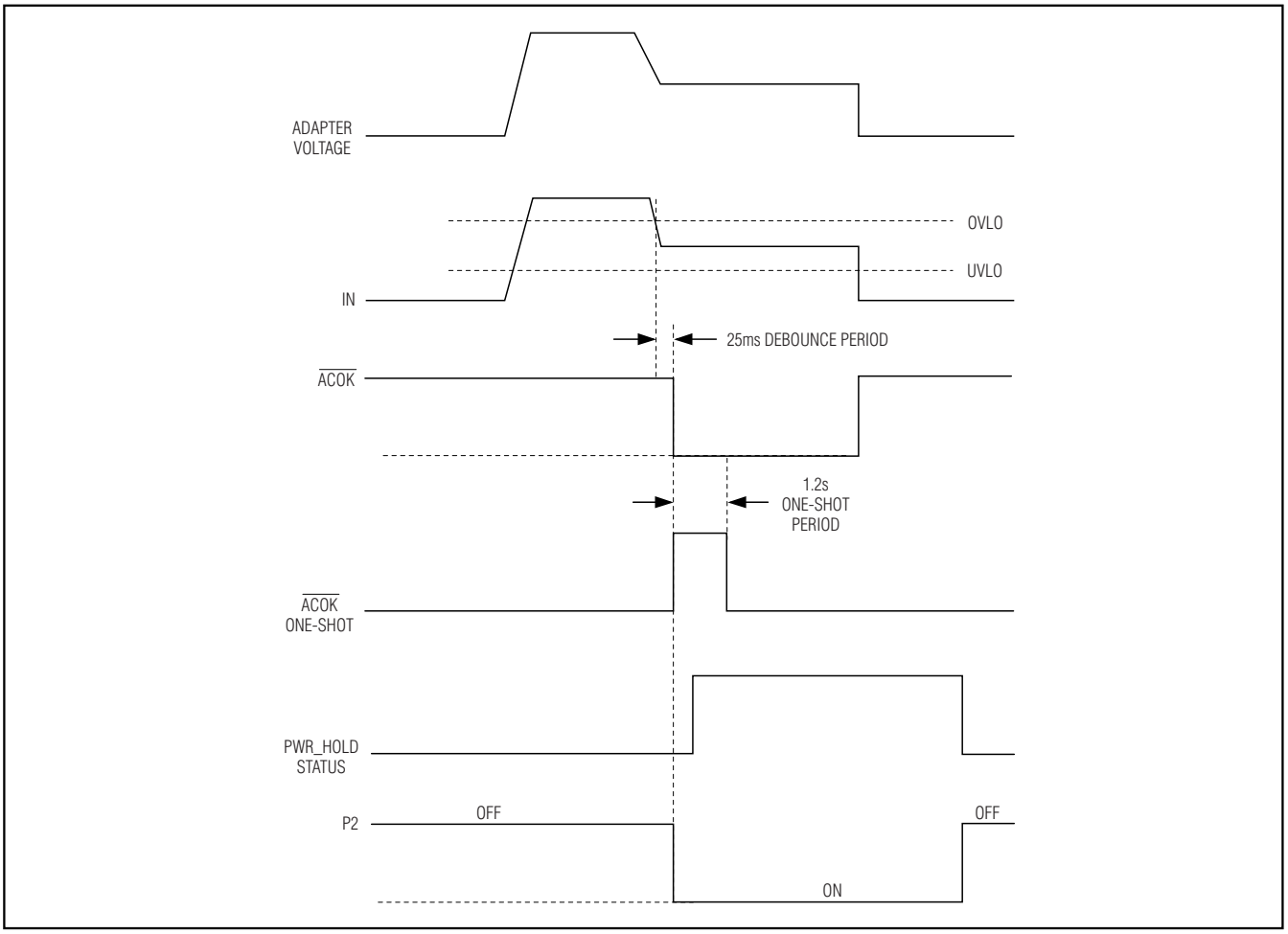


Figure 7. MAX4919B/MAX4920B/MAX4921B Power_Hold Waveform When Voltage at IN is Present

Note that upon V_{BTI} falling below the 2.15V (min) threshold, the internal switch remains off, irrespective of the control signals at HP_PWR, PWR_ON, or PWR_HOLD.

Thermal Shutdown

The MAX4919B/MAX4920B/MAX4921B feature thermal shutdown circuitry. The internal 1.8A (min) switch turns off when the junction temperature exceeds +135°C and immediately goes into a fault mode. The device can be reset upon the junction temperature dropping below +125°C. Before P2 can be turned on again, any condition that is attempting to turn it on must be first removed, i.e., the one-shot (from IN or HP_PWR) must be completed, and PWR_ON and PWR_HOLD must be low. If the three conditions are satisfied, P2 turns on again only if either IN or PWR_HOLD is cycled OFF and ON.

Applications Information

MOSFET Configuration

The MAX4919B/MAX4920B/MAX4921B can drive either a single n-channel or back-to-back n-channel MOSFET (Figure 10). The back-to-back configuration will have almost zero reverse current when the adapter is not present or when the adapter voltage is below the undervoltage lockout threshold.

If reverse-current leakage is not a concern, a single n-channel MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types and is a lower cost solution. Note that if the input is actually pulled low, the output will be pulled low as well due to the parasitic body diode in the MOSFET. If this is a concern, then use the back-to-back configuration.

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V_{GS} (MAX) (V)	V_{DS} (MAX) (V)	R_{ON} at 4.5V (mΩ)	MANUFACTURER
Si5504DC	Complementary MOSFET/1206-8	±20	30	143 (N-FET)	Vishay Siliconix www.vishay.com
			-30	290 (P-FET)	
Si5902DC	Dual/1206-8	±20	30	143 (N-FET)	
Si1426DH	Single/µDFN-6	±20	30	115 (N-FET)	
Si5435DC	Single/1206-8	±20	-30	80 (P-FET)	
FDC6561AN	Dual/SSOT-6	±20	30	145 (N-FET)	Fairchild Semiconductor www.fairchildsemi.com
FDG315N	Single/µDFN-6	±20	30	160 (N-FET)	
FDC658P	Single/SSOT-6	±20	-30	75 (P-FET)	
FDC654P	Single/SSOT-6	±20	-30	125 (P-FET)	

MOSFET Selection

The MAX4919B/MAX4920B/MAX4921B are designed for use with a complementary MOSFET or single p-channel and dual back-to-back n-channel MOSFETS. In most situations, MOSFETs with $R_{DS(ON)}$ specified for a V_{GS} of 4.5V will work well. Also, the V_{DS} should be 30V in order for the MOSFET to withstand the full 28V IN range of the MAX4919B/MAX4920B/MAX4921B. Table 1 shows a selection of MOSFETs which are appropriate for use.

IN Bypass Considerations

For most applications, bypass IN to GND with a 1µF ceramic capacitor to enable ±15kV ESD protection (when GP1 is not utilized). If ±15kV is not required, place a minimum 0.1µF capacitor at IN to GND. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the +30V absolute maximum rating at IN.

BTO Bypass Capacitor Considerations

In order to guarantee a successful startup of the internal p-channel MOSFET, use a capacitance lower than $C_{BTO(MAX)}$. If the load capacitance is too large, then current may not have enough time to charge the capacitance and the device assumes that there is a faulty load condition. The maximum capacitive-load value that can be driven by BTO is obtained by the following formula:

$$C_{BTO(MAX)} \le \frac{I_{LIM} \times t_{CLIM}}{V_{BTI}}$$

where C_{BTO} is the output capacitor at BTO, V_{BTI} is the battery voltage, t_{CLIM} is the minimum current-limit blanking time, and I_{CLIM} is the minimum forward current-limit value.

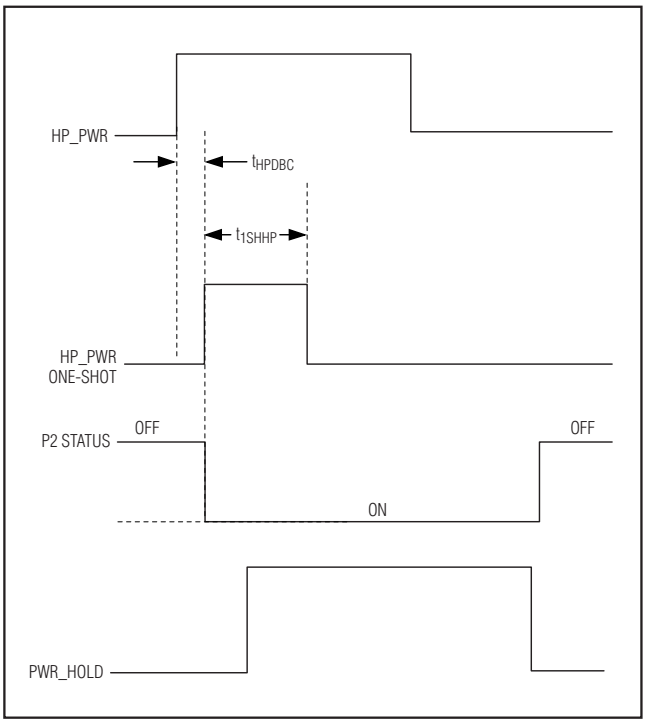


Figure 8. MAX4919B/MAX4920B/MAX4921B Power_Hold Waveform When Voltage IN is Not Present

Additional Applications Information

Adapter Application

Figures 11 and 12 depict the MAX4919B/MAX4920B being utilized in an application where the AC adapter supplies the input voltage and the car adapter is not plugged in. In this case, when the AC adapter (5V) is plugged in, the voltage at IN initially makes sure that a negative voltage is not present.

If V_{IN} remains above the UVLO and below the OVLO ranges for more than 25ms (debouncer), the n-channel MOSFET (N1) turns on and after 25ms, $\overline{ACOK}$ asserts low, then a one-shot timer starts that turns P2 on for 1.2s. During this duration, the µP needs to issue a PWR_HOLD to keep P2 on before the one-shot period expires. The adapter then powers the charger to charge the battery and the battery supports the load.

Reverse-Polarity Protection

Figure 11 shows an application where the external p-channel MOSFET is added for reverse-polarity protection. The reverse-polarity protection works by turning off the p-channel MOSFET when the adapter voltage is below ground. The p-channel MOSFET only turns off if the voltage at IN is less than the threshold voltage of the p-channel MOSFET. Due to the body diode leakage path through the external n-channel MOSFET, the reverse-polarity protection operation requires a reverse current-limited load. Figure 11 shows a battery charger as the load connected to the source of n-channel MOSFET. If the voltage at the load connection (source of the n-channel MOSFET) is greater than the drop across the n-channel MOSFET's body diode plus the p-channel MOSFET threshold voltage, then the p-channel MOSFET remains on if the adapter voltage is below ground. If the load has reverse-current protection, the voltage at the load pulls down and the p-channel MOSFET turns off limiting reverse current. If the load allows a large reverse current, then this current flows out of the adapter input and the reverse-polarity protection is defeated.

Car-Kit Application

Figures 13 and 14 illustrate the MAX4921B being utilized when the car-kit adapter, with built-in charger, is plugged in and connected directly to the battery. HP_PWR goes through a 25ms debounce period and then a 1.2s one-shot is issued.

During this one-shot period, the µP needs to issue a PWR_HOLD to keep P2 on before the one-shot period expires. The car kit then charges the battery and the battery supports the load. Note that the reverse-polarity protection p-channel MOSFET cannot be used in this application due to the direct connection of the battery to the source of the n-channel MOSFET.

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

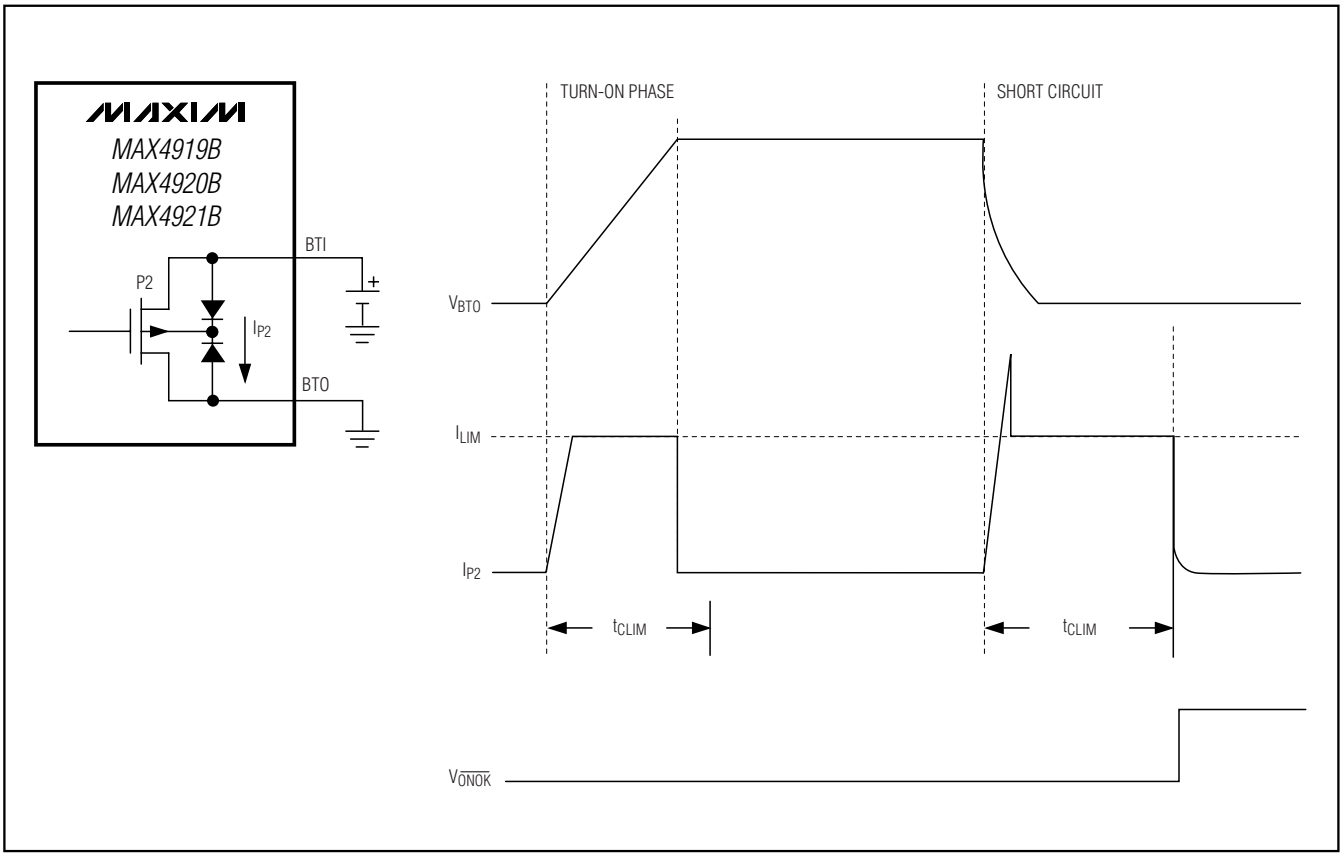


Figure 9. MAX4919B/MAX4920B/MAX4921B Current-Limit Diagram

Chip Information

PROCESS: BiCMOS

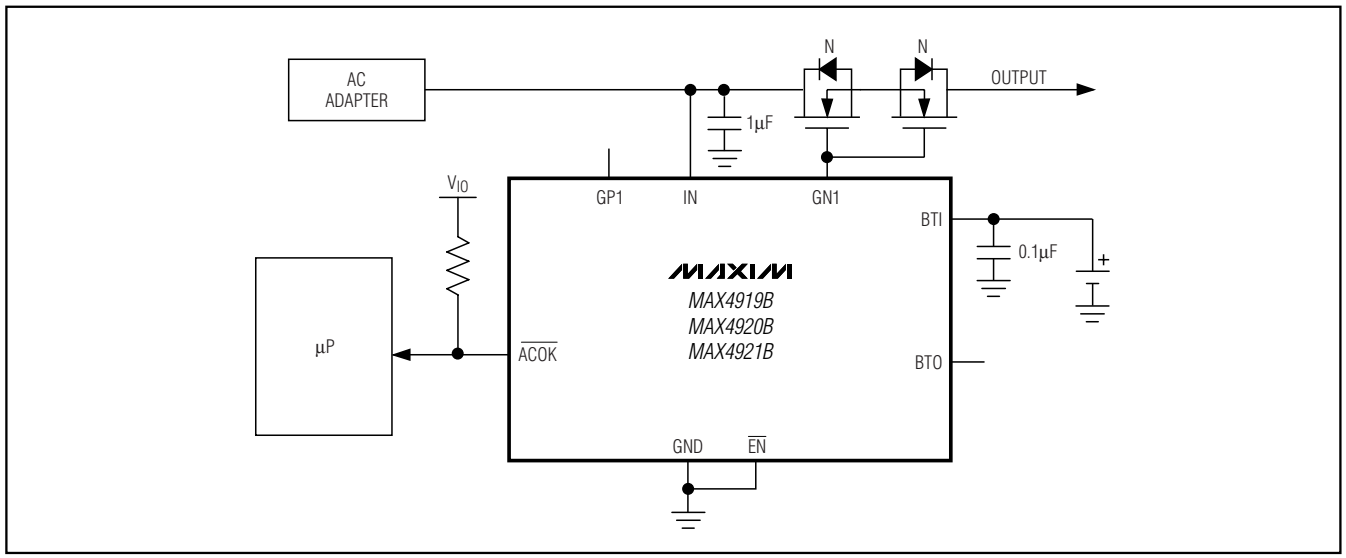


Figure 10. Back-to-Back External MOSFET Configuration

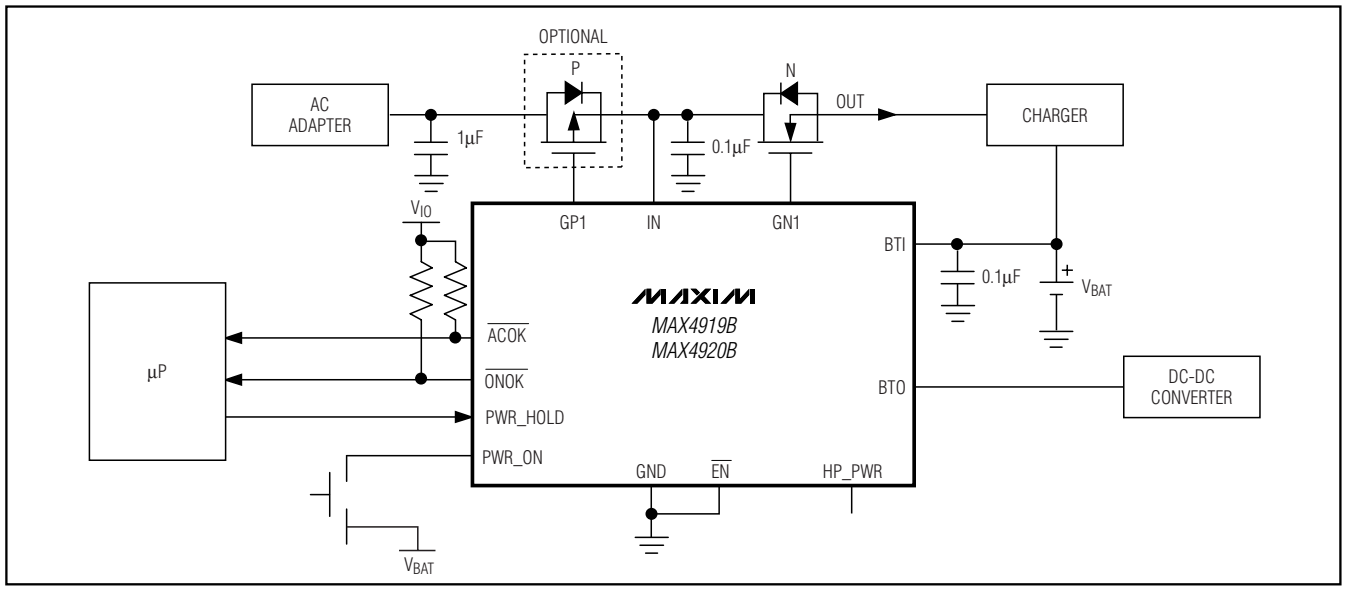


Figure 11. MAX4919B/MAX4920B Always Powered From Battery (Car-Kit Adapter Never Plugged In)

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

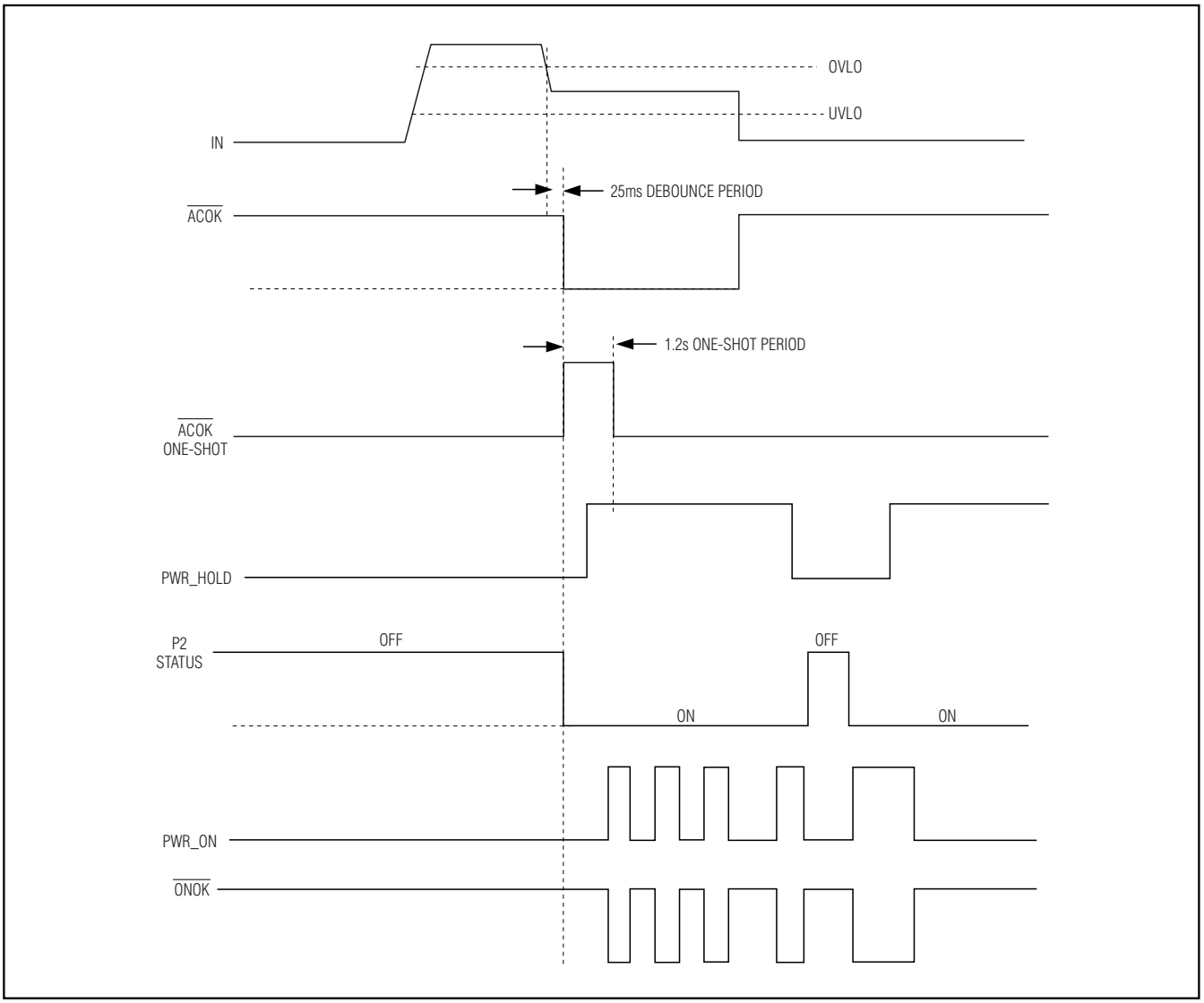


Figure 12. MAX4919B/MAX4920B Timing Diagram For Non-Car-Kit Adapter Application

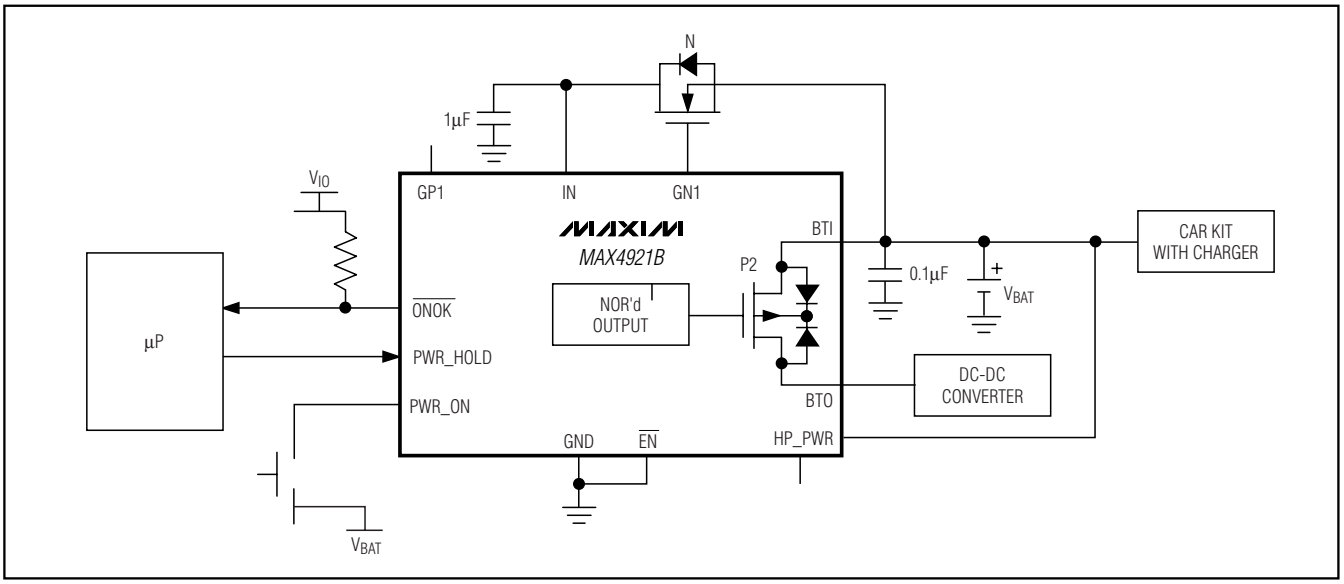


Figure 13. MAX4920B With Car-Kit Adapter and Built-In Charger Connected

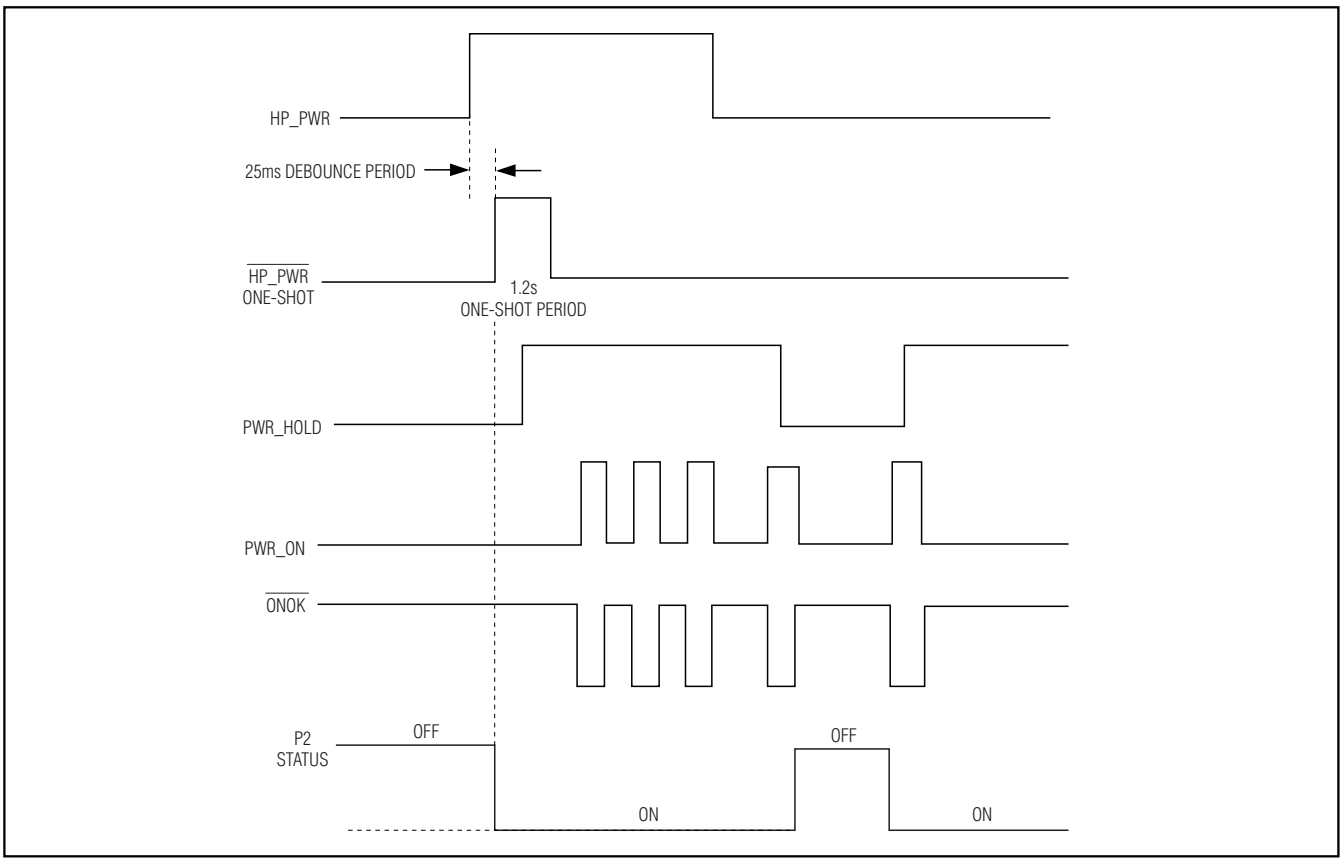
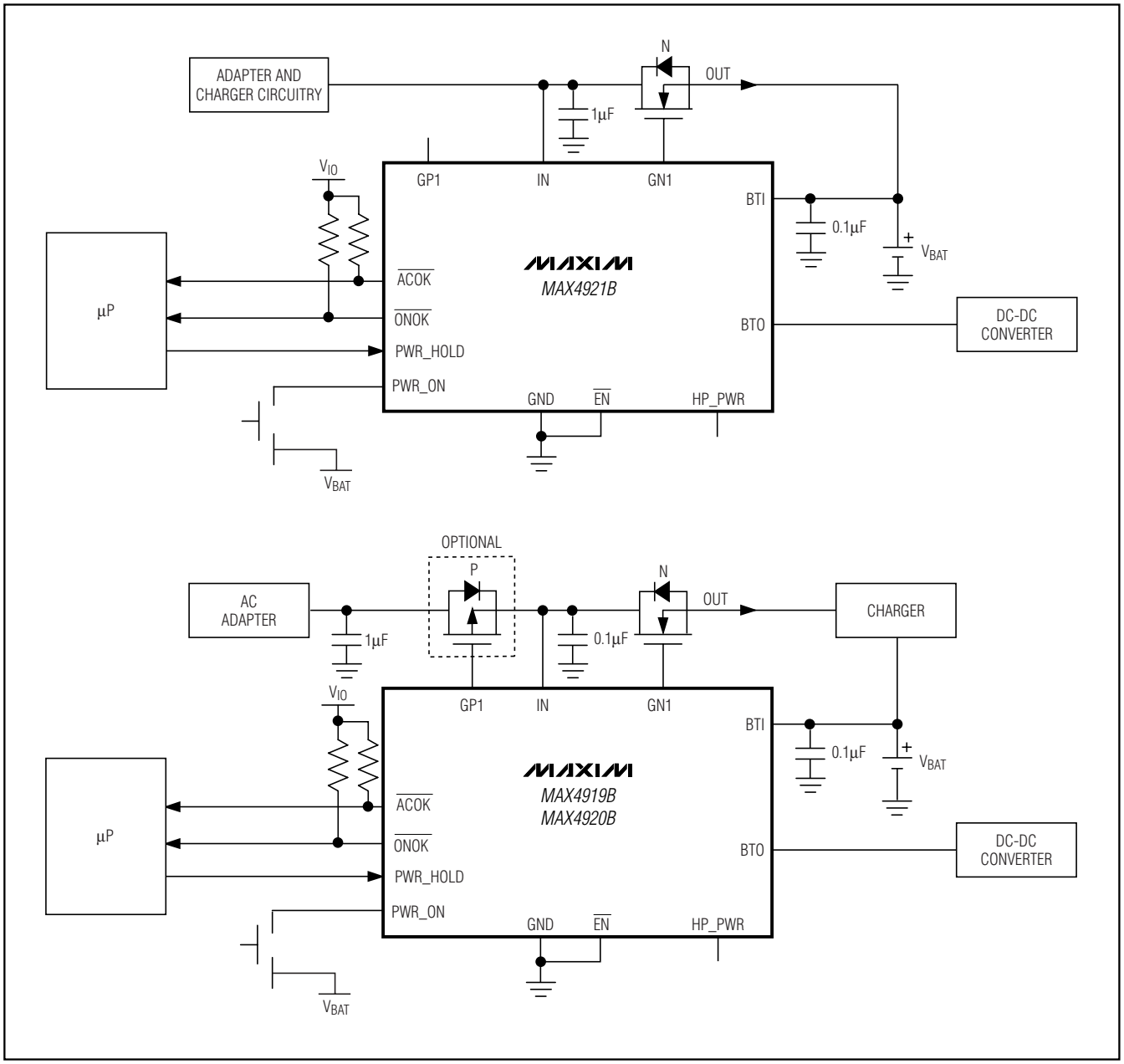


Figure 14. Timing Diagram For Car-Kit Adapter Application

Battery Power-Up Logic with Overvoltage and Overcurrent Protection

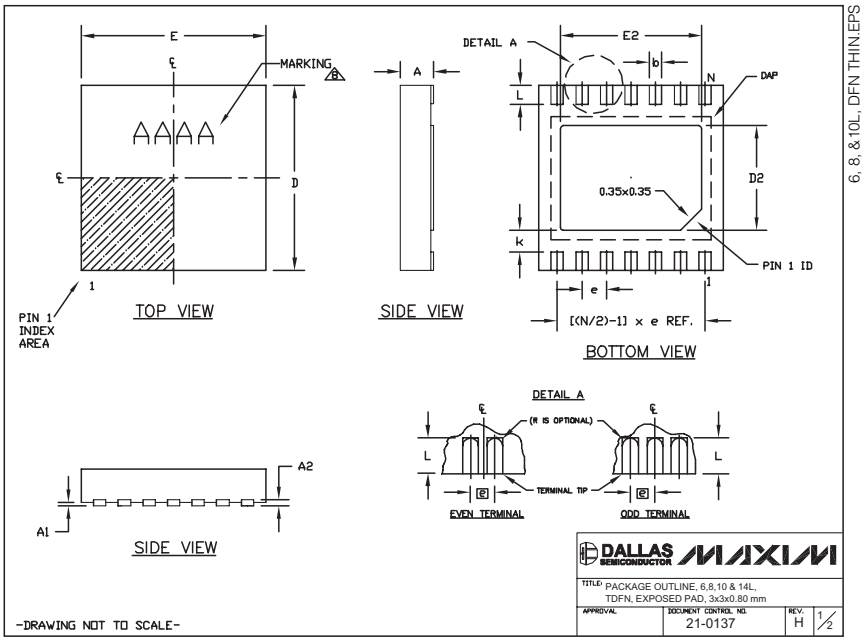
Typical Operating Circuits



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, & 10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1033-2	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. H
2/2

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