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H-Bridge Driver and Pulse Width Controller for Digital Camera Micro Modules

DESCRIPTION

The SiP42104 is a 250 mA integrated H-bridge driver and programmable output-pulse-width controller. It offers a complete and cost-effective solution for micro camera focus module applications such as shutter, iris, lens cover and Infrared filter drivers. The output voltage direction of the H-bridge is set by the presence of the rising or falling edge at the digital interface pin IN and the corresponding on-duration is set by the RC pin time constant. During time-out, the input deglitcher-latch is transparent to input noise durations of less than 300 ns. Internal breakbefore-make prevents output shoot-through. When the H-bridge turns off after time-out, the lower N-channel MOSFETs are turned on for a short interval to prevent turning on their body diodes. The low IN threshold logic and the sub micro-amp steady state quiescent current is ideal for low battery applications.

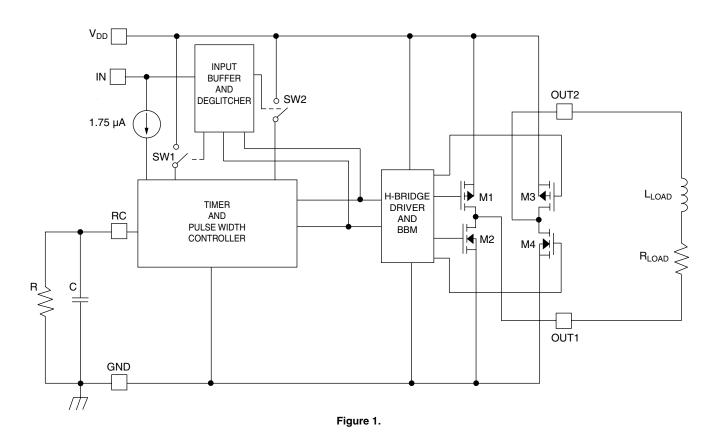
The SiP42104 is offered in the ultra-small lead (Pb)-free SC-89 package (SOT666) and it is rated over the industrial ambient range of - 40 $^{\circ}$ C to + 85 $^{\circ}$ C.

FEATURES

- Low supply range: 2.3 to 4.2 V
- Low R_H : 0.85 Ω at 2.8 V and 150 mA
- Output current up to 250 mA
- Output voltage direction depends on input Rising or falling edges
- · Break before make cross-over protection
- 300 ns de-glitch circuit
- · Programmable RC timer to set output pulse width
- Sub micro-amp guiescent current
- SC89-6L package (1.6 x 1.6 x 0.6 mm)

APPLICATIONS

- Digital camera
- Cell phones
- Small DC motor control
- Dual-stage latchable relay driver



Document Number: 74633 S-80224-Rev. C, 04-Feb-08

TYPICAL APPLICATION CIRCUIT





COMPLIANT

SiP42104

Vishay Siliconix

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ABSOLUTE MAXIMUM RATINGS				
Parameter	Limit	Unit		
Supply Input Voltage (V _{DD})	- 0.3 to 4.5			
Input Voltage (V _{IN})	- 0.3 to 4.5	V		
Output DC Voltage (V _{OUT1} , V _{OUT2})	- 0.3 to 4.5			
Maximum Pulsed Current (I _{OUT1} , I _{OUT1})	250	mA		
ESD Rating (HBM)	5.5	kV		
Thermal Resistance ^a (θ _{JA})	465	°C/W		
Power Dissipation ^b (P _D)	172	mW		
Maximum Junction Temperature (T _{JM})	150			
Lead Temperature ^c (T _L)	260	°C		
Storage Temperature (T _S)	- 65 to 150			

Notes:

a. Soldered down to PCB 1 inch² 1 oz copper.

b. Derate - 2.15 mW/°C above 70 °C.

c. Soldering 5 s.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE					
Parameter	Limit	Unit			
V _{DD}	2.3 to 4.2	V			
I _{OUT}	± 150	mA			
Timing Resistor	10 K to 500 K	Ω			
Timing Capacitor	10 to 220	nF			
Output Inductive Load L	10 to 550	μH			
DCR Of Output Inductive Load	15 to 30	Ω			



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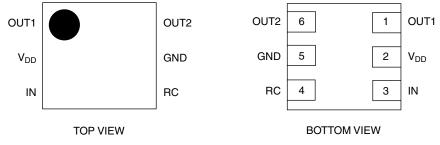
SPECIFICATIONS							
Parameter	Symbol	Test Conditions V_{DD} = 2.8 V, T_A = - 40 to 85 °Cunless otherwise noted.Typical values are at T_A = 25 °C	Temp.	Min. ^a	Typ. ^b	Max. ^a	Unit
H-Bridge Section							
Supply Voltage Range	V _{DD}		Full	2.3		4.2	V
Operating Current	I _{DDQ}	IN = RC = 0 V	Full			5	μA
H-Bridge Resistance ^c	R _H	I _{OUT} = 150 mA	Full		0.85	1.6	Ω
RC Time-out Voltage	V1	Falling edge set by RC	Room	670	756	840	
Fast Discharge Voltage	V2	Falling edge set by R ₁ C	Room	480	644	730	mV
RC Pulse Width	T _{RC}	R = 500 K, C = 100 nF	Room		65		ms
IN Logic High	V _{THI}	Rising, M1/M4 on	Full	1.6			
IN Logic Low	V _{TLO}	Falling, M1/M4 off	Full		0.82	0.5	V
Hysteresis	V _{HYS}	V _{THI} - V _{TLO}	Full		0.28		
IN Pull- Down current	I _{PD}	$V_{IN} = V_{DD}$	Room		1.75		μA
Break-Before-Make	T _{BBM}		Room		50		ns
Trigger Edges	T _{EDGE}	Input rise and fall	Room		< 0.1		
Trigger Pulse Duration	T _{IN}	Input minimum pulse width	Room		≥2		μs
Trigger Response Time	T _{RT}	Delay from IN to output	Room		0.6		

Notes:

a. The algebraic convention whereby the most negative value is a minimum and most positive is a maximum.b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

c. R_H is the $R_{DS(ON)}$ of M1 + M4 or M2 + M3.

PIN CONFIGURATION



SC89 PACKAGE

Figure 2.

PIN DESCRIPTION	I	
Pin Number	Name	Function
1	OUT1	H-Bridge Output 1
2	V _{DD}	Supply Voltage
3	IN	Input Edge Trigger Direction Control. Positive Edge Sets OUT1 High and OUT2 Low. Negative Edge Sets OUT2 High and OUT1 Low.
4	RC	Pulse Width Timing Setting
5	GND	Ground Connection
6	OUT2	H-Bridge Output 2

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ORDERING INFORMATION

Part Number	Marking	Temperature Range	Package		
SiP42104DX-T1-E3 ^b	HL ^a	- 40 °C to 85 °C	SC89-6L (SOT666)		

Notes:

a. "H" is part identifier and "L" is lot and date code identifier.

b. T1 Tape and Reel orientation with pin1 bottom left hand corner of cavity.

FUNCTIONAL BLOCK DIAGRAM

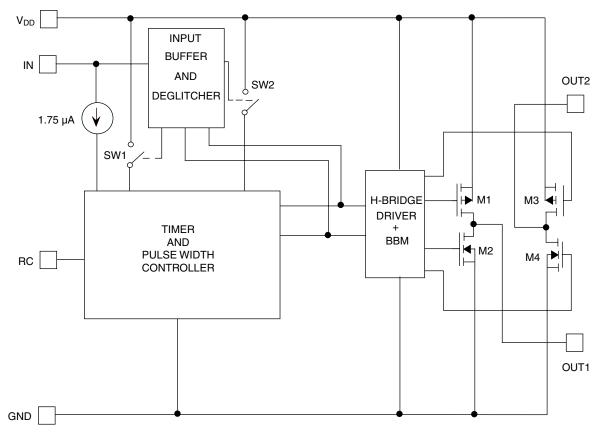
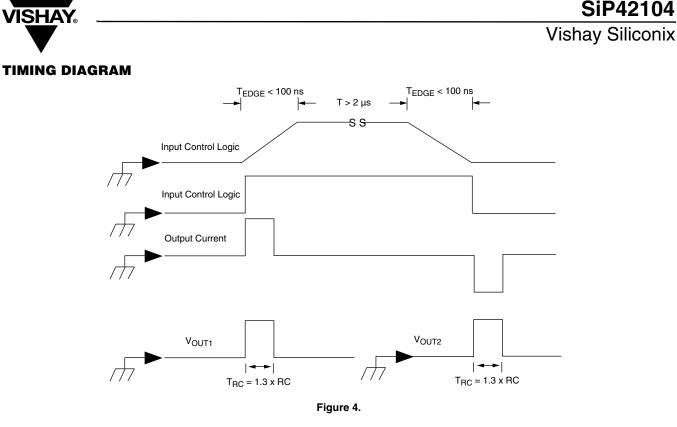


Figure 3.



DETAILED OPERATIONAL DESCRIPTION

SiP42104 is an easy to use integrated H-bridge driver and programmable output pulse width controller IC intended for digital camera micro module focus mode applications. The IC is designed to drive a solenoid of several hundred micro-Henrys and operates over the supply range of 2.3 to 4.2 V. Both H-bridge output can source and sink up to 250 mA. The break-before-make delays prevents shoot-through via M1 to M2 or M3 to M4 in the H-bridge and is guaranteed by design.

In the absence of any edge transitions at the input pin, the IC is in the power-down mode with the H-bridge outputs at high impedance drawing only sub micro-amp of leakage current from the supply.

The input pin is CMOS logic level and has typical 1.75 µA pull-down current, the input pin is buffered by a Schmitt trigger with the threshold level of 1.1 V and typical hysteresis of 280 mV. A logic transition closes SW2 and initiates the H-Bridge output turn-on for duration set by the external RC time constant. The logic level transition is latched in the device and this logic level transition determines which of the H-Bridge output MOSFETs turns on. If the logic transition is rising from ground to V_{DD}, with the high condition being present for at least 2 µs, then M1 and M4 will turn on, M2 and M3 will turn off. This means that OUT1 will go high and OUT2 will go low. Conversely, a falling logic transition is from V_{DD} to ground, with the low level being present for 2 µs, will turn on M2 and M3. M1 and M4 will turn off. Once the input transition is latched, SiP42104 will ignore any input spurious transition until the RC pin time out is completed. An internal deglitch filter following the input buffer prevents SiP42104 from being accidentally triggered by the input pulse less than 300 ns duration.

Document Number: 74633 S-80224-Rev. C, 04-Feb-08 A positive edge transition on the input pin also initiates SiP42104 to charge the RC pin to V_{DD} via SW1. This pre-charge period lasts for approximately 30 µs. When the pre-charge period is completed, SW1 will turn off and the external capacitor begins to discharge via the external resistor. The timer and pulse width controller sense the voltage on RC pin. When the voltage on the RC pin falls to V1 (0.27 x V_{DD}). The timer and pulse width controller terminate the timeout and turn off the relevant H-bridge outputs. This yields and output pulse width given by:

T_{OUTPUT} = 1.3 x RC

SiP42104 H-bridge output typically drives an inductive load. When output are turned off after the RC timeout, the current will still be flowing in the inductive load. To prevent the load current from forward biasing the body diodes of the output MOSFETs, both H-bridge low-side MOSFETs M2 and M4 will turn on briefly to allow the inductive load current to discharge to zero. When the voltage on the RC pin has fallen to V2 (0.23 x V_{DD}). This yields a discharge time:

$$\Gamma_{\text{DISCHARGE}} = 0.13 \times C \times R1$$

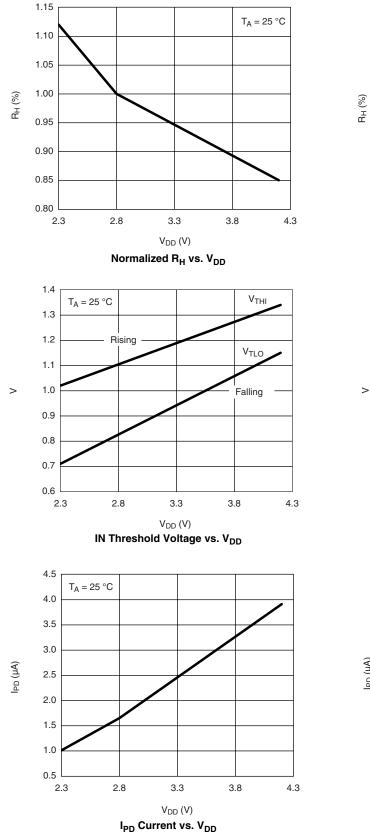
Where R1 is the built-in resistor of 1.1 k Ω .

Following this discharge time period, SW2 and all H-bridge output MOSFETs are turned off. SiP42104 powers down to its low quiescent current state. SiP42104 will remain in this state until the next input transition logic applied to the input pin to wake up.

SiP42104

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TYPICAL CHARACTERISTICS

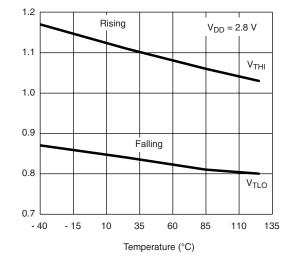


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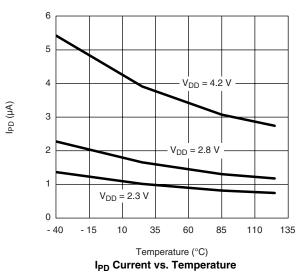
1.3

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Temperature (°C) Normalized R_H vs. Temperature



IN Threshold Voltage vs. Temperature



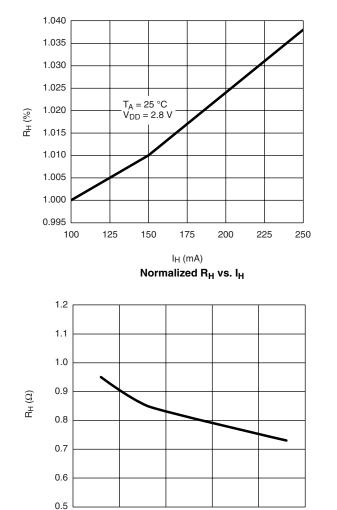
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SiP42104

Vishay Siliconix

TYPICAL CHARACTERISTICS



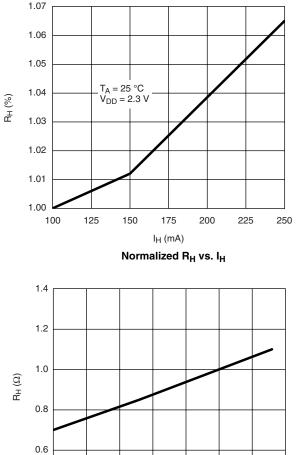
3.5

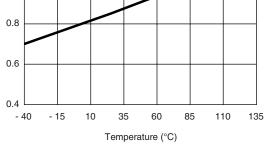
V_{DD} (V)

R_H vs. V_{DD}

4.0

4.5





R_H vs. Temperature

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2.0

2.5

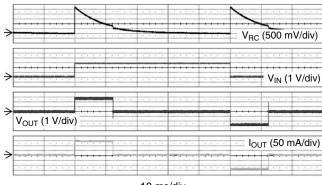
3.0

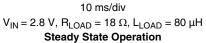
SiP42104

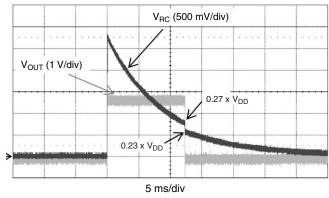
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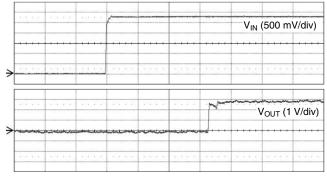
TYPICAL WAVEFORMS



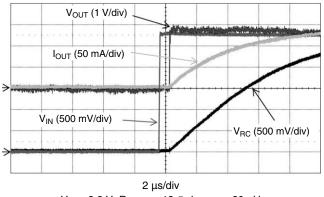


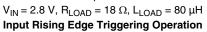


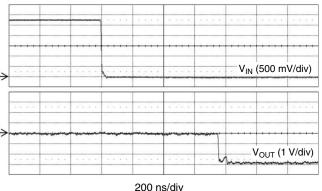
$$\label{eq:VIN} \begin{split} V_{IN} = 2.8 \ V, \ R_{LOAD} = 18 \ \Omega, \ L_{LOAD} = 80 \ \mu H \\ \textbf{RC Threshold Voltage} \end{split}$$



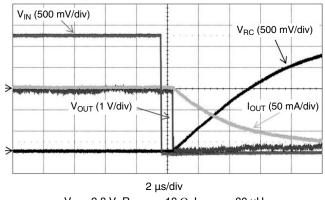
 $200 \text{ ns/div} \\ V_{IN} = 2.8 \text{ V}, \text{ R}_{LOAD} = 18 \ \Omega, \text{ } L_{LOAD} = 80 \ \mu\text{H} \\ \text{Input Rising Edge Trigger Response Time} \\$







 $V_{\text{IN}} = 2.8 \text{ V}, \text{ } \text{R}_{\text{LOAD}} = 18 \ \Omega, \text{ } \text{L}_{\text{LOAD}} = 80 \ \mu\text{H}$ Input Falling Edge Trigger Response Time



 $V_{IN} = 2.8 \text{ V}, \text{ R}_{LOAD} = 18 \Omega, \text{ L}_{LOAD} = 80 \mu\text{H}$ Input Falling Edge Triggering Operation

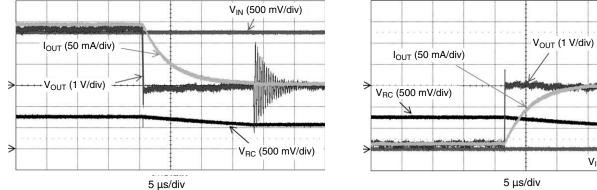


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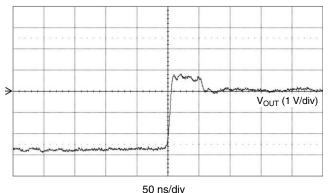
V_{IN} (500 mV/div)

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TYPICAL WAVEFORMS



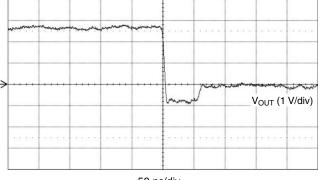
 V_{IN} = 2.8 V, R_{LOAD} = 18 Ω , L_{LOAD} = 80 μ H Inductive Discharge OUT2 to OUT1



 $V_{\text{IN}} = 2.8 \text{ V}, \text{ R}_{\text{LOAD}} = 18 \ \Omega, \text{ L}_{\text{LOAD}} = 80 \ \mu\text{H}$

Inductive Discharge OUT1 to OUT2

 $V_{\text{IN}} = 2.8 \text{ V}, \text{ R}_{\text{LOAD}} = 18 \ \Omega, \text{ L}_{\text{LOAD}} = 80 \ \mu\text{H}$ **Rising Edge T_{BBM}**



 $50 \text{ ns/div} \\ V_{IN} = 2.8 \text{ V}, \text{ R}_{LOAD} = 18 \ \Omega, \text{ L}_{LOAD} = 80 \ \mu\text{H} \\ \textbf{Falling Edge T}_{BBM}$

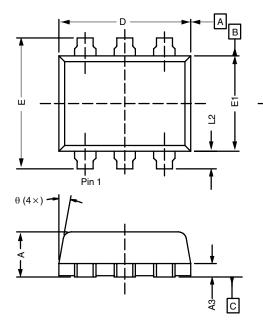
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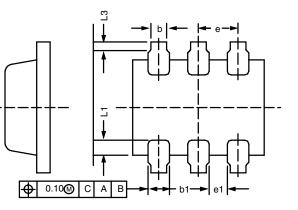
Document Number: 74633 S-80224-Rev. C, 04-Feb-08



Package Information Vishay Siliconix

SC-89: 6-LEAD (SOT-666)





NOTES:

- 1. All dimensions are in millimeters.
- 2. Package outline exclusive of mold flash and metal burr.
- 3. Package outline inclusive of plating.
- 4. Maximum webbing flash remain 0.075 mm.

	МІ		RS*	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.56	-	0.60	0.022	-	0.024	
A3	0.13	0.17	0.18	0.005	0.006	0.007	
b	0.17	-	0.25	0.006	-	0.010	
b1	-	0.27	0.34	-	0.011	0.013	
D	1.50	1.66	1.70	0.059	0.065	0.067	
E	1.50	1.65	1.70	0.059	0.065	0.067	
E1	1.10	1.20	1.30	0.043	0.047	0.051	
е	e 0.50 BSC			0.020 BSC			
e ₁	0.20	-	-	0.008	-	_	
L1	0.11	0.19	0.26	0.004	0.007	0.010	
L2	0.10	0.23	0.30	0.004	0.009	0.012	
L3	0.05	0.10	-	0.002	0.004	-	
θ	8°	10°	12°	8°	10°	12°	
ECN: S-52444—Rev. D, 28-Nov-05							

DWG: 5891

*Use millimeters as the primary measurement



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