International
IOR Rectifier

May 9, 2008

IRS2336(D)
IRS23364D

HIGH VOLTAGE 3 PHASE GATE DRIVER IC

Features

- Drives up to six IGBT/MOSFET power devices
- Gate drive supplies up to 20 V per channel
- Integrated bootstrap functionality (IRS2336(4)D)
- Over-current protection
- Over-temperature shutdown input
- Advanced input filter
- Integrated deadtime protection
- Shoot-through (cross-conduction) protection
- Undervoltage lockout for V_{CC} & V_{BS}
- Enable/disable input and fault reporting
- Adjustable fault clear timing
- Separate logic and power grounds
- 3.3 V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Matched propagation delays for all channels
- -40°C to 125°C operating range
- RoHS compliant
- Lead-Free

Product Summary

Topology		3 Phase
V_{OFFSET}		≤ 600 V
V_{OUT}	IRS2336(D)	10 V – 20 V
	IRS23364D	11.5 V – 20 V
I_{o+} & I_{o-} (typical)		200 mA & 350 mA
t_{ON} & t_{OFF} (typical)		530 ns & 530 ns
Deadtime (typical)		275 ns

Package Options

28-Lead PDIP

28-Lead SOIC Wide Body

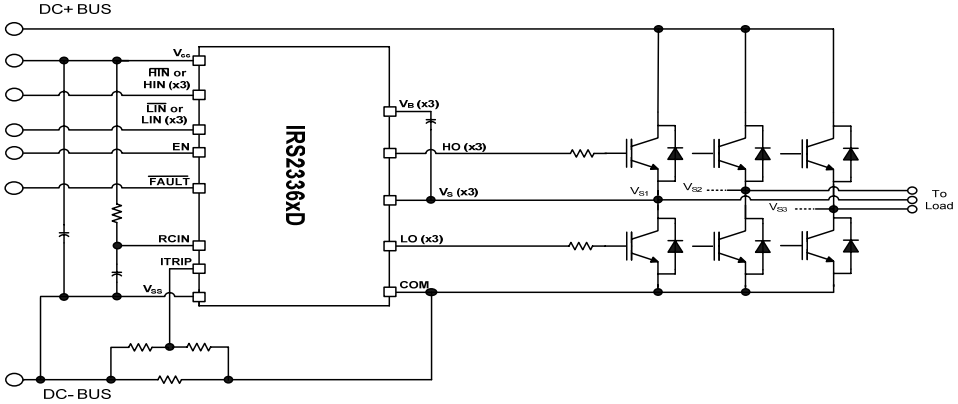
48-Lead MLPQ7X7
(without 14 leads)

44-Lead PLCC
(without 12 leads)

Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Typical Connection Diagram



© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Description

The IRS2336xD are high voltage, high speed, power MOSFET and IGBT gate drivers with three high-side and three low-side referenced output channels for 3-phase applications. This IC is designed to be used with low-cost bootstrap power supplies; the bootstrap diode functionality has been integrated into this device to reduce the component count and the PCB size. Proprietary HVIC and latch immune CMOS technologies have been implemented in a rugged monolithic structure. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3 V logic). A current trip function which terminates all six outputs can be derived from an external current sense resistor. Enable functionality is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that a fault (e.g., over-current, over-temperature, or undervoltage shutdown event) has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Shoot-through protection circuitry and a minimum deadtime circuitry have been integrated into this IC. Propagation delays are matched to simplify the HVIC's use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high-side configuration, which operate up to 600 V.

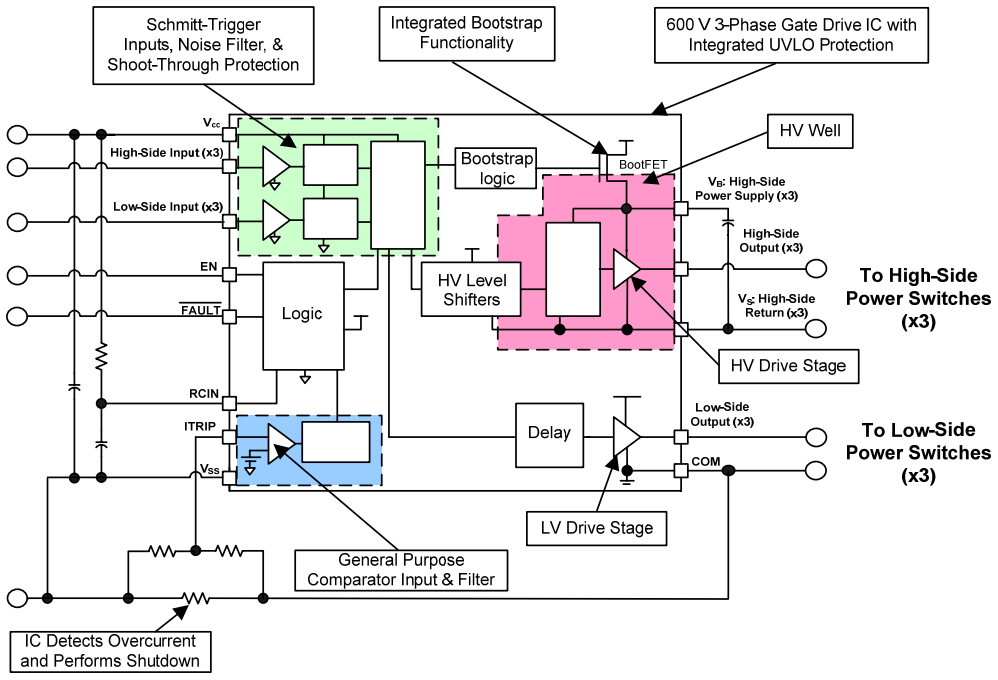
Feature Comparison: IRS2336xD Family

Part Number	Input Logic	UVLO	$V_{IT,TH}$	t_{ON}, t_{OFF}	V_{OUT}
IRS2336(D)	HIN/N, LIN/N	8.9 V/ 8.2 V	0.46 V	530 ns, 530 ns	10 V – 20 V
IRS23364D	HIN, LIN	11.1 V/ 10.9 V	0.46 V	530 ns, 530 ns	11.5 V – 20 V

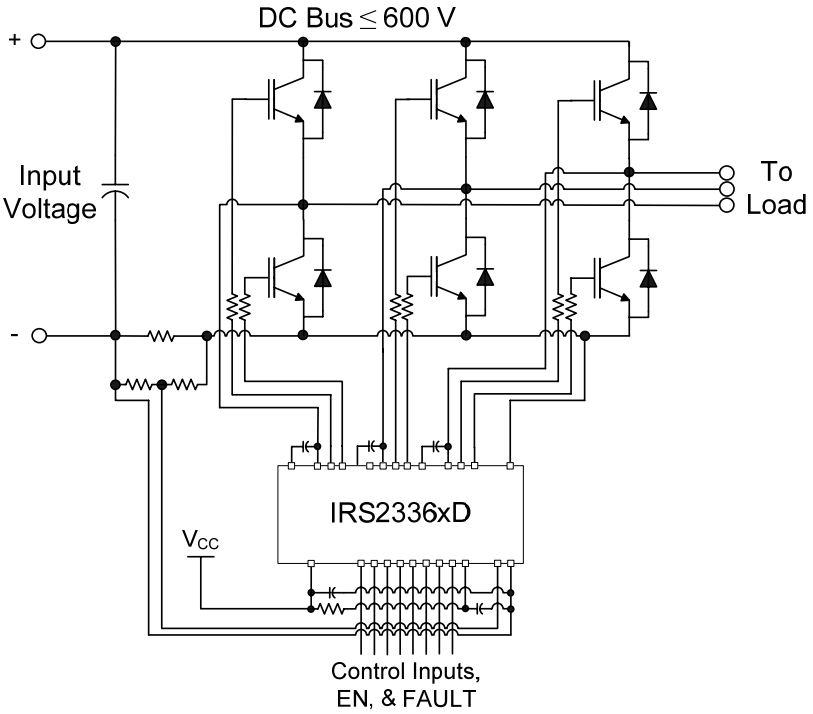
© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Simplified Block Diagram



Typical Application Diagram



© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC28W	MSL3†††, 260°C (per IPC/JEDEC J-STD-020)
		MLPQ7X7	
		PLCC44	MSL3†††, 245°C (per IPC/JEDEC J-STD-020)
		PDIP28	Not applicable (non-surface mount package style)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
	Charged Device Model ††††	Class IV (per JEDEC standard JESD22-C101)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† Charged Device Model classification is based on SOIC28W package.

© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20 V), and V_B & V_S (20 V).

Symbol	Definition		Min	Max	Units
V_{CC}	Low side supply voltage		-0.3	20†	V
V_{IN}	Logic input voltage (HIN, LIN, ITRIP, EN)	IRS2336(D)	V_{SS}-0.3	V_{SS}+5.2	
		IRS23364D	V_{SS}-0.3	V_{CC}+0.3	
V_{RCIN}	RCIN input voltage		V_{SS}-0.3	V_{CC}+0.3	
V_B	High-side floating well supply voltage		-0.3	620†	
V_S	High-side floating well supply return voltage		V_B-20†	V_B+0.3	
V_{HO}	Floating gate drive output voltage		V_S-0.3	V_B+0.3	
V_{LO}	Low-side output voltage		COM-0.3	V_{CC}+0.3	
V_{FLT}	Fault output voltage		V_{SS}-0.3	V_{CC}+0.3	
COM	Power ground		V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Allowable V_S offset supply transient relative to V_{SS}		—	50	V/ns
PW_{HIN}	High-side input pulse width		500	—	ns
P_D	Package power dissipation @ $T_A \leq +25°C$	28-Lead PDIP	—	1.5	W
		28-Lead SOICW	—	1.6	
		44-Lead PLCC	—	2.0	
		48-Lead MLPQ7X7	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	28-Lead PDIP	—	83	°C/W
		28-Lead SOICW	—	78	
		44-Lead PLCC	—	63	
		48-Lead MLPQ7X7	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are tested at 25 V. An internal 20 V clamp exists for each supply.

© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC}-COM) = (V_B-V_S) = 15 V.

Symbol	Definition		Min	Max	Units
V_{CC}	Low-side supply voltage	IRS2336(D)	10	20	V
		IRS23364D	11.5	20	
V_{IN}	HIN, LIN, & EN input voltage	IRS2336(D)	V_{SS}	V_{SS}+5	
		IRS23364D		V_{CC}	
V_B	High-side floating well supply voltage	IRS2336(D)	V_S+10	V_S+20	
		IRS23364D	V_S+11.5	V_S+20	
V_S	High-side floating well supply offset voltage†		COM-8	600	
V_S(t)	Transient high-side floating supply voltage††		-50	600	
V_{HO}	Floating gate drive output voltage		V_s	V_B	
V_{LO}	Low-side output voltage		COM	V_{CC}	
COM	Power ground		-5	5	
V_{FLT}	FAULT output voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage		V_{SS}	V_{SS}+5	
T_A	Ambient temperature		-40	125	ºC

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative V_S of V_{SS} - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	IRS2336(D)	8	8.9	9.8	V	NA
		IRS23364D	10.4	11.1	11.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	IRS2336(D)	7.4	8.2	9		
		IRS23364D	10.2	10.9	11.4		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	IRS2336(D)	0.3	0.7	—		
		IRS23364D	—	0.2	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	IRS2336(D)	8	8.9	9.8		
		IRS23364D	10.4	11.1	11.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	IRS2336(D)	7.4	8.2	9		
		IRS23364D	10.2	10.9	11.4		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	IRS2336(D)	0.3	0.7	—		
		IRS23364D	—	0.2	—		
I_{LK}	High-side floating well offset supply leakage		—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current		—	70	120		All inputs are in the off state
I_{QCC}	Quiescent V_{CC} supply current	IRS2336	—	2	3	mA	
		IR2336(4)D	—	3	4		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O		—	0.90	1.4	V	I_O= 20 mA
V_{OL}	Low level output voltage drop, V_O		—	0.40	0.6	V	
I_{o+}	Output high short circuit pulsed current		120	200	—	mA	V_O=0 V,V_{IN}=0 V, PW ≤ 10 µs
I_{o-}	Output low short circuit pulsed current		250	350	—		V_O=15 V,V_{IN}=5 V, PW ≤ 10 µs
V_{IH}	Logic “0” input voltage		2.5	—	—	V	NA
	Logic “1” input voltage						
V_{IL}	Logic “1” input voltage		—	—	0.8		
	Logic “0” input voltage						
$V_{IN,CLAMP}$	Input voltage clamp (HIN, LIN, ITRIP and EN)	IRS2336(D)	4.8	5.2	5.65		I_{IN} = 100 µA
I_{HIN+}	Input bias current (HO = High)	IRS2336(D)	—	150	200	µA	V_{IN} = 0 V
		IRS23364D	—	120	165		V_{IN} = 4 V
I_{HIN-}	Input bias current (HO = Low)	IRS2336(D)	—	110	150		
		IRS23364D	—	—	1		V_{IN} = 0 V
I_{LIN+}	Input bias current (LO = High)	IRS2336(D)	—	150	200		
		IRS23364D	—	120	165		V_{IN} = 4 V
I_{LIN-}	Input bias current (LO = Low)	IRS2336(D)	—	110	150		
		IRS23364D	—	—	1		V_{IN} = 0 V
$V_{RCIN,TH}$	RCIN positive going threshold		—	8	—	V	NA
$V_{RCIN,HY}$	RCIN hysteresis		—	3	—		
I_{RCIN}	RCIN input bias current		—	—	1	µA	V_{RCIN} = 0 V or 15 V
$R_{ON,RCIN}$	RCIN low on resistance		—	50	100	Ω	I = 1.5 mA

© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor

Static Electrical Characteristics (continued)

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
$V_{IT,TH+}$	ITRIP positive going threshold		0.37	0.46	0.55	V	NA
$V_{IT,TH-}$	ITRIP negative going threshold		—	0.4	—		
$V_{IT,HYS}$	ITRIP hysteresis		—	0.07	—		
I_{ITRIP+}	"High" ITRIP input bias current	IRS2336(D)	—	5	20	µA	V_{IN} = 4 V
		IRS23364D	—	5	40		
I_{ITRIP-}	"Low" ITRIP input bias current		—	—	1		V_{IN} = 0 V
$V_{EN,TH+}$	Enable positive going threshold		—	—	2.5	V	NA
$V_{EN,TH-}$	Enable negative going threshold		0.8	—	—		
I_{EN+}	"High" enable input bias current	IRS2336(D)	—	5	20	µA	V_{IN} = 4 V
		IRS23364D	—	120	165		
I_{EN-}	"Low" enable input bias current		—	—	1		V_{IN} = 0 V
$R_{ON,FLT}$	FAULT low on resistance		—	50	100	Ω	I = 1.5 mA
R_{BS}	Internal BS diode Ron (IRS2336(4)D)		—	200	—		NA

© 2008 International Rectifier

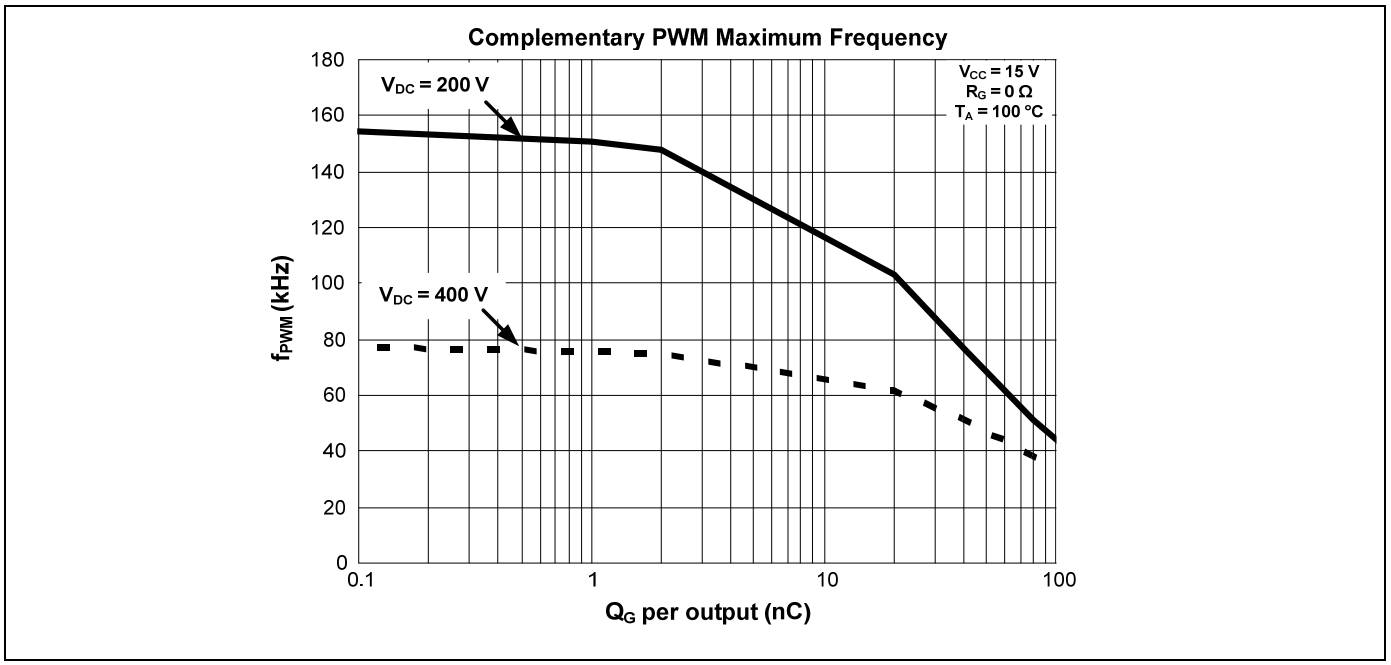
Downloaded from Elcodis.com electronic components distributor

Dynamic Electrical Characteristics

V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{ON}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0 V & 5 V
t_{OFF}	Turn-off propagation delay	400	530	750		
t_R	Turn-on rise time	—	125	190		
t_F	Turn-off fall time	—	50	75		
$t_{FIL,IN}$	Input filter time† (HIN, LIN, ITRIP)	200	350	510		
t_{EN}	Enable low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or 5 V
$t_{FILTER,EN}$	Enable input filter time	100	200	—		NA
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1200	ns	V_{ITRIP} = 5 V
t_{BL}	ITRIP blanking time	—	400	—		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	950		
DT	Deadtime	190	275	420		V_{IN} = 0 V & 5 V without external deadtime
MDT	DT matching††	—	—	60		
MT	Delay matching time (t_{ON}, t_{OFF}) ††	—	—	50		V_{IN} = 0 V & 5 V with external deadtime larger than DT
PM	Pulse width distortion†††	—	—	75		PW input=10 µs

† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.
†† This parameter applies to all of the channels. Please see the application section for more details.
††† PM is defined as PW_{IN} - PW_{OUT}.



© 2008 International Rectifier

Downloaded from Elcodis.com electronic components distributor