Features

- Single Voltage Read/Write Operation: 2.65V to 3.6V
- Access Time – 70 ns
- Sector Erase Architecture
  - Sixty-three 32K Word (64K Bytes) Sectors with Individual Write Lockout
  - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Word Program Time – 10 µs
- Fast Sector Erase Time – 100 ms
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Byte/Word in the Non-suspending Sectors by Suspending Programming of Any Other Byte/Word
- Low-power Operation
  - 10 mA Active
  - 15 µA Standby
- $\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection
- VPP Pin for Write Protection and Accelerated Program Operation
- $\overline{\text{RESET}}$ Input for Device Initialization
- Sector Lockdown Support
- TSOP and CBGA Package Options
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)

32-megabit (2M x 16/4M x 8) 3-volt Only Flash Memory

AT49BV322D
AT49BV322DT

1. Description

The AT49BV322D(T) is a 2.7-volt 32-megabit Flash memory organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 71 sectors for erase operations. The device is offered in a 48-lead TSOP and a 48-ball CBGA package. The device has $\overline{\text{CE}}$ and $\overline{\text{OE}}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “Sector Lockdown” on page 7).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory. The end of a program or an erase cycle is detected by the READY/$\overline{\text{BUSY}}$ pin, $\overline{\text{Data}}$ Polling or by the toggle bit.

The VPP pin provides data protection. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 10.0V, the program (Dual-word Program command) operation is accelerated.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Byte/Word Program) is exited by powering down the device, or by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 500 ns and then bringing it back to V_{CC}. Erase, Erase Suspend/Resume and Program Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

The $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at logic “1”, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8 - I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

7. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on V_{PP} with Respect to Ground	-0.6V to + 9.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. Protection Register Addressing Table(1)(2)(3)

Address	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
81	Factory	A	1	0	0	0	0	0	0	1
82	Factory	A	1	0	0	0	0	0	1	0
83	Factory	A	1	0	0	0	0	0	1	1
84	Factory	A	1	0	0	0	0	1	0	0
85	User	B	1	0	0	0	0	1	0	1
86	User	B	1	0	0	0	0	1	1	0
87	User	B	1	0	0	0	0	1	1	1
88	User	B	1	0	0	0	1	0	0	0

Notes:
1. All address lines not specified in the above table must be "0" when accessing the protection register, i.e., A20 - A8 = 0.
2. The addressing shown above should be used when the device is operating in the word (x16) mode.
3. In the byte (x8) mode, A-1 should be used when addressing the protection register:
   with A-1 = 0, the LSB of the address location can be accessed; and
   with A-1 = 1, the MSB of the address location can be accessed

11. DC and AC Operating Range

		AT49BV322D(T)-70
Operating Temperature (Case)	Ind.	-40°C - 85°C
V_{CC} Power Supply		2.65V to 3.6V

12. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[1]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X[2]	Ai	D_{OUT}
Program/Erase[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[4]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[2]	X	V_{IH}	X	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	V_{IH}	V_{ILPP}[5]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High-Z
Reset	X	X	X	V_{IL}	X	X	High-Z
Product Identification Software[6]				V_{IH}		A0 = V_{IL}, A1 - A20 = V_{IL}	Manufacturer Code[7]
						A0 = V_{IH}, A1 - A20 = V_{IL}	Device Code[7]

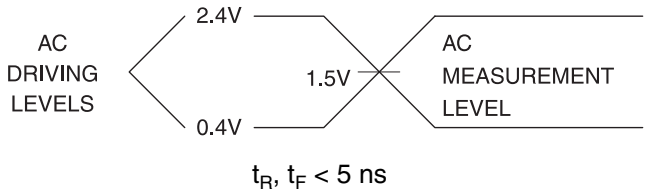
Notes:
1. The VPP pin can be tied to V_{CC}. For faster program operations, V_{PP} can be set to 9.5V ± 0.5V.
2. X can be V_{IL} or V_{IH}.
3. Refer to "Program Cycle Waveforms" on page 24.
4. V_{IHPP} (min) = 1.65V
5. V_{ILPP} (max) = 0.4V.
6. See details under "Software Product Identification Entry/Exit" on page 26.
7. Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: C8H (x8) - AT49BV322D; 01C8H (x16) - AT49BV322D; C9H (x8) - AT49BV322DT; 01C9H (x16) - AT49BV322DT.

13. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			2	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			2	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		15	25	µA
I_{CC}[(1)]	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		10	15	mA
I_{CC1}	V_{CC} Programming Current				25	mA
I_{PP1}	V_{PP} Input Load Current				10	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 1.0 mA			0.20	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA	2.5			V

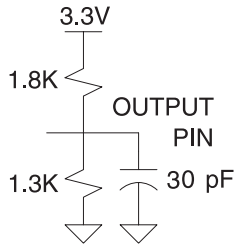
Note: 1. In the erase mode, I_{CC} is 25 mA.

14. Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

15. Output Test Load



16. Pin Capacitance

f = 1 MHz, T = 25°C[1]

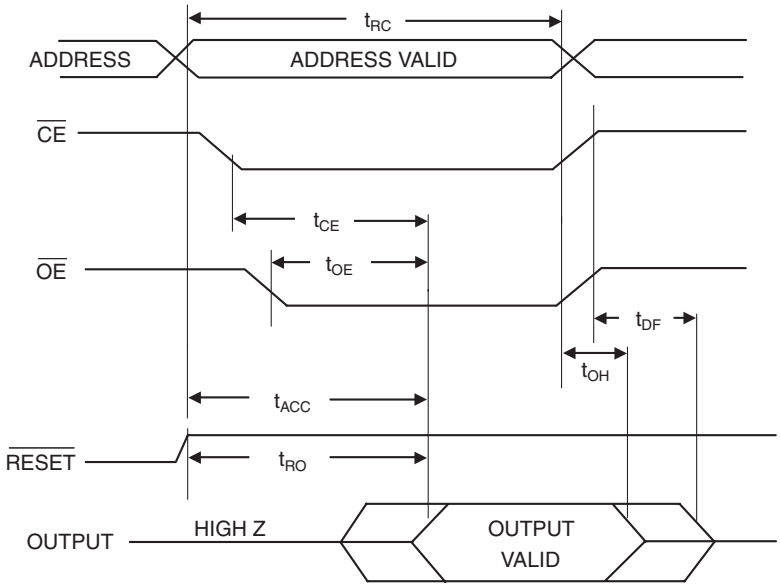
Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

17. AC Read Characteristics

Symbol	Parameter	AT49BV322D(T)-70		Units
		Min	Max	
t_{RC}	Read Cycle Time	70		ns
t_{ACC}	Address to Output Delay		70	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	20	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		100	ns

18. AC Read Waveforms[1][2][3][4]



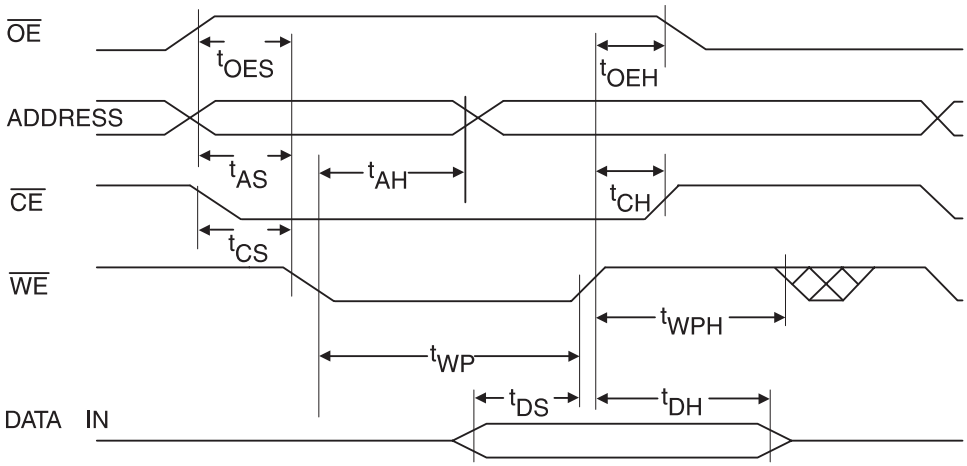
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

19. AC Byte/Word Load Characteristics

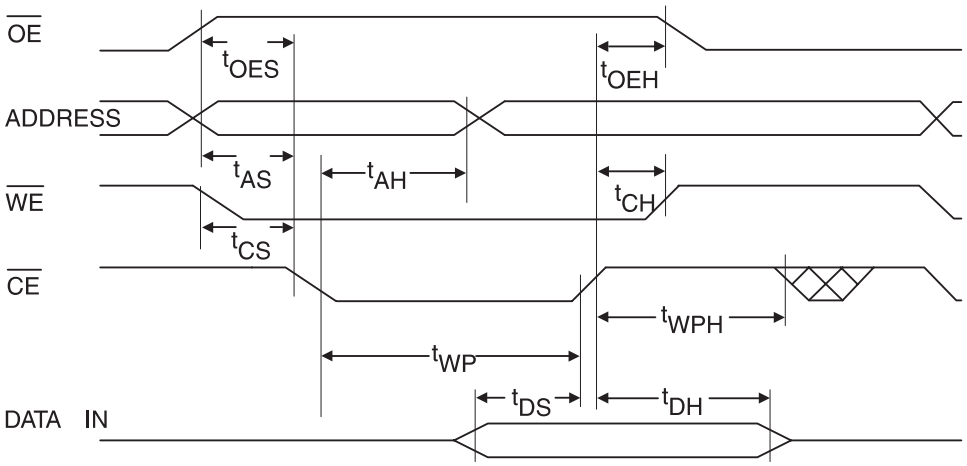
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	25		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	25		ns
t_{WPH}	Write Pulse Width High	15		ns
t_{DS}	Data Setup Time	25		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

20. AC Byte/Word Load Waveforms

20.1 $\overline{WE}$ Controlled



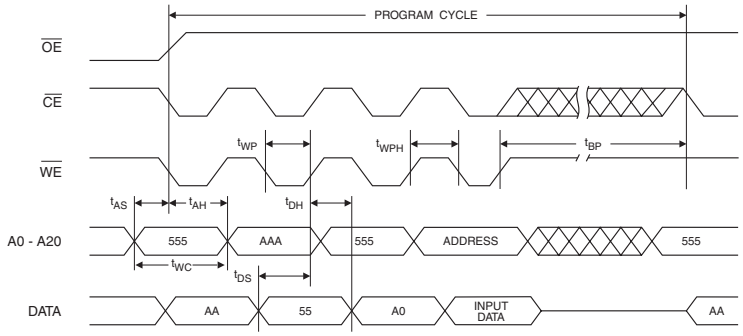
20.2 $\overline{CE}$ Controlled



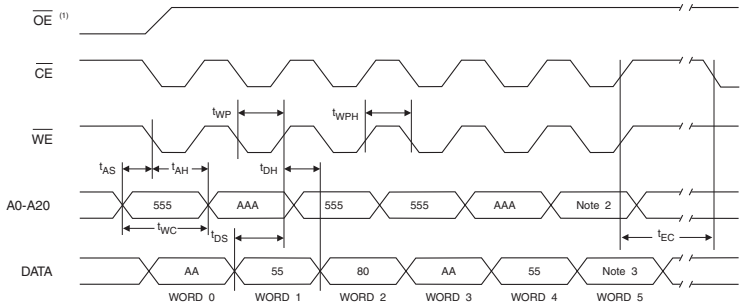
21. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		10	120	µs
t_{BPD}	Byte/Word Programming Time in Dual Programming Mode		5	60	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	25			ns
t_{DS}	Data Setup Time	25			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	25			ns
t_{WPH}	Write Pulse Width High	15			ns
t_{WC}	Write Cycle Time	70			ns
t_{RP}	$\overline{\text{Reset}}$ Pulse Width	500			ns
t_{EC}	Chip Erase Cycle Time		33		seconds
t_{SEC1}	Sector Erase Cycle Time (4K Word Sectors)		0.1	2.0	seconds
t_{SEC2}	Sector Erase Cycle Time (32K Word Sectors)		0.5	6.0	seconds
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs

22. Program Cycle Waveforms



23. Sector or Chip Erase Cycle Waveforms



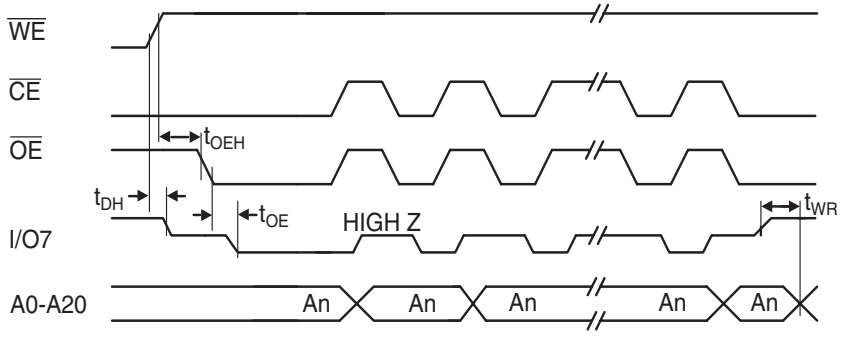
Notes:
1. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under "Command Definition Table" on page 13.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

24. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 22.

25. $\overline{\text{Data}}$ Polling Waveforms

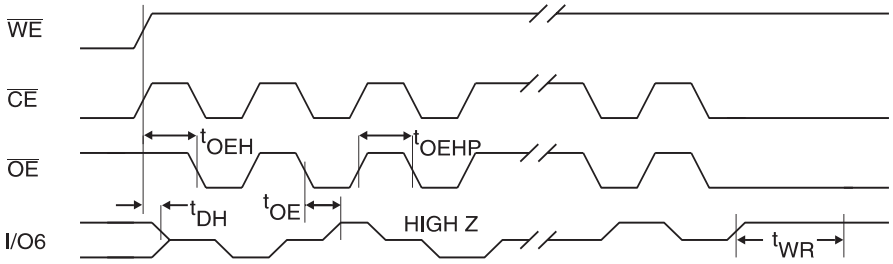


26. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 22.

27. Toggle Bit Waveforms[1][2][3]



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

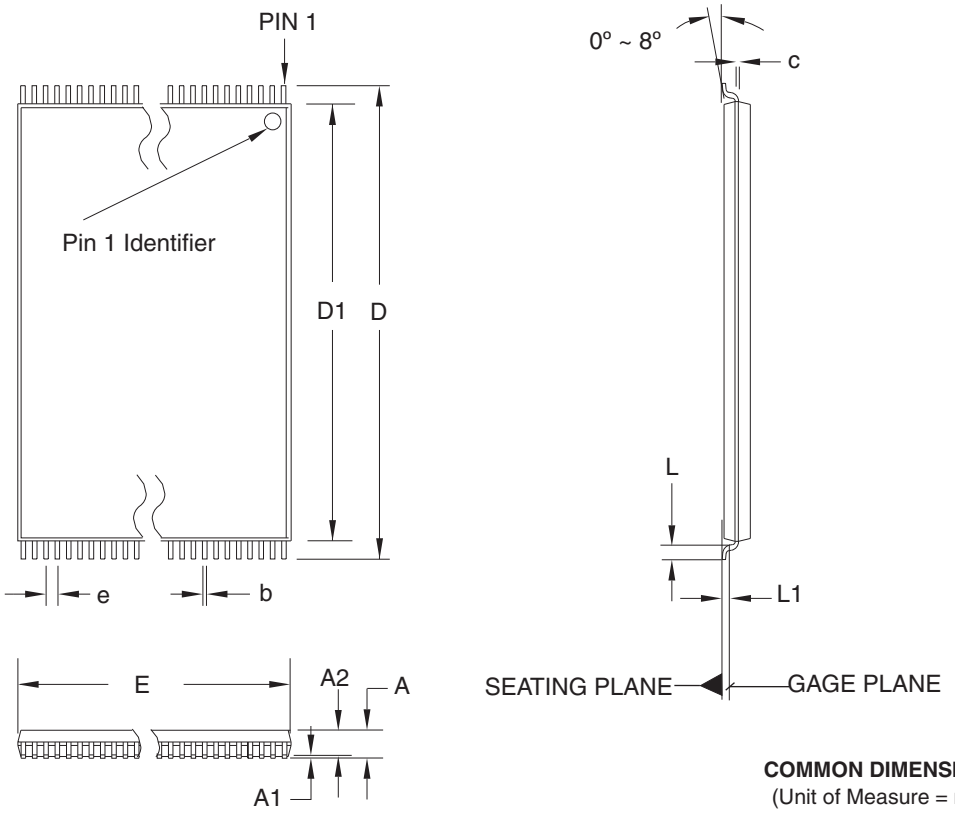
32. Ordering Information

32.1 Green Package (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	25	0.025	AT49BV322D-70CU AT49BV322D-70TU	48C17 48T	Industrial (-40° to 85°C)
70	25	0.025	AT49BV322DT-70CU AT49BV322DT-70TU	48C17 48T	Industrial (-40° to 85°C)

Package Type	
48C17	48-ball, Plastic Chip-Size Ball Grid Array Package (CBGA)
48T	48-lead, Plastic Thin Small Outline Package (TSOP)

33.2 48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	11.90	12.00	12.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48T**, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	48T	B