Dual Mobile-Friendly PWM Controller with DDR Option

The ISL6227 dual PWM controller delivers high efficiency precision voltage regulation from two synchronous buck DC/DC converters. It was designed especially to provide power regulation for DDR memory, chipsets, graphics and other system electronics in Notebook PCs. The ISL6227's wide input voltage range capability allows for voltage conversion directly from AC/DC adaptor or Li-Ion battery pack.

Automatic mode transition of constant-frequency synchronous rectification at heavy load, and hysteretic (HYS) diode-emulation at light load, assure high efficiency over a wide range of conditions. The HYS mode of operation can be disabled separately on each PWM converter if constant-frequency continuous-conduction operation is desired for all load levels. Efficiency is further enhanced by using the lower MOSFET $r_{DS(ON)}$ as the current sense element.

Voltage-feed-forward ramp modulation, current mode control, and internal feedback compensation provide fast response to input voltage and load transients. Input current ripple is minimized by channel-to-channel PWM phase shift of 0°, 90° or 180° (determined by input voltage and status of the DDR pin).

The ISL6227 can control two independent output voltages adjustable from 0.9V to 5.5V, or by activating the DDR pin, transform into a complete DDR memory power supply solution. In DDR mode, CH2 output voltage VTT tracks CH1 output voltage VDDQ. CH2 output can both source and sink current, an essential power supply feature for DDR memory. The reference voltage VREF required by DDR memory is generated as well.

In dual power supply applications the ISL6227 monitors the output voltage of both CH1 and CH2. An independent PGOOD (power good) signal is asserted for each channel after the soft-start sequence has completed, and the output voltage is within PGOOD window. In DDR mode CH1 generates the only PGOOD signal.

Built-in overvoltage protection prevents the output from going above 115% of the set point by holding the lower MOSFET on and the upper MOSFET off. When the output voltage re-enters regulation, PGOOD will go HIGH and normal operation automatically resumes. Once the soft-start sequence has completed, undervoltage protection latches the offending channel off if the output drops below 75% of its set point value. Adjustable overcurrent protection (OCP) monitors the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET. If more precise current-sensing is required, an external current sense resistor may be used.

Features

- Provides regulated output voltage in the range 0.9V to 5.5V
- Operates from an input battery voltage range of 5V to 28V or from 3.3V/5V system rail
- Complete DDR1 and DDR2 memory power solution with VTT tracking VDDQ/2 and a VDDQ/2 buffered reference output
- Flexible PWM or HYS plus PWM mode selection with HYS diode emulation at light loads for higher system efficiency
- $r_{DS(ON)}$ current sensing
- Excellent dynamic response with voltage feed-forward and current mode control accommodating wide range LC filter selections
- Undervoltage lock-out on VCC pin
- Power-good, overcurrent, overvoltage, undervoltage protection for both channels
- Synchronized 300kHz PWM operation in PWM mode
- Pb-free plus anneal available (RoHS compliant)

Applications

- Notebook PCs and Desknotes
- Tablet PCs/Slates
- Hand-held portable instruments

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6227CA*	ISL 6227CA	-10 to +100	28 Ld QSOP	M28.15
ISL6227CAZ* (Note)	ISL 6227CAZ	-10 to +100	28 Ld QSOP (Pb-free)	M28.15
ISL6227IA*	ISL 6227IA	-40 to +100	28 Ld QSOP	M28.15
ISL6227IAZ* (Note)	ISL 6227IAZ	-40 to +100	28 Ld QSOP (Pb-free)	M28.15
ISL6227HRZ* (Note)	ISL 6227HRZ	-10 to +100	28 Ld QFN (Pb-free)	L28.5x5
ISL6227IRZ* (Note)	ISL 6227IRZ	-40 to +100	28 Ld QFN (Pb-free)	L28.5x5

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . GND - 0.3V to +6.5V
Input Voltage, V_{IN} . . . . . GND - 0.3V to +28.0V
PHASE, UGATE . . . . . GND -5V (Note 1) to 33.0V
BOOT, ISEN . . . . . GND -0.3V to +33.0V
BOOT with Respect to PHASE . . . . . + 6.5V
All Other Pins . . . . . GND - 0.3V to V_{CC} + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QSOP Package (Note 2)	80	N/A
QFN Package(Notes 3, 4)	36	6

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V ± 5%
Input Voltage, V_{IN} . . . . . +5.0V to +28.0V
Ambient Temperature Range . . . . . -10°C to +100°C
Junction Temperature Range . . . . . -10°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. 250ns transient. See Confining The Negative Phase Node Voltage Swing in Application Information Section
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
5. Limits established by characterization and are not production tested.

Electrical Specifications

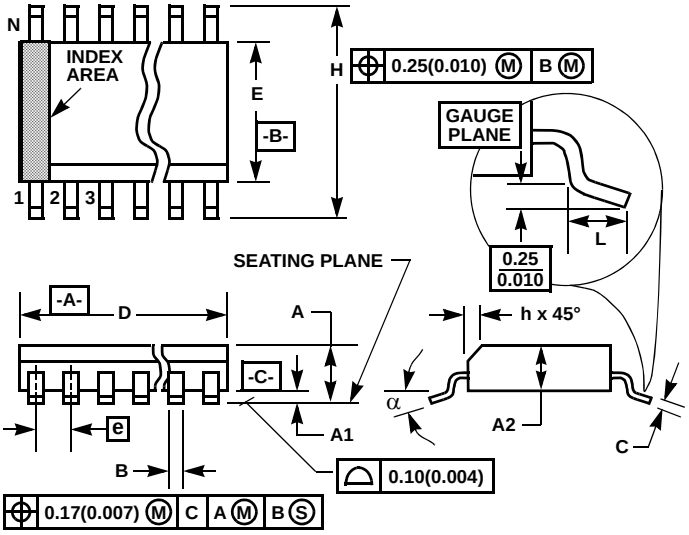
Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Bias Current	I_{CC}	LGATEx, UGATEx Open, VSENx forced above regulation point, V_{IN} > 5V	-	1.8	3.0	mA
Shut-down Current	I_{CCSN}		-	-	1	µA
VCC UVLO						
Rising VCC Threshold	V_{CCU}		4.3	4.45	4.5	V
Falling VCC Threshold	V_{CCD}		4	4.14	4.34	V
V_{IN}						
Input Voltage Pin Current (Sink)	I_{VIN}		-	-	35	µA
Shut-Down Current	I_{VINS}		-	-	1	µA
OSCILLATOR						
PWM1 Oscillator Frequency	f_c	Commercial, ISL6227C	255	300	345	kHz
		Industrial, ISL6227I	240	300	345	kHz
Ramp Amplitude, pk-pk	V_{R1}	V_{IN} = 16V (Note 5)	-	2	-	V
Ramp Amplitude, pk-pk	V_{R2}	V_{IN} = 5V (Note 5)	-	0.625	-	V
Ramp Offset	V_{ROFF}	(Note 5)	-	1	-	V
Ramp/V_{IN} Gain	G_{RB1}	$V_{IN} \geq$ 4.2V (Note 5)	-	125	-	mV/V
Ramp/V_{IN} Gain	G_{RB2}	$V_{IN} \leq$ 4.1V (Note 5)	-	250	-	mV/V
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}		-	0.9	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-Up	I_{SOFT}		-	-4.5	-	µA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Complete Threshold	V_{ST}	(Note 5)	-	1.5	-	V
PWM CONVERTERS						
Load Regulation		0.0mA < I_{VOUT1} < 5.0A; 5.0V < V_{BATT} < 28.0V	-2.0	-	+2.0	%
VSEN Pin Bias Current	I_{VSEN}	(Note 5)	-	80	-	nA
Minimum Duty Cycle	D_{min}		-	4	-	%
Maximum Duty Cycle	D_{max}		-	87	-	%
VOUT Pin Input Impedance	I_{VOUT}	VOUT = 5V	-	134	-	kΩ
Undervoltage Shut-Down Level	V_{UVL}	Fraction of the set point; ~2µs noise filter	70	75	80	%
Overvoltage Protection	V_{OVP1}	Fraction of the set point; ~2µs noise filter	110	115	-	%
GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}	V_{CC} = 5V	-	4	8	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}	V_{CC} = 5V	-	2.3	4	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}	V_{CC} = 5V	-	4	8	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}	V_{CC} = 5V	-	1.1	3	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3µs noise filter	84	89	92	%
Power Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3µs noise filter.	110	115	120	%
PGOODx Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOODx Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	0.5	1	V
ISEN Sourcing Current		(Note 5)	-	-	260	µA
OCSET Sourcing Current Range			2	-	20	µA
EN - Low (Off)			-	-	0.8	V
EN - High (On)			2.0	-	-	V
Continuous-Conduction-Mode(CCM) Enforced (HYS Operation Inhibited)		VOUTX pulled low	-	-	0.1	V
Automatic CCM/HYS Operation Enabled		VOUTX connected to the output	0.9	-	-	V
DDR - Low (Off)			-	-	0.8	V
DDR - High (On)			3	-	-	V
DDR REF Output Voltage	V_{DDREF}	DDR = 1, I_{REF} = 0...10mA	0.99* V_{OC2}	V_{OC2}	1.01* V_{OC2}	V
DDR REF Output Current	I_{DDREF}	DDR = 1 (Note 5)	-	10	12	mA

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-