

AD845

FEATURES

Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:

Settles to 0.01% in 350 ns

100 V/ μ s Slew Rate

12.8 MHz Min Unity Gain Bandwidth

1.75 MHz Full Power Bandwidth at 20 V p-p

DC PERFORMANCE:

0.25 mV Max Input Offset Voltage

5 μ V/ $^{\circ}$ C Max Offset Voltage Drift

0.5 nA Input Bias Current

250 V/mV Min Open-Loop Gain

4 μ V p-p Max Voltage Noise, 0.1 Hz to 10 Hz

94 dB Min CMRR

Available in Plastic Mini-DIP, Hermetic Cerdip, and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard

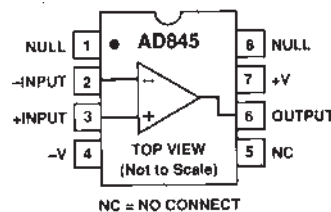
GENERAL DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/ μ s, a stable unity gain bandwidth of 16 MHz, and a settling time of 350 ns to 0.01%—while driving a parallel load of 100 pF and 500 Ω —represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs that use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

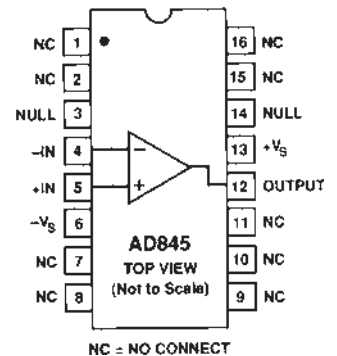
The AD845 is ideal for use in applications such as active filters, high speed integrators, photodiode preamps, sample-and-hold amplifiers, and log amplifiers, and for buffering A/D and D/A converters. The 250 μ V max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ± 10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity gain buffer circuits.

CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package
and Cerdip (Q) Package



16-Lead SOIC
(R-16) Package



The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 $^{\circ}$ C to 70 $^{\circ}$ C temperature range. AD845A and AD845B devices are specified for operation over the -40 $^{\circ}$ C to +85 $^{\circ}$ C industrial temperature range. The AD845S is specified to operate over the full military temperature range of -55 $^{\circ}$ C to +125 $^{\circ}$ C. Both the industrial and military versions are available in 8-lead Cerdip packages. The commercial version is available in an 8-lead plastic mini-DIP and 16-lead SOIC; J and S grade chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, HA2520, HA2522, HA2525, HA2620, HA2622, HA2625, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

AD845—SPECIFICATIONS (@ 25°C and ±15 V dc, unless otherwise noted.)

Parameter	Conditions	AD845J/A			AD845K/B			AD845S			Unit			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max				
INPUT OFFSET VOLTAGE ¹	T _{MIN} to T _{MAX}	Initial Offset			0.7	1.5	2.5	0.1	0.25	0.4	0.25	1.0	mV	
		Offset Drift				20		1.5	5.0		10		μV/°C	
INPUT BIAS CURRENT ²	V _{CM} = 0 V T _{MIN} to T _{MAX}	Initial			0.75	2	45/75	0.5	1	18/38	0.75	2	500	nA
														nA
INPUT OFFSET CURRENT	V _{CM} = 0 V T _{MIN} to T _{MAX}	Initial			25	300	3/6.5	15	100	1.2/2.6	25	300	20	pA
														nA
INPUT CHARACTERISTICS		Input Resistance			10 ¹¹			10 ¹¹			10 ¹¹			kΩ
		Input Capacitance			4.0			4.0			4.0			pF
INPUT VOLTAGE RANGE	V _{CM} = ±10 V	Differential			±20			±20			±20			V
		Common-Mode			±10	+10.5/-13		±10	+10.5/-13		±10	+10.5/-13		V
		Common-Mode Rejection			86	110		94	113		86	110		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	f = 10 Hz			4			4			4			μV p-p
		f = 100 Hz			80			80			80			nV/√Hz
		f = 1 kHz			60			60			60			nV/√Hz
		f = 10 kHz			25			25			25			nV/√Hz
		f = 100 kHz			18			18			18			nV/√Hz
		f = 100 kHz			12			12			12			nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	0.1			0.1			0.1			0.1			pA/√Hz
OPEN-LOOP GAIN	V _O = ±10 V R _{LOAD} ≥ 2 kΩ R _{LOAD} ≥ 500 Ω T _{MIN} -T _{MAX}	200			500			250			500			V/mV
		100			250			125			250			V/mV
		70						75			50			V/mV
														V/mV
OUTPUT CHARACTERISTICS	R _{LOAD} ≥ 500 Ω Short Circuit Open Loop	±12.5			±12.5			±12.5			±12.5			V
		50			50			50			50			mA
		5			5			5			5			Ω
FREQUENCY RESPONSE	Unity Gain V _O = ±10 V R _{LOAD} = 500 Ω	12.8			16			13.6			16			MHz
		1.75			1.75			1.75			1.75			MHz
		20			20			20			20			ns
		20			20			20			20			%
		80			100			94			100			V/μs
		350			250			350			500			ns
DIFFERENTIAL GAIN	f = 4.4 MHz	0.04			0.04			0.04			0.04			%
DIFFERENTIAL PHASE	f = 4.4 MHz	0.02			0.02			0.02			0.02			Degree
POWER SUPPLY	V _S = ±5 to ±15 V T _{MIN} to T _{MAX}	±15			±15			±15			±15			V
		±4.75			±18			±4.75			±18			V
		88			110			95			113			dB
		10			12			10			12			mA

NOTES

¹Input offset voltage specifications are guaranteed after five minutes of operation at T_A = 25°C.

²Bias current specifications are guaranteed maximum at either input after five minutes of operation at T_A = 25°C.

³FPBW = slew rate/2 π V peak.

⁴S grade T_{MIN}-T_{MAX} are tested with automatic test equipment at T_A = -55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	±18 V
Internal Power Dissipation ²	
Plastic Mini-DIP	1.6 W
CERDIP	1.4 W
16-Lead SOIC	1.5 W
Input Voltage	+V _S
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	+V _S and -V _S
Storage Temperature Range	
Q	-65°C to +150°C
N, R	-65°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

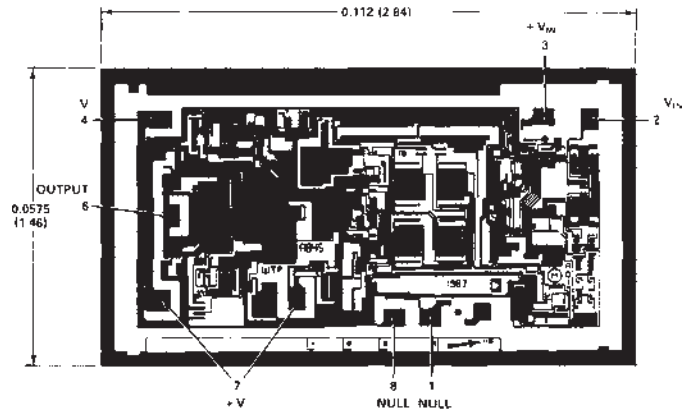
NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Mini-DIP package: $\theta_{JA} = 100^\circ\text{C/W}$; CERDIP package: $\theta_{JA} = 110^\circ\text{C/W}$; SOIC package: $\theta_{JA} = 100^\circ\text{C/W}$.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



SUBSTRATE CONNECTED TO +V_S

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option ¹
AD845JN	0°C to 70°C	8-Lead PDIP	N-8
AD845KN	0°C to 70°C	8-Lead PDIP	N-8
AD845JR-16	0°C to 70°C	16-Lead SOIC	R-16
AD845JR-16-REEL	0°C to 70°C	Tape and Reel	R-16
AD845JR-16-REEL7	0°C to 70°C	Tape and Reel	R-16
AD845AQ	-40°C to +85°C	8-Lead CERDIP	Q-8
AD845BQ	-40°C to +85°C	8-Lead CERDIP	Q-8
AD845SQ	-55°C to +125°C	8-Lead CERDIP	Q-8
AD845SQ/883B	-55°C to +125°C	8-Lead CERDIP	Q-8
5962-8964501PA ²	-55°C to +125°C	8-Lead CERDIP	Q-8
AD845JCHIPS	0°C to 70°C	Die	

NOTES

¹N = Plastic DIP; Q = CERDIP; R = Small Outline IC (SOIC).

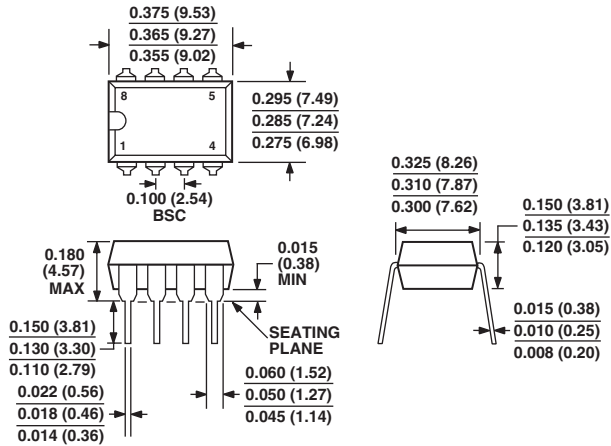
²See military data sheet.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]

(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA

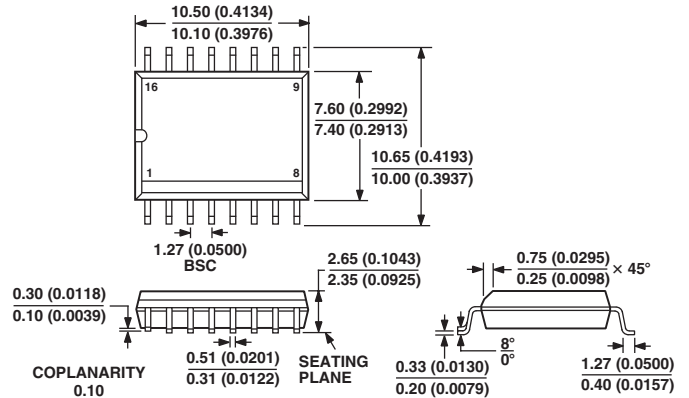
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC]

Wide Body

(R-16)

Dimensions shown in millimeters and (inches)

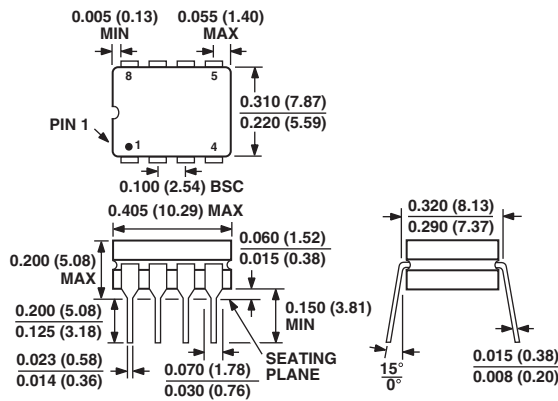


COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic Dual In-Line Package [CERDIP]

(Q-8)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN