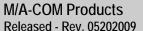


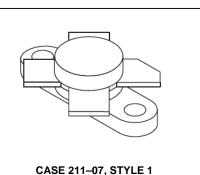
The RF Line NPN Silicon Power Transistor 30W, 30-200MHz, 28V

Designed primarily for wideband large-signal driver and output amplifier stages in the 30-200 MHz frequency range.

- Guaranteed performance at 150 MHz, 28 Vdc Output power = 30 W Minimum gain = 10 dB
- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Gold metallization system for high reliability applications



Product Image



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	VCEO	35	Vdc
Collector-Base Voltage	V _{CBO}	65	Vdc
Emitter–Base Voltage	V _{EBO}	4.0	Vdc
Collector Current — Continuous	Ι _C	3.4	Adc
Total Device Dissipation @ T _C = 25°C (1) Derate above 25°C	PD	82 0.47	Watts W/ºC
Storage Temperature Range	T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Мах	Unit
Thermal Resistance, Junction to Case	R _{eJC}	2.13	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
DFF CHARACTERISTICS	•			1	•
Collector–Emitter Breakdown Voltage (I _C = 30 mAdc, I _B = 0)	V _{(BR)CEO}	35	_	-	Vdc
Collector–Emitter Breakdown Voltage (I _C = 30 mAdc, V _{BE} = 0)	V _{(BR)CES}	65	_	-	Vdc
Collector–Base Breakdown Voltage (I _C = 30 mAdc, I _E = 0)	V _{(BR)CBO}	65	_	-	Vdc
Emitter–Base Breakdown Voltage (I _E = 3.0 mAdc, I _C = 0)	V _{(BR)EBO}	4.0	_	-	Vdc
Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0)	I _{CBO}	_	_	3.0	mAdc

DC Current Gain (I _C = 1.5 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	20	—	80	—
NOTE:					(continued)

NOTE:

1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

1

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The RF Line NPN Silicon Power Transistor 30W, 30-200MHz, 28V

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Мах	Unit
DYNAMIC CHARACTERISTICS	ŀ		•		
Output Capacitance (V _{CB} = 30 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	-	30	40	pF
FUNCTIONAL TESTS (Figure 1)	ł	•	1	•	•
Common–Emitter Amplifier Power Gain (V _{CC} = 28 Vdc, P _{out} = 30 W, f = 150 MHz)	G _{PE}	10	13.5	_	dB
Collector Efficiency (V _{CC} = 28 Vdc, P _{out} = 30 W, f = 150 MHz)	η	50	-	_	%
Load Mismatch (V _{CC} = 28 Vdc, P _{out} = 30 W, f = 150 MHz, VSWR = 30:1 all phase angles)	Ψ	No Degradation in Power Output			

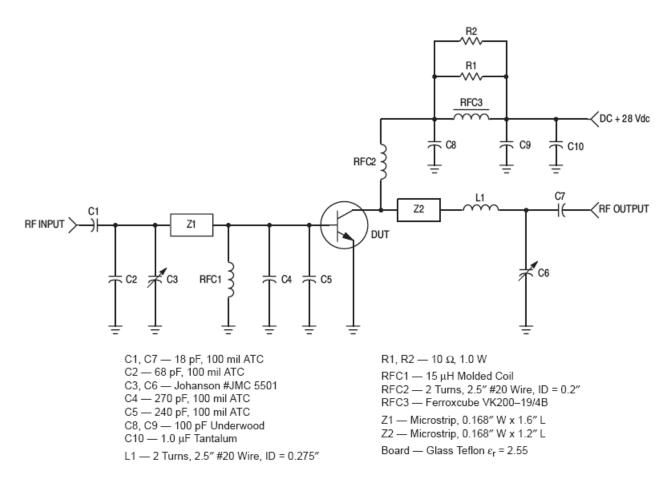


Figure 1. 150 MHz Test Circuit

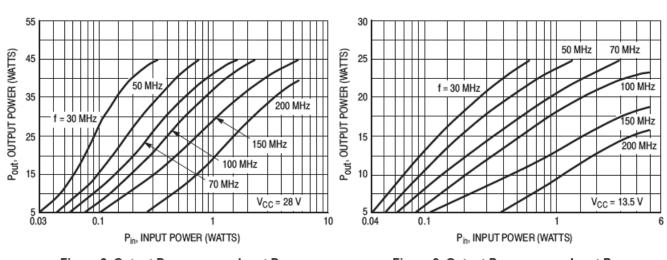
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TYPICAL PERFORMANCE CURVES

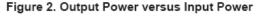


Figure 3. Output Power versus Input Power

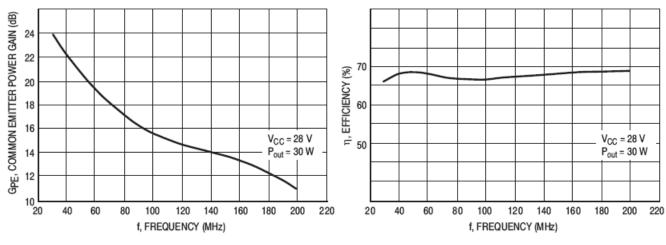


Figure 4. Power Gain versus Frequency

Figure 5. Efficiency versus Frequency

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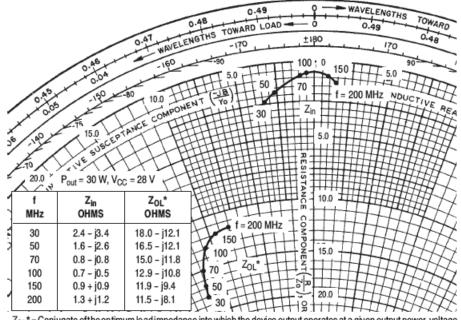
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 Z_{OL} * = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.



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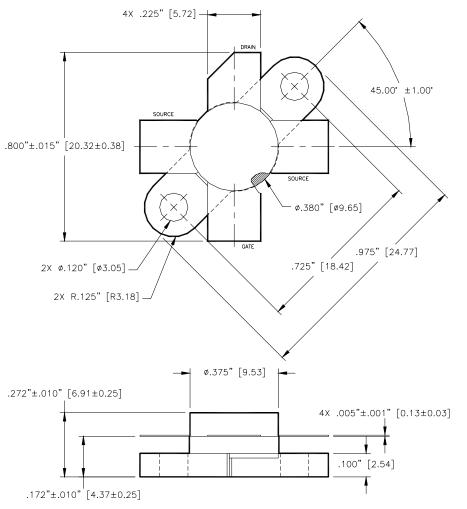
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Unless otherwise noted, tolerances are inches $\pm .005$ " [millimeters ± 0.13 mm]

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