

# MC14069UB

## Hex Inverter

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications
- Pb-Free Packages are Available

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

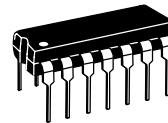
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

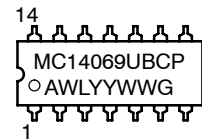


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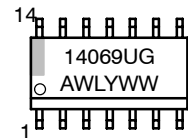
### MARKING DIAGRAMS



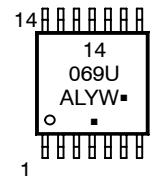
PDIP-14  
P SUFFIX  
CASE 646



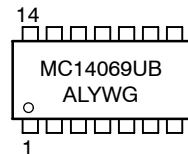
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location

WL, L = Wafer Lot

YY, Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14069UB

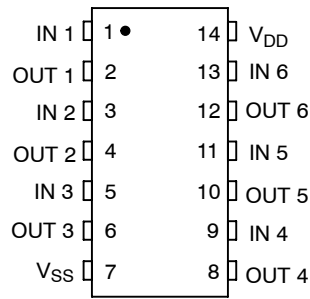


Figure 1. Pin Assignment

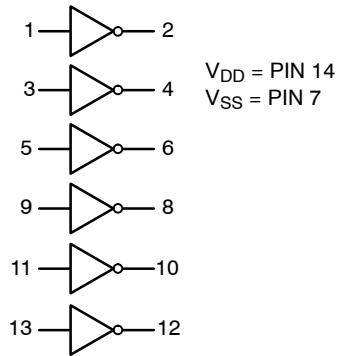
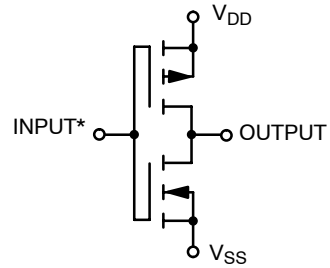


Figure 3. Logic Diagram



\*Double diode protection on all inputs not shown  
(1/6 of circuit shown)

Figure 2. Circuit Schematic

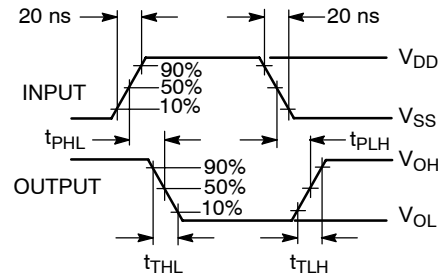
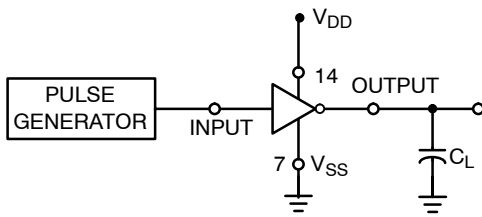


Figure 4. Switching Time Test Circuit and Waveforms

## ORDERING INFORMATION

Device	Package	Shipping†
MC14069UBCP	PDIP-14	25 Units / Tape & Ammo Box
MC14069UBCPG	PDIP-14 (Pb-Free)	
MC14069UBD	SOIC-14	55 Units / Rail
MC14069UBDG	SOIC-14 (Pb-Free)	
MC14069UBDR2	SOIC-14	2500 Units / Tape & Reel
MC14069UBDR2G	SOIC-14 (Pb-Free)	
MC14069UBDTR2	TSSOP-14*	
MC14069UBDTR2G	TSSOP-14*	
MC14069UBFEL	SOEIAJ-14	2000 Units / Tape & Reel
MC14069UBFELG	SOEIAJ-14 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(2)</sup>	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub>  V <sub>in</sub> = 0	"0" Level V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc	
		10	9.95	-	9.95	10	-	9.95	-		
		15	14.95	-	14.95	15	-	14.95	-		
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	-	1.0	-	2.25	1.0	-	1.0	Vdc	
		10	-	2.0	-	4.50	2.0	-	2.0		
		15	-	2.5	-	6.75	2.5	-	2.5		
	"1" Level V <sub>IH</sub>	5.0	4.0	-	4.0	2.75	-	4.0	-	Vdc	
		10	8.0	-	8.0	5.50	-	8.0	-		
		15	12.5	-	12.5	8.25	-	12.5	-		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
		15	-4.2	-	-3.4	-8.8	-	-2.4	-		
	Sink I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc	
		10	1.6	-	1.3	2.25	-	0.9	-		
15		4.2	-	3.4	8.8	-	2.4	-			
Input Current	I <sub>in</sub>	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	0.25	-	0.0005	0.25	-	7.5	μAdc	
		10	-	0.5	-	0.0010	0.5	-	15		
		15	-	1.0	-	0.0015	1.0	-	30		
Total Supply Current <sup>(3) (4)</sup> (Dynamic plus Quiescent, Per Gate) (C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /6 I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /6 I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub> /6								μAdc
Output Rise and Fall Times <sup>(3)</sup> (C <sub>L</sub> = 50 pF) t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.60 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.40 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	-	-	-	100	200	-	-	ns	
		10	-	-	-	50	100	-	-		
		15	-	-	-	40	80	-	-		
Propagation Delay Times <sup>(3)</sup> (C <sub>L</sub> = 50 pF) t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 20 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 22 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 17 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	-	-	-	65	125	-	-	ns	
		10	-	-	-	40	75	-	-		
		15	-	-	-	30	55	-	-		

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

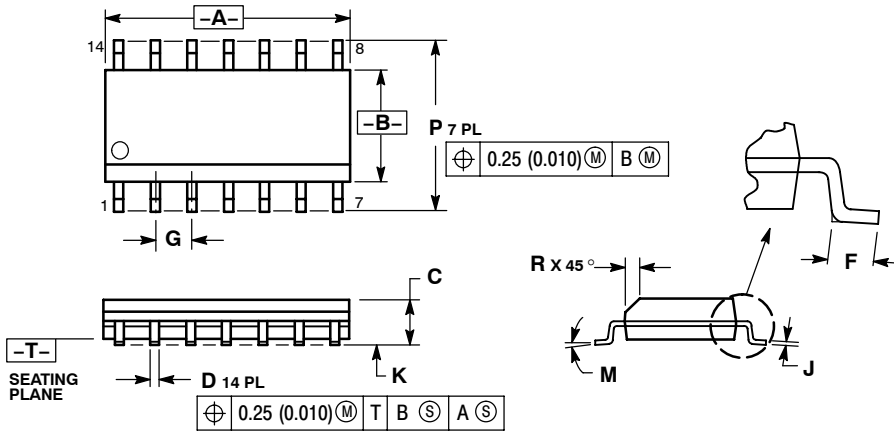
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14069UB

SOIC-14  
CASE 751A-03  
ISSUE H

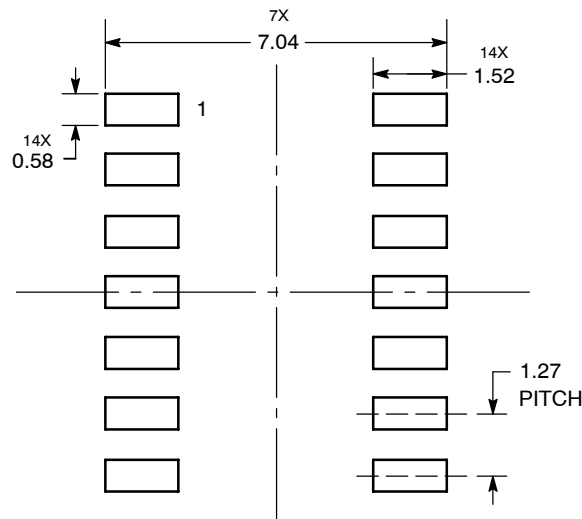


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.