Ultrafast, 4 ns Single-Supply Comparators

AD8611/AD8612

FEATURES

4 ns propagation delay at 5 V
Single-supply operation: 3 V to 5 V
100 MHz input
Latch function

APPLICATIONS

High speed timing
Clock recovery and clock distribution
Line receivers
Digital communications
Phase detectors
High speed sampling
Read channel detection
PCMCIA cards
Zero-crossing detector
High speed analog-to-digital converter (ADC)
Upgrade for LT1394 and LT1016 designs

PIN CONFIGURATIONS

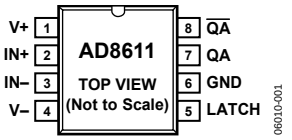


Figure 1. 8-Lead Narrow Body SOIC (R-8)

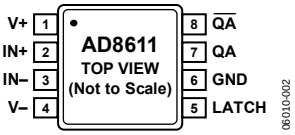


Figure 2. 8-Lead MSOP (RM-8)

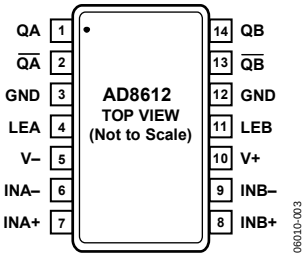


Figure 3. 14-Lead TSSOP (RU-14)

GENERAL DESCRIPTION

The AD8611/AD8612 are single and dual 4 ns comparators with latch function and complementary output. The latch is not functional if V_{CC} is less than 4.3 V.

Fast 4 ns propagation delay makes the AD8611/AD8612 good choices for timing circuits and line receivers. Propagation delays for rising and falling signals are closely matched and tracked over temperature. This matched delay makes the AD8611/AD8612 good choices for clock recovery because the duty cycle of the output matches the duty cycle of the input.

The AD8611 has the same pinout as the LT1016 and LT1394, with lower supply current and a wider common-mode input range, which includes the negative supply rail.

The AD8611/AD8612 are specified over the industrial temperature range (−40°C to +85°C). The AD8611 is available in both 8-lead MSOP and narrow 8-lead SOIC surface-mount packages. The AD8612 is available in a 14-lead TSSOP surface-mount package.

Rev. A

SPECIFICATIONS

$V+ = 5.0$ V, $V- = V_{GND} = 0$ V, $T_A = 25°C$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
		$-40°C \le T_A \le +85°C$			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		μV/°C
Input Bias Current	I_B	$V_{CM} = 0$ V	−6	−4		μA
	I_B	$-40°C \le T_A \le +85°C$	−7	−4.5		μA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V			±4	μA
Input Common-Mode Voltage Range	V_{CM}		0.0		3.0	V
Common-Mode Rejection Ratio	CMRR	$0 \text{ V} \le V_{CM} \le 3.0$ V	55	85		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT						
Logic 1 Voltage Threshold	V_{IH}	$V_{CC} > 4.3$ V	2.0	1.65		V
Logic 0 Voltage Threshold	V_{IL}	$V_{CC} > 4.3$ V		1.60	0.8	V
Logic 1 Current	I_{IH}	$V_{CC} > 4.3$ V, $V_{LH} = 3.0$ V	−1.0	−0.3		μA
Logic 0 Current	I_{IL}	$V_{CC} > 4.3$ V, $V_{LL} = 0.3$ V	−5	−2.7		μA
Latch Enable						
Pulse Width	$t_{PW(E)}$	$V_{CC} > 4.3$ V		3		ns
Setup Time	t_S	$V_{CC} > 4.3$ V		0.5		ns
Hold Time	t_H	$V_{CC} > 4.3$ V		0.5		ns
DIGITAL OUTPUTS						
Logic 1 Voltage	V_{OH}	$I_{OH} = 50$ μA, $\Delta V_{IN} > 250$ mV	3.0	3.35		V
Logic 1 Voltage	V_{OH}	$I_{OH} = 3.2$ mA, $\Delta V_{IN} > 250$ mV	2.4	3.4		V
Logic 0 Voltage	V_{OL}	$I_{OL} = 3.2$ mA, $\Delta V_{IN} > 250$ mV		0.25	0.4	V
DYNAMIC PERFORMANCE						
Input Frequency	f_{MAX}	400 mV p-p sine wave		100		MHz
Propagation Delay	t_P	200 mV step with 100 mV overdrive[1]		4.0	5.5	ns
		$-40°C \le T_A \le +85°C$		5		ns
Propagation Delay	t_P	100 mV step with 5 mV overdrive		5		ns
Differential Propagation Delay						
(Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV step with 100 mV overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		2.5		ns
Fall Time		80% to 20%		1.1		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$4.5 \text{ V} \le V+ \le 5.5$ V	55	73		dB
V+ Supply Current[2]	I+			5.7	10	mA
		$-40°C \le T_A \le +85°C$			10	
Ground Supply Current[2]	I_{GND}	$V_O = 0$ V, $R_L = \infty$		3.5	7	mA
		$-40°C \le T_A \le +85°C$			7	mA
V− Supply Current[2]	I−			2.2	4	mA
		$-40°C \le T_A \le +85°C$			5	mA

[1] Guaranteed by design.
[2] Per comparator.

V+ = 3.0 V, V− = VGND = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
Input Bias Current	I_B	V_{CM} = 0 V	−6	−4.0		µA
	I_B	−40°C ≤ T_A ≤ +85°C	−7	−4.5		µA
Input Common-Mode Voltage Range	V_{CM}		0		1.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.0 V	55			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = −3.2 mA, V_{IN} > 250 mV	1.2[1]			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA, V_{IN} > 250 mV			0.3	V
LATCH ENABLE INPUT		Not functional if V_{CC} < 4.3 V				
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	2.7 V ≤ V+ ≤ 6 V		46		dB
Supply Currents		V_O = 0 V, R_L = ∞				
V+ Supply Current[2]	I+	−40°C ≤ T_A ≤ +85°C		4.5	6.5	mA
					10	mA
Ground Supply Current[2]	I_{GND}	−40°C ≤ T_A ≤ +85°C		2.5	3.5	mA
					5.5	mA
V− Supply Current[2]	I−			2	3.5	mA
		−40°C ≤ T_A ≤ +85°C			4.8	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	100 mV step with 20 mV overdrive[3]		4.5	6.5	ns

[1] Output high voltage without pull-up resistor. It may be useful to have a pull-up resistor to V+ for 3 V operation.
[2] Per comparator.
[3] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Total Analog Supply Voltage	7.0 V
Digital Supply Voltage	7.0 V
Input Voltage[1]	±4 V
Differential Input Voltage	±5 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
R, RU, RM Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	
R, RU, RM Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

[1]The analog input voltage is equal to ±4 V or the analog supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	240	43	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

[1]θ_{JA} is specified for the worst-case conditions, that is, a device in socket for P-DIP and a device soldered in circuit board for SOIC and TSSOP.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

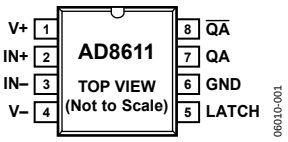


Figure 4. 8-Lead Narrow Body SOIC Pin Configuration

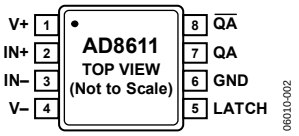


Figure 5. 8-Lead MSOP Pin Configuration

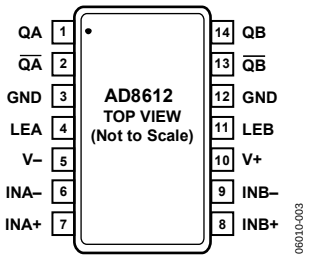
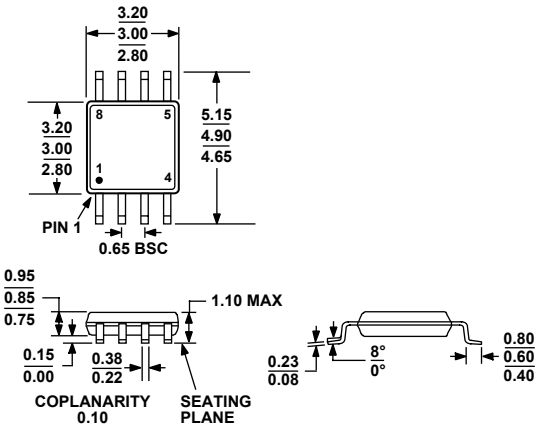


Figure 6. 14-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

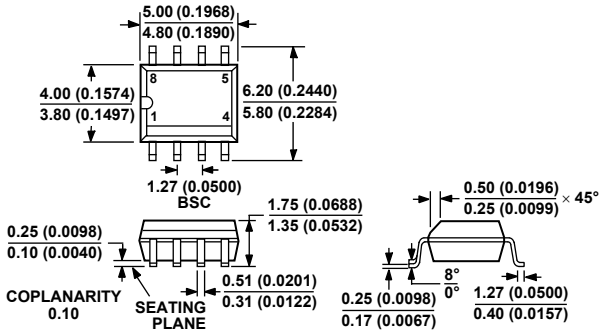
Pin No.			
SOIC and MSOP	**TSSOP**	**Mnemonic**	**Description**
1	10	V+	Positive Supply Terminal.
2		IN+	Noninverting Analog Input of the Differential Input Stage.
3		IN–	Inverting Analog Input of the Differential Input Stage.
4	5	V–	Negative Supply Terminal.
5		LATCH	Latch Enable Input.
6	3, 12	GND	Negative Logic Supply
7	1	QA	One of Two Complementary Output for Channel A.
8	2	$\overline{QA}$	One of Two Complementary Output for Channel A.
	14	QB	One of Two Complementary Output for Channel B.
	13	$\overline{QB}$	One of Two Complementary Output for Channel B.
	4	LEA	Channel A Latch Enable.
	11	LEB	Channel B Latch Enable.
	7	INA+	Noninverting Analog Input of the Differential Input Stage for Channel A.
	6	INA–	Inverting Analog Input of the Differential Input Stage for Channel A.
	8	INB+	Noninverting Analog Input of the Differential Input Stage for Channel B.
	9	INB–	Inverting Analog Input of the Differential Input Stage for Channel B.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

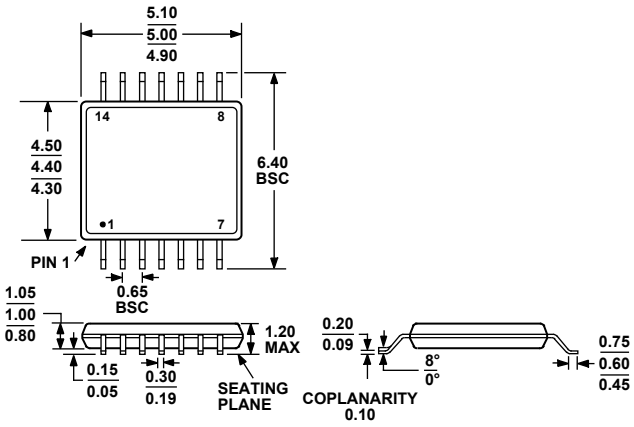
Figure 27. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 29. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8611ARM-REEL	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611ARM-R2	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611ARMZ-REEL[1]	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611ARMZ-R2[1]	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611AR	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611AR-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611AR-REEL7	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ-REEL[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ-REEL7[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8612ARU	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
AD8612ARU-REEL	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
AD8612ARUZ[1]	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
AD8612ARUZ-REEL[1]	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	

[1] Z = Pb-free part.