

# FAN6921ML

## Integrated Critical Mode PFC/Quasi-Resonant Current Mode PWM Controller

### Features

- Integrated PFC and Flyback Controller
- Critical Mode PFC Controller
- Zero-Current Detection for PFC Stage
- Quasi-Resonant Operation for PWM Stage
- Internal Minimum  $t_{off}$  8 $\mu$ s for QR PWM Stage
- Internal 10ms Soft-Start for PWM
- Brownout Protection
- H/L Line Over-Power Compensation (OPC)
- Latched Protection (FB Pin)
  - Over-Power/ Overload Protection
  - Short-Circuit Protection
  - Open-Loop Protection
- Externally Latch Triggering (RT Pin)
- Adjustable Over-Temperature Latched (RT Pin)
- VDD Pin & Output Voltage OVP (Latched)
- Internal Temperature Shutdown (140°C)

### Applications

- AC/DC NB Adapters
- Open-Frame SMPS
- Battery Charger

### Description

The highly integrated FAN6921ML combines a Power Factor Correction (PFC) controller and a Quasi-Resonant PWM controller. Integration provides cost-effective design and allows for fewer external components.

For PFC, FAN6921ML uses a controlled on-time technique to provide a regulated DC output voltage and to perform natural power factor correction. With an innovative THD optimizer, FAN6921ML can reduce input current distortion at zero-crossing duration to improve THD performance.

For PWM, FAN6921ML enhances the power system performance through valley detection, green-mode operation, and high / low line over power compensation. FAN6921ML provides: secondary-side open-loop and over-current protection, external latch triggering, adjustable over-temperature protection by RT pin and external NTC resistor, internal over-temperature shutdown, V<sub>DD</sub> pin OVP, and DET pin over-voltage for output OVP, and brownin/out for AC input voltage under-voltage protection (UVP).

The FAN6921ML controller is available in a 16-pin small outline package (SOP).

### Ordering Information

Part Number	OLP Mode	Operating Temperature Range	Package	Packing Method
FAN6921MLMY	Latch	-40°C to +105°C	16-Pin Small Outline Package (SOP)	Tape & Reel

Application Diagram

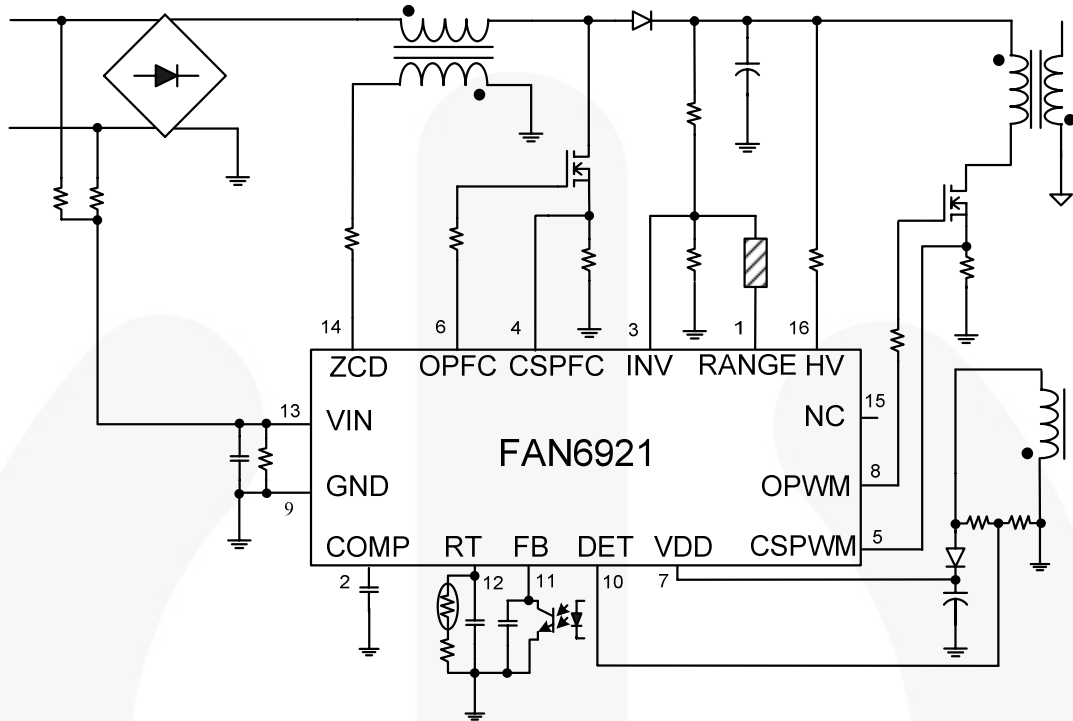


Figure 1. Typical Application

### Internal Block Diagram

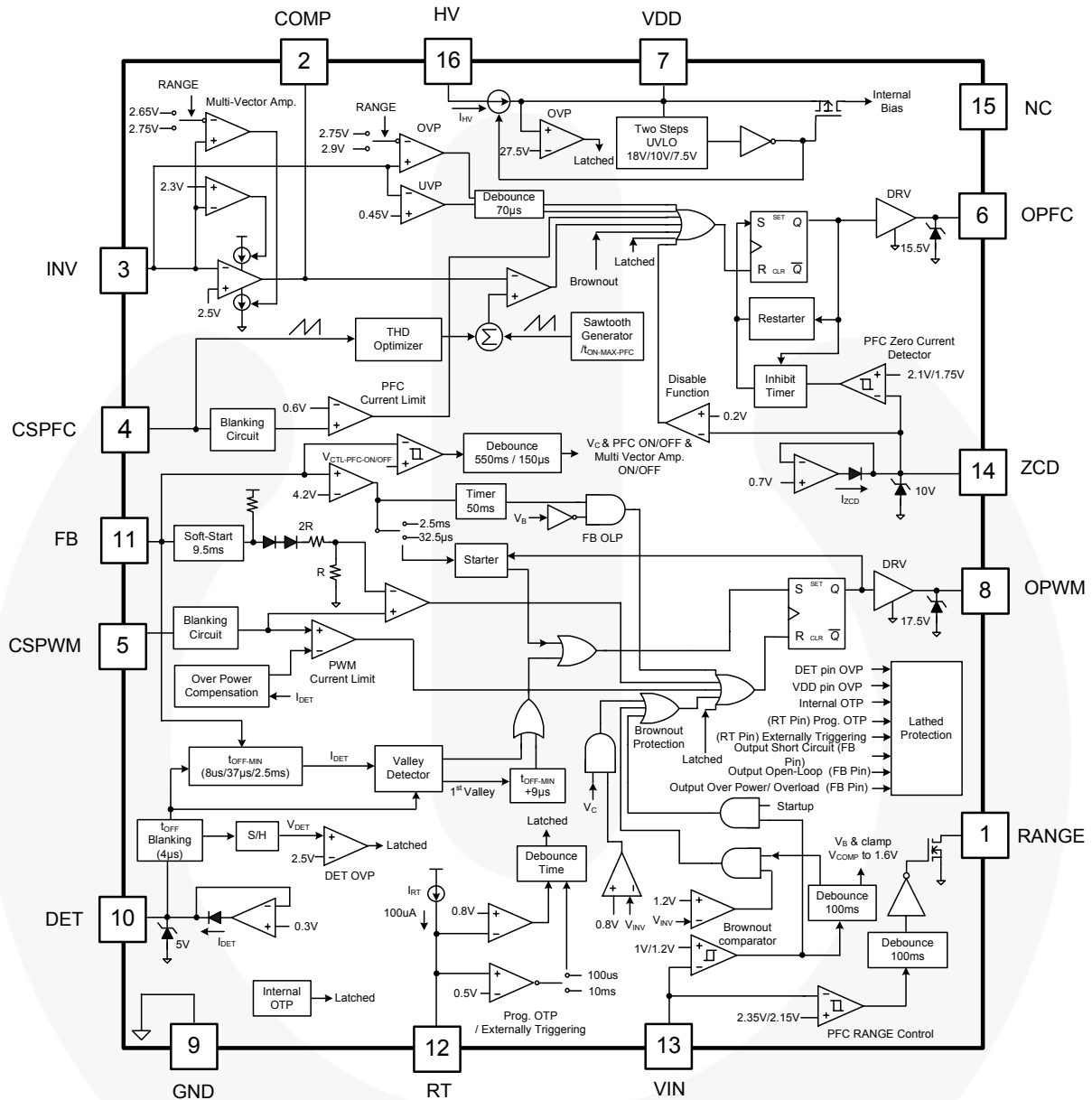


Figure 2. Functional Block Diagram

## Marking Information

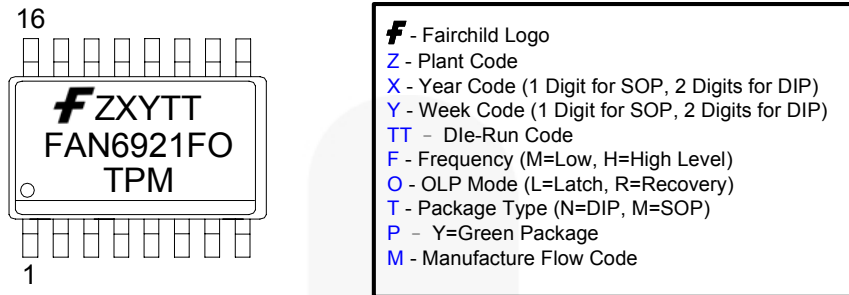


Figure 3. Marking Diagram

## Pin Configuration

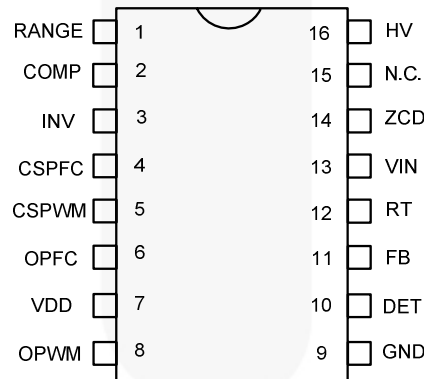


Figure 4. Pin Configuration

## Pin Definitions

Pin #	Name	Description
1	RANGE	RANGE pin's impedance changes according to VIN pin voltage level. When the input voltage detected by the VIN pin is lower than a threshold voltage, it sets to high impedance; whereas it sets to low impedance if input voltage is high level.
2	COMP	Output pin of the error amplifier. It is a transconductance type error amplifier for PFC output voltage feedback. Proprietary multi-vector current is built-in to this amplifier; therefore, the compensation for the PFC voltage feedback loop allows a simple compensation circuit between this pin and GND.
3	INV	Inverting input of the error amplifier. This pin is used to receive PFC voltage level by a voltage divider and provides PFC output over- and under-voltage protections.
4	CSPFC	Input to the PFC over-current protection comparator that provides cycle-by-cycle current limiting protection. When the sensed voltage across the PFC current-sensing resistor reaches the internal threshold (0.6 typical), the PFC switch is turned off to activate cycle-by-cycle current limiting.

## Pin Definitions

Pin #	Name	Description
5	CSPWM	Input to the comparator of the PWM over-current protection and performs PWM current-mode control with FB pin voltage. A resistor is used to sense the switching current of the PWM switch and the sensing voltage is applied to the CSPWM pin for the cycle-by-cycle current limit, current-mode control, and high / low line over-power compensation according to DET pin source current during PWM on time.
6	OPFC	Totem-pole driver output to drive the external power MOSFET. The clamped gate output voltage is 15.5V.
7	VDD	Power supply. The threshold voltages for startup and turn-off are 18V and 7.5V, respectively. The startup current is less than 30 $\mu$ A and the operating current is lower than 10mA.
8	OPWM	Totem-pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 17.5V.
9	GND	The power ground and signal ground.
10	DET	This pin is connected to an auxiliary winding of the PWM transformer through a resistor divider for the following purposes: <ul style="list-style-type: none"> <li>Producing an offset voltage to compensate the threshold voltage of PWM current limit for providing over-power compensation. The offset is generated in accordance with the input voltage when PWM switch is on.</li> <li>Detecting the valley voltage signal of drain voltage of the PWM switch to achieve the valley voltage switching and minimize the switching loss on the PWM switch.</li> <li>Providing output over-voltage protection. A voltage comparator is built-in to the DET pin. The DET pin detects the flat voltage through a voltage divider paralleled with auxiliary winding. This flat voltage is reflected to the secondary winding during PWM inductor discharge time. If output OVP and this flat voltage is higher than 2.5V, the controller enters latch mode and stops all PFC and PWM switching operation.</li> </ul>
11	FB	Feedback voltage pin. This pin is used to receive the output voltage level signal to determine PWM gate duty for regulating output voltage. The FB pin voltage can also activate open-loop, overload, or output-short-circuit protection if the FB pin voltage is higher than a threshold of around 4.2V for more than 50ms. The input impedance of this pin is a 5k $\Omega$ equivalent resistance. A 1/3 attenuator is connected between the FB pin and the input of the CSPWM/FB comparator.
12	RT	Adjustable over-temperature protection and external latch triggering. A constant current flows out of the RT pin. When RT pin voltage is lower than 0.8V (typical), latch mode protection is activated and stops all PFC and PWM switching operation until the AC plug is removed.
13	VIN	Line-voltage detection for brownin/out protections. This pin can receive the AC input voltage level through a voltage divider. The voltage level of the VIN pin is not only used to control RANGE pin's status, but it can also perform brownin/out protection for AC input voltage UVP.
14	ZCD	Zero-current detection for the PFC stage. This pin is connected to an auxiliary winding coupled to PFC inductor winding to detect the ZCD voltage signal once the PFC inductor current discharges to zero. When the ZCD voltage signal is detected, the controller starts a new PFC switching cycle. When the ZCD pin voltage is pulled to under 0.2V (typical), it disables the PFC stage and the controller stops PFC switching. This can be realized with an external circuit if disabling the PFC stage is desired.
15	NC	No connection
16	HV	High-voltage startup. HV pin is connected to the AC line voltage through a resistor (100k $\Omega$ typical) for providing a high-charging current to V <sub>DD</sub> capacitor.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		30	V
V <sub>HV</sub>	HV		500	V
V <sub>H</sub>	OPFC, OPWM	-0.3	25.0	V
V <sub>L</sub>	Others (INV, COMP, CSPFC, DET, FB, CSPWM, RT)	-0.3	7.0	V
V <sub>ZCD</sub>	Input Voltage to ZCD Pin	-0.3	12.0	V
P <sub>D</sub>	Power Dissipation		800	mW
θ <sub>JA</sub>	Thermal Resistance; Junction-to-Air		104	°C/W
θ <sub>JC</sub>	Thermal Resistance; Junction-to-Case		41	°C/W
T <sub>J</sub>	Operating Junction Temperature	-40	+150	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
T <sub>L</sub>	Lead Temperature; Soldering 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114 (All Pins Except HV Pin) <sup>(3)</sup>		4500	V
	Charged Device Model, JESD22-C101 (All Pins Except HV Pin) <sup>(3)</sup>		1250	

### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the GND pin.
3. All pins including HV pin: CDM=750V, HBM=1000V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T <sub>A</sub>	Operating Ambient Temperature	-40	+105	°C

## Electrical Characteristics

$V_{DD}=15V$ ,  $T_A=-40\sim 105^{\circ}C$  ( $T_A=T_J$ ), unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>V<sub>DD</sub> Section</b>						
$V_{OP}$	Continuously Operating Voltage				25	V
$V_{DD-ON}$	Turn-On Threshold Voltage		16.5	18.0	19.5	V
$V_{DD-PWM-OFF}$	PWM Off Threshold Voltage		9	10	11	V
$V_{DD-OFF}$	Turn-Off Threshold Voltage		6.5	7.5	8.5	V
$I_{DD-ST}$	Startup Current	$V_{DD}=V_{DD-ON} - 0.16V$ , Gate Open		10	20	$\mu A$
$I_{DD-OP}$	Operating Current	$V_{DD}=15V$ , OPFC; OPWM=100KHz; $C_{L-PFC}$ , $C_{L-PWM}=2nF$			10	mA
$I_{DD-GREEN}$	Green Mode Operating Supply Current (Average)	$V_{DD}=15V$ , OPWM=450Hz, $C_{L-PWM}=2nF$		5.5		mA
$I_{DD-PWM-OFF}$	Operating Current at PWM-OFF Phase	$V_{DD}=V_{DD-PWM-OFF} - 0.5V$	70	120	170	$\mu A$
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection (Latch-Off)		26.5	27.5	28.5	V
$t_{VDD-OVP}$	$V_{DD}$ OVP Debounce Time		100	150	200	$\mu s$
$I_{DD-LATCH}$	$V_{DD}$ OVP Latch-up Holding Current	$V_{DD}=7.5V$		120		$\mu A$
<b>HV Startup Current Source Section</b>						
$V_{HV-MIN}$	Minimum Startup Voltage on HV Pin				50	V
$I_{HV}$	Supply Current from Pin HV	$V_{AC}=90V$ ( $V_{DC}=120V$ ), $V_{DD}=0V$		1.2		mA
		HV=500V, $V_{DD}=V_{DD-OFF} + 1V$		1.0		$\mu A$
<b>V<sub>VIN</sub> and RANGE Section</b>						
$V_{VIN-UVP}$	The Threshold Voltage for AC Input Under-Voltage Protection		0.95	1.00	1.05	V
$V_{VIN-RE-UVP}$	Under-Voltage Protection Reset Voltage (for Startup)		$V_{VIN-UVP} + 0.15V$	$V_{VIN-UVP} + 0.2V$	$V_{VIN-UVP} + 0.25V$	V
$t_{VIN-UVP}$	Under-Voltage Protection Debounce Time (No Need at Startup/Hiccup Mode)		70	100	130	ms
$V_{VIN-RANGE-H}$	High $V_{VIN}$ Threshold for RANGE Comparator	RANGE=Ground	2.30	2.35	2.40	V
$V_{VIN-RANGE-L}$	Low $V_{VIN}$ Threshold for RANGE Comparator	RANGE=Open	2.10	2.15	2.20	V
$t_{RANGE}$	Range-Enable/Disable Debounce Time		70	100	130	ms
$V_{RANGE-OL}$	Output Low Voltage of RANGE Pin	$I_O=1mA$			0.5	V
$t_{ON-MAX-PFC}$	PFC Maximum On Time		22	25	28	$\mu s$

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## Electrical Characteristics (Continued)

$V_{DD}=15V$ ,  $T_A=-40\sim 105^{\circ}C$  ( $T_A=T_J$ ), unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>PFC Stage</b>						
<b>Voltage Error Amplifier Section</b>						
G <sub>m</sub>	Transconductance <sup>(4)</sup>		100	125	150	μmho
V <sub>REF</sub>	Feedback Comparator Reference Voltage		2.465	2.500	2.535	V
V <sub>INV-H</sub>	Clamp High Feedback Voltage	RANGE=Open	2.70	2.75	2.80	V
		RANGE=Ground	2.60	2.65	2.70	V
V <sub>RATIO</sub>	Clamp High Output Voltage Ratio	V <sub>INVH</sub> / V <sub>REF</sub> , RANGE=Open	1.06		1.14	
		V <sub>INVH</sub> / V <sub>REF</sub> , RANGE=Ground	1.04		1.08	
V <sub>INV-L</sub>	Clamp Low Feedback Voltage		2.25	2.30	2.35	V
V <sub>INV-OVP</sub>	Over Voltage Protection for INV Input	RANGE=Open		2.90	2.95	V
		RANGE=Ground		2.75	2.80	V
t <sub>INV-OVP</sub>	Over-Voltage Protection Debounce Time		50	70	90	μs
V <sub>INV-UVP</sub>	Under-Voltage Protection for INV Input		0.35	0.45	0.55	V
t <sub>INV-UVP</sub>	Under Voltage Protection Debounce Time		50	70	90	μs
V <sub>INV-FB-Latch</sub>	INV Threshold Voltage for Blocking FB latch		0.7	0.8	0.9	V
V <sub>INV-BO</sub>	PWM and PFC Off Threshold for Brownout Protection		1.15	1.20	1.25	V
V <sub>INV-BO2</sub>	PWM Off Threshold Voltage for Brownout Protection, PFC Off		0.7	0.8	0.9	V
V <sub>COMP</sub>	Comparator Output High Voltage		4.8		6.0	V
V <sub>OZ</sub>	Zero Duty Cycle Voltage on COMP Pin		1.15	1.25	1.35	V
I <sub>COMP</sub>	Comparator Output Source Current	V <sub>INV</sub> =2.3V, V <sub>COMP</sub> =1.5	15	25	35	μA
		V <sub>INV</sub> =1.5V	0.50	0.75	1.00	mA
	Comparator Output Sink Current	RANGE=Open, V <sub>INV</sub> =2.75V, V <sub>COMP</sub> =5	20	30	40	μA
		RANGE=Ground, V <sub>INV</sub> =2.65V, V <sub>COMP</sub> =5	20	30	40	μA
<b>PFC Current Sense Section</b>						
V <sub>CSPFC</sub>	Threshold Voltage for Peak Current Cycle-by-Cycle Limit	V <sub>COMP</sub> =5V		0.60		V
t <sub>PD</sub>	Propagation Delay			110	200	ns
t <sub>BNK</sub>	Leading-Edge Blanking Time		110	180	250	ns
A <sub>v</sub>	CSPFC Compensation Ratio for THD		0.90	0.95	1.00	

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**Electrical Characteristics** (Continued)

$V_{DD}=15V$ ,  $T_A=-40^{\circ}C\sim 105^{\circ}C$  ( $T_A=T_J$ ), unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>PFC Output Section</b>						
$V_Z$	PFC Gate Output Clamping Voltage	$V_{DD}=25V$	14.0	15.5	17.0	V
$V_{OL}$	PFC Gate Output Voltage Low	$V_{DD}=15V$ , $I_O=100mA$			1.5	V
$V_{OH}$	PFC Gate Output Voltage High	$V_{DD}=15V$ , $I_O=100mA$	8			V
$t_R$	PFC Gate Output Rising Time	$V_{DD}=12V$ , $C_L=3nF$ , 20~80%	30	65	100	ns
$t_F$	PFC Gate Output Falling Time	$V_{DD}=12V$ , $C_L=3nF$ , 80~20%	30	50	70	ns
<b>PFC Zero Current Detection Section</b>						
$V_{ZCD}$	Input Threshold Voltage Rising Edge	$V_{ZCD}$ Increasing	1.9	2.1	2.3	V
$V_{ZCD-HYST}$	Threshold Voltage Hysteresis	$V_{ZCD}$ Decreasing	0.25	0.35	0.45	V
$V_{ZCD-HIGH}$	Upper Clamp Voltage	$I_{ZCD}=3mA$	8	10		V
$V_{ZCD-LOW}$	Lower Clamp Voltage	$I_{ZCD}=-1.5mA$	0.55	0.70	0.85	V
$V_{ZCD-SSC}$	Starting Source Current Threshold Voltage	$I_{ZCD}=5\mu A$	0.8	0.9	1.0	V
$t_{DELAY}$	Maximum Delay from ZCD to Output Turn-On	$V_{COMP}=5V$ , $f_S=60KHz$	100		200	ns
$t_{RESTART-PFC}$	Restart Time		300	500	700	$\mu s$
$t_{INHIB}$	Inhibit Time (Maximum Switching Frequency Limit)	$V_{COMP}=5V$	1.5	2.5	3.5	$\mu s$
$V_{ZCD-DIS}$	PFC Enable/Disable Function Threshold Voltage		150	200	250	mV
$t_{ZCD-DIS}$	PFC Enable/Disable Function Debounce Time	$V_{ZCD}=100mV$	100	150	200	$\mu s$
<b>PWM Stage</b>						
<b>Feedback Input Section</b>						
$A_V$	Input-Voltage to Current Sense Attenuation <sup>(4)</sup>	$A_V=\Delta V_{CS} / \Delta V_{FB}$ , $0 < V_{CS} < 0.9$	1/2.75	1/3.00	1/3.25	V/V
$Z_{FB}$	Input Impedance <sup>(4)</sup>	$FB > V_G$	3	5	7	K $\Omega$
$I_{OZ}$	Bias Current	$FB = V_{OZ}$		1.2	2.0	mA
$V_{OZ}$	Zero Duty-Cycle Input Voltage		0.7	0.9	1.1	V
$V_{FB-OLP}$	Open-Loop Protection Threshold Voltage		3.9	4.2	4.5	V
$t_{FB-OLP}$	The Debounce Time for Open-Loop Protection		40	50	60	ms
$t_{FB-SS}$	Internal Soft-Start Time <sup>(4)</sup>	$V_{FB}=0V\sim 3.6V$	8.5	9.5	10.5	ms

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**Electrical Characteristics** (Continued)V<sub>DD</sub>=15V, T<sub>A</sub>=-40~105°C (T<sub>A</sub>=T<sub>J</sub>), unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>DET Pin OVP and Valley Detection Section</b>						
V <sub>DET-OVP</sub>	Comparator Reference Voltage		2.45	2.50	2.55	V
A <sub>v</sub>	Open-Loop Gain <sup>(4)</sup>			60		dB
B <sub>w</sub>	Gain Bandwidth <sup>(4)</sup>			1		MHz
t <sub>DET-OVP</sub>	Output OVP(Latched) Debounce Time		100	150	200	μs
I <sub>DET-SOURCE</sub>	Maximum Source Current	V <sub>DET</sub> =0V			1	mA
V <sub>DET-HIGH</sub>	Upper Clamp Voltage	I <sub>DET</sub> =-1mA			5	V
V <sub>DET-LOW</sub>	Lower Clamp Voltage	I <sub>DET</sub> =1mA	0.5	0.7	0.9	V
t <sub>VALLEY-DELAY</sub>	Delay from Valley Signal Detected to Output Turn-On <sup>(4)</sup>		150	200	250	ns
t <sub>OFF-BNK</sub>	Leading-Edge Blanking Time for DET-OVP (2.5V) and Valley Signal when PWM MOS Turns Off <sup>(4)</sup>		3	4	5	μs
t <sub>TIME-OUT</sub>	Time-Out After t <sub>OFF-MIN</sub>		8	9	10	μs
<b>PWM Oscillator Section</b>						
t <sub>ON-MAX-PWM</sub>	Maximum On Time		38	45	52	μs
t <sub>OFF-MIN</sub>	Minimum Off Time	V <sub>FB</sub> ≥ V <sub>N</sub>	7	8	9	μs
		V <sub>FB</sub> =V <sub>G</sub>	32	37	42	μs
V <sub>N</sub>	Beginning of Green-On Mode at FB Voltage Level		1.95	2.10	2.25	V
V <sub>G</sub>	Beginning of Green-Off Mode at FB Voltage Level		1.00	1.15	1.30	V
ΔV <sub>G</sub>	Hysteresis for Beginning of Green-Off Mode at FB Voltage Level			0.1		V
V <sub>CTL-PFC-OFF</sub>	Threshold Voltage on FB to Disable PFC	RANGE Pin Internally Open	1.70	1.75	1.80	V
	Threshold Voltage on FB to Disable PFC	RANGE Pin Internally Ground	1.65	1.70	1.75	
V <sub>CTL-PFC-ON</sub>	Hysteresis Voltage on FB to Enable PFC	RANGE Pin Internally Open	1.95	2.00	2.05	V
	Hysteresis Voltage on FB to Enable PFC	RANGE Pin Internally Ground	1.75	1.80	1.85	
t <sub>PFC-OFF</sub>	PFC OFF Debounce Time to Disable PFC	PFC Status from ON to OFF	400	500	600	ms
t <sub>INHIB-PFC-OFF</sub>	Inhibit Time During t <sub>PFC-OFF</sub>	t <sub>PFC-OFF</sub>	30	34	38	μs
t <sub>PFC-ON</sub>	PFC ON Debounce Time to Enable PFC <sup>(4)</sup>	PFC Status from OFF to ON		150		μs
t <sub>STARTER-PWM</sub>	Start Timer (Time-Out Timer)	V <sub>FB</sub> < V <sub>G</sub>	2.0	2.5	3.0	ms
		V <sub>FB</sub> > V <sub>FB-OLP</sub>	25.5	32.5	39.5	μs

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**Electrical Characteristics** (Continued)

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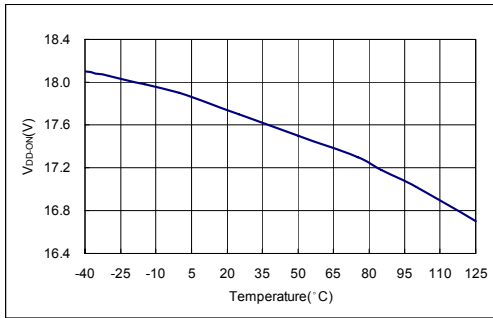
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>PWM Output Section</b>						
$V_{CLAMP}$	PWM Gate Output Clamping Voltage	$V_{DD}=25V$	16.0	17.5	19.0	V
$V_{OL}$	PWM Gate Output Voltage Low	$V_{DD}=15V$ , $I_o=100mA$			1.5	V
$V_{OH}$	PWM Gate Output Voltage High	$V_{DD}=15V$ , $I_o=100mA$	8			V
$t_R$	PWM Gate Output Rising Time	$C_L=3nF$ , $V_{DD}=12V$ , 20~80%		80	110	ns
$t_F$	PWM Gate Output Falling Time	$C_L=3nF$ , $V_{DD}=12V$ , 20~80%		40	70	ns
<b>Current Sense Section</b>						
$t_{PD}$	Delay to Output			150	200	ns
$V_{LIMIT}$	The Limit Voltage on CSPWM Pin for Over Power Compensation	$I_{DET} < 75\mu A$ , $T_A=25^{\circ}C$	0.81	0.84	0.87	V
		$I_{DET}=185\mu A$ , $T_A=25^{\circ}C$	0.69	0.72	0.75	
		$I_{DET}=350\mu A$ , $T_A=25^{\circ}C$	0.55	0.58	0.61	
		$I_{DET}=550\mu A$ , $T_A=25^{\circ}C$	0.37	0.40	0.43	
$V_{SLOPE}$	Slope Compensation <sup>(4)</sup>	$t_{ON}=45\mu s$ , RANGE=Open	0.25	0.30	0.35	V
		$t_{ON}=0\mu s$	0.05	0.10	0.15	
$t_{ON-BNK}$	Leading-Edge Blanking Time			300		ns
$V_{CS-FLOATING}$	CSPWM Pin Floating $V_{CSPWM}$ Clamped High Voltage	CSPWM Pin Floating	4.5		5	V
$t_{CS-H}$	Delay Once CSPWM Pin Floating	CSPWM Pin Floating		150		$\mu s$
<b>RT Pin Over-Temperature Protection Section</b>						
$T_{OTP}$	Internal Threshold Temperature for OTP <sup>(4)</sup>		125	140	155	$^{\circ}C$
$T_{OTP-HYST}$	Hysteresis Temperature for Internal OTP <sup>(4)</sup>			30		$^{\circ}C$
$I_{RT}$	Internal Source Current of RT Pin		90	100	110	$\mu A$
$V_{RT-LATCH}$	Latch-Mode Triggering Voltage		0.75	0.80	0.85	V
$V_{RT-RE-LATCH}$	Latch-Mode Release Voltage		$V_{RT-LATCH}+0.15$	$V_{RT-LATCH}+0.20$	$V_{RT-LATCH}+0.25$	V
$V_{RT-OTP-LEVEL}$	Threshold Voltage for Two-level Debounce Time		0.45	0.50	0.55	V
$t_{RT-OTP-H}$	Debounce Time for OTP			10		ms
$t_{RT-OTP-L}$	Debounce Time for Externally Triggering	$V_{RT} < V_{RT-OTP-LEVEL}$	70	100	130	$\mu s$

**Note:**

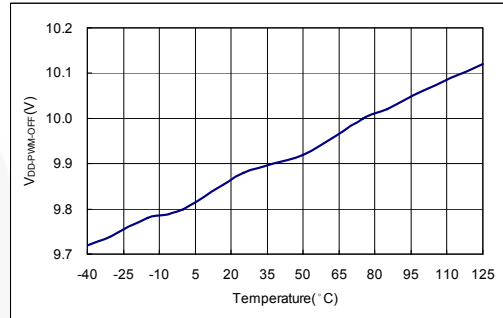
4. Guaranteed by design.

## Typical Performance Characteristics

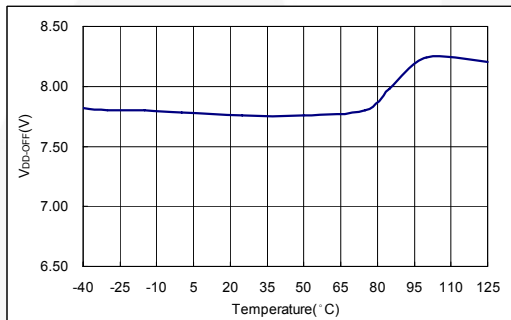
These characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .



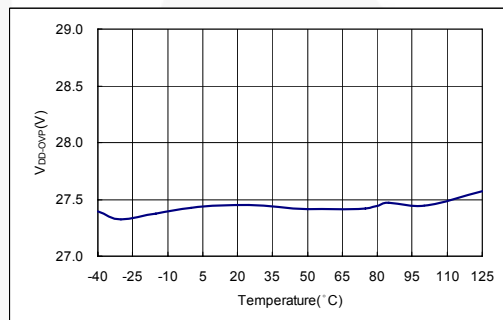
**Figure 5. Turn-On Threshold Voltage**



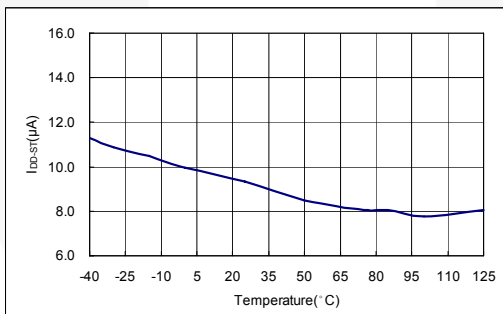
**Figure 6. PWM-Off Threshold Voltage**



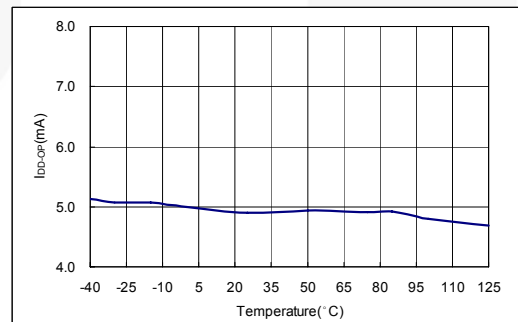
**Figure 7. Turn-Off Threshold Voltage**



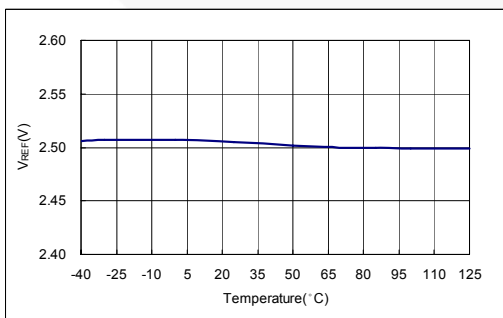
**Figure 8. V<sub>DD</sub> Over-Voltage Protection Threshold**



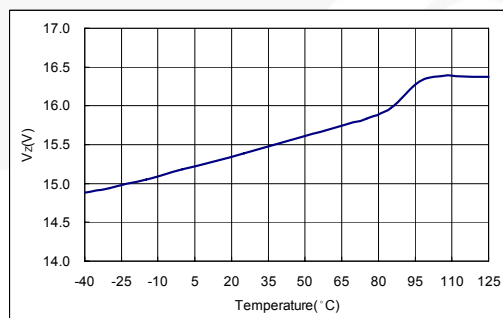
**Figure 9. Startup Current**



**Figure 10. Operating Current**



**Figure 11. PFC Output Feedback Reference Voltage**



**Figure 12. PFC Gate Output Clamping Voltage**

## Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .

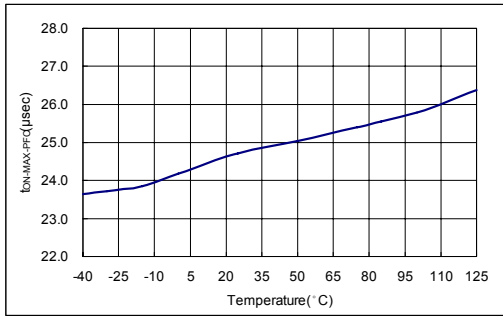


Figure 13. PFC Maximum On Time

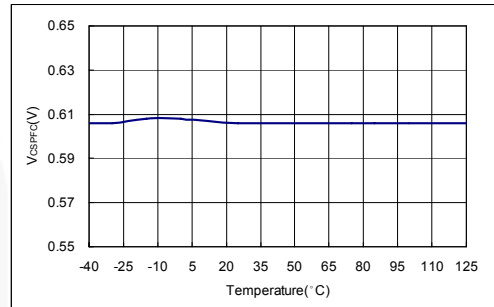


Figure 14. PFC Peak Current Limit Voltage

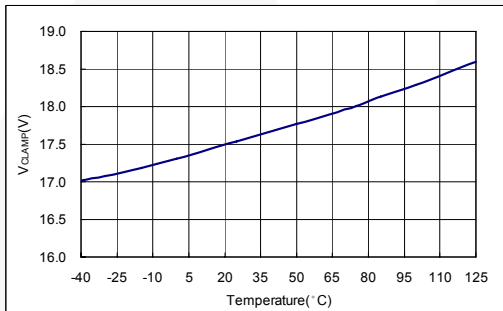


Figure 15. PWM Gate Output Clamping Voltage

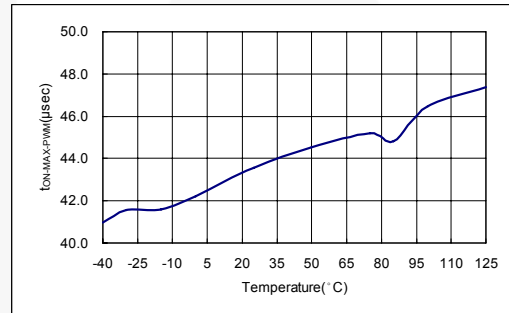


Figure 16. PWM Maximum On Time

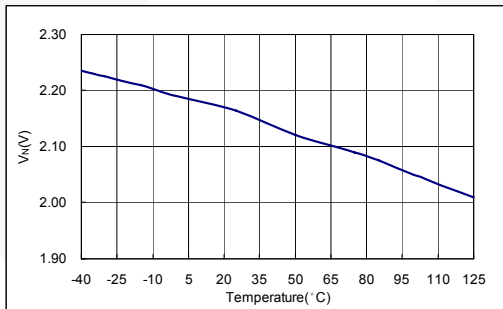


Figure 17. Beginning of Green-On Mode at  $V_{FB}$

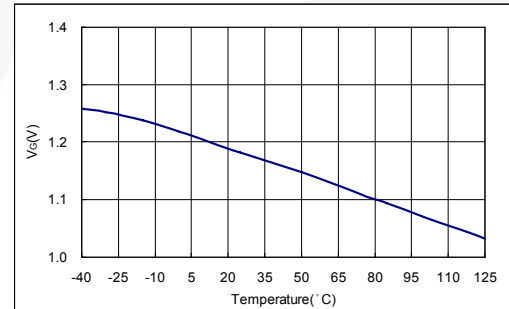


Figure 18. Beginning of Green-Off Mode at  $V_{FB}$

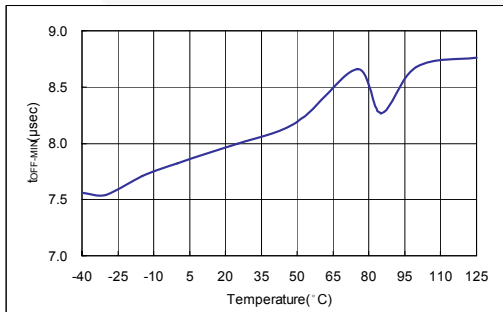


Figure 19. PWM Minimum Off Time for  $V_{FB} > V_{ON}$

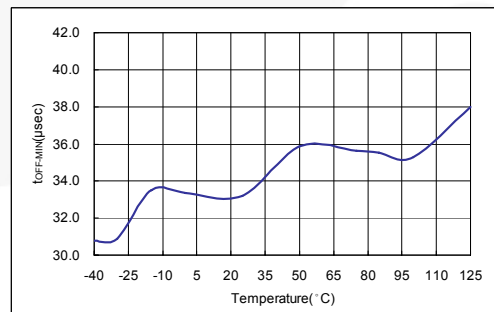
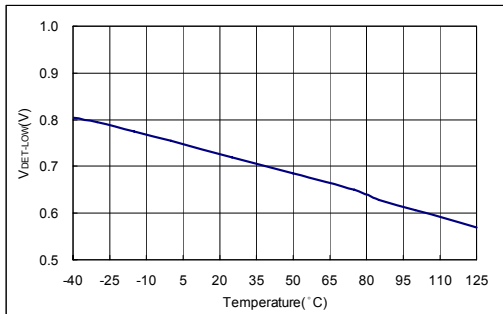


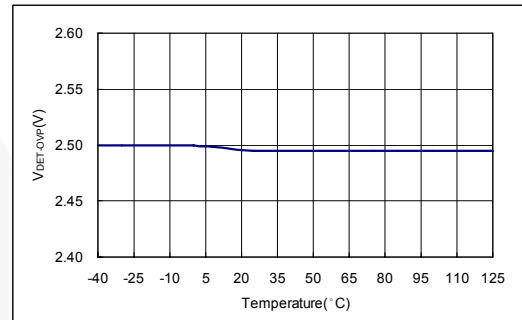
Figure 20. PWM Minimum Off Time for  $V_{FB} = V_G$

## Typical Performance Characteristics (Continued)

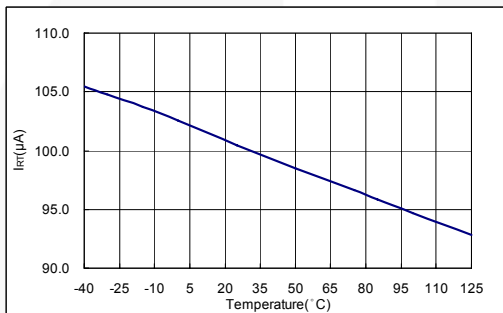
These characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .



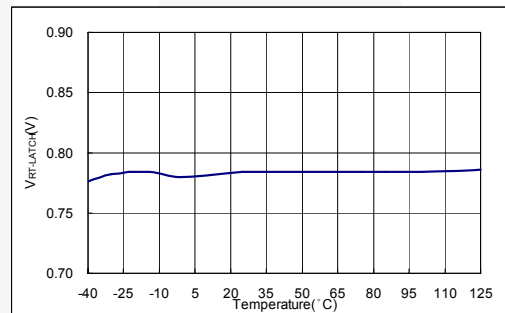
**Figure 21. Lower Clamp Voltage of DET Pin**



**Figure 22. Reference Voltage for Output Over-Voltage Protection of DET Pin**



**Figure 23. Internal Source Current of RT Pin**



**Figure 24. Over-Temperature Protection Threshold Voltage of RT Pin**

## Functional Description

### PFC Stage

#### Multi-Vector Error Amplifier and THD Optimizer

For better dynamic performance, faster transient response, and precise clamping on PFC output, FAN6921ML uses a transconductance type amplifier with proprietary innovative multi-vector error amplifier (US Patent 6,900,623). The schematic diagram of this amplifier is shown in Figure 25. The PFC output voltage is detected from the INV pin by an external resistor divider circuit that consists of  $R_1$  and  $R_2$ . When PFC output variation voltage reaches 6% over or under the reference voltage of 2.5V, the multi-vector error amplifier adjusts its output sink or source current to increase the loop response to simplify the compensated circuit.

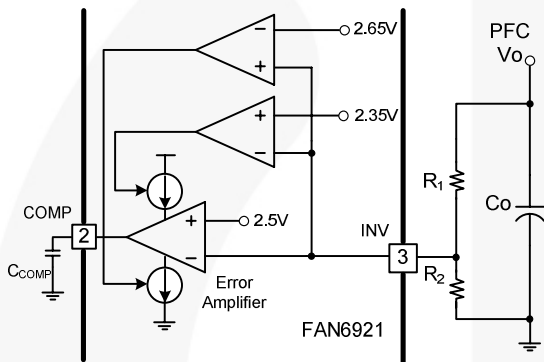


Figure 25. Multi-Vector Error Amplifier

The feedback voltage signal on the INV pin is compared with reference voltage 2.5V, which makes the error amplifier source or sink current to charge or discharge its output capacitor  $C_{COMP}$ . The COMP voltage is compared with the internally generated sawtooth waveform to determine the on time of PFC gate. Normally, with lower feedback loop bandwidth, the variation of the PFC gate on time should be very small and almost constant within one input AC cycle. However, the power factor correction circuit operating at light-load condition has a defect, zero crossing distortion, that distorts input current and makes the system's Total Harmonic Distortion (THD) worse. To improve the result of THD at light-load condition, especially at high input voltage, an innovative THD optimizer (US Patent 7,116,090) is inserted by sampling the voltage across the current-sense resistor. This sampling voltage on current-sense resistor is added into the sawtooth waveform to modulate the on time of PFC gate, so it is not constant on time within a half AC cycle. The method of operation between THD optimizer and PWM is shown in Figure 26. After THD optimizer processes, around the valley of AC input voltage, the compensated on time becomes wider than the original. The PFC on time, which is around the peak voltage, is narrowed by the THD optimizer. The timing sequences of the PFC MOS and the shape of the inductor current are shown in Figure 27. Figure 28 shows the difference between calculated fixed on time and fixed on time with THD optimizer during a half AC cycle.

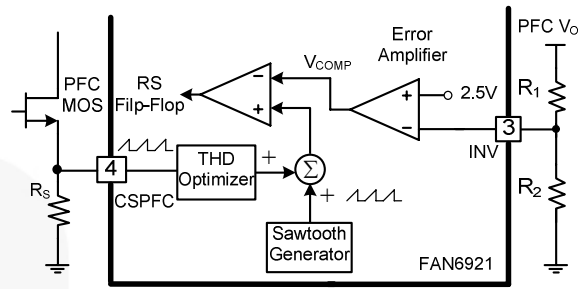


Figure 26. Multi-Vector Error Amplifier with THD Optimizer

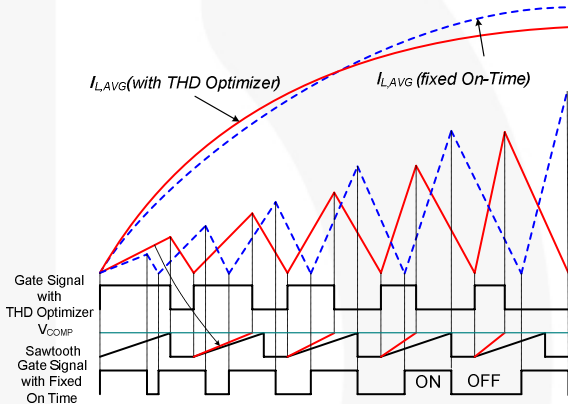


Figure 27. Operation Waveforms of Fixed On Time with and without THD Optimizer

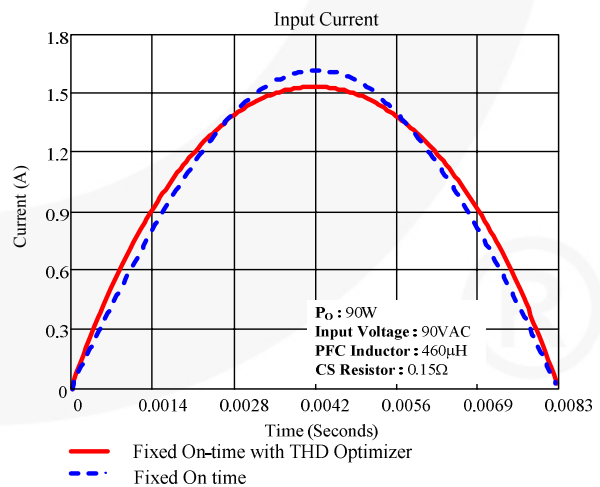
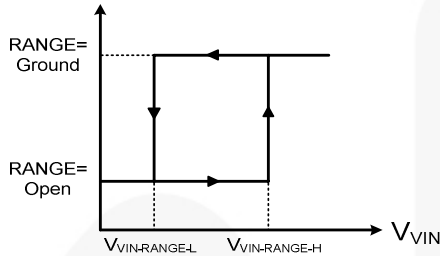


Figure 28. Calculated Waveforms of Fixed On Time with and without THD Optimizer During a Half AC Cycle

### RANGE Pin

A built-in low voltage MOSFET can be turned on or off according to  $V_{VIN}$  voltage level. The drain pin of this internal MOSFET is connected to the RANGE pin. Figure 29 shows the status curve of  $V_{VIN}$  voltage level and RANGE impedance (open or ground).



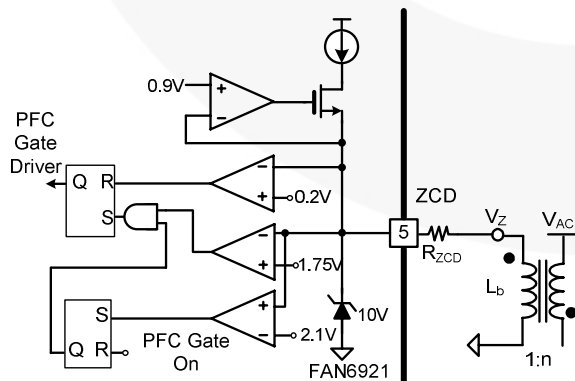
**Figure 29. Hysteresis Behavior between RANGE Pin and VIN Pin Voltage**

### Zero Current Detection (ZCD Pin)

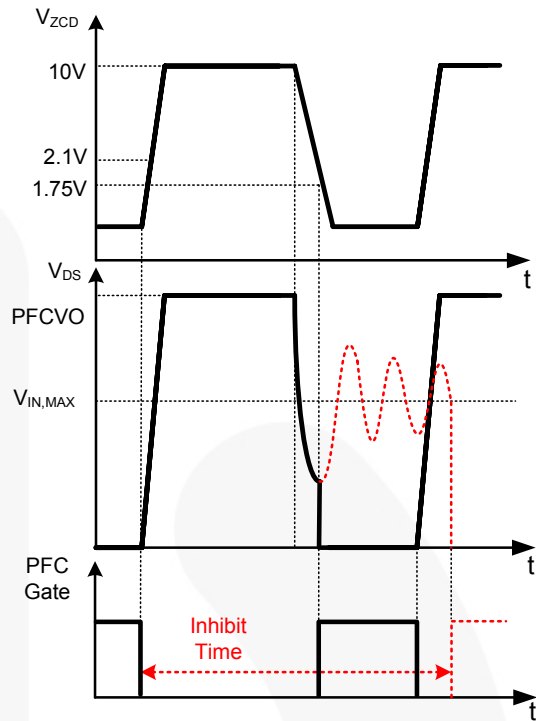
Figure 30 shows the internal block of zero-current detection. The detection function is performed by sensing the information on an auxiliary winding of the PFC inductor. Referring to Figure 31, when PFC MOS is off, the stored energy of the PFC inductor starts to release to the output load. Then the drain voltage of PFC MOS starts to decrease since the PFC inductor resonates with parasitic capacitance. Once the ZCD pin voltage is lower than the triggering voltage (1.75V typical), the PFC gate signal is sent again to start a new switching cycle.

If PFC operation needs to be shut down due to abnormal conditions, pull the ZCD pin LOW, with voltage under 0.2V (typical), to activate the PFC disable function to stop PFC switching operation.

For preventing excessive high switching frequency at light load, a built-in inhibit timer is used to limit the minimum  $t_{OFF}$  time. Even if the ZCD signal has been detected, the PFC gate signal is not sent during the inhibit time (2.5 $\mu$ s typical).



**Figure 30. Internal Block of the Zero-Current Detection**



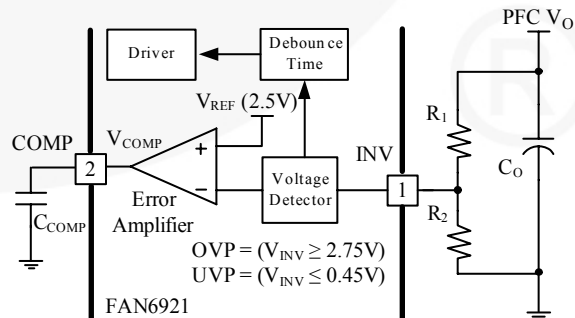
**Figure 31. Operation Waveforms of PFC Zero-Current Detection**

### Protection for PFC Stage

#### PFC Output Voltage UVP and OVP (INV Pin)

FAN6921ML provides several kinds of protection for the PFC stage. PFC output over- and under-voltage are essential for PFC stage. Both are detected and determined by INV pin voltage, as shown in Figure 32. When INV pin voltage is over 2.75V or under 0.45V, due to overshoot or abnormal conditions, and lasts for a debounce time around 70 $\mu$ s; the OVP or UVP circuit is activated to stop PFC switching operation immediately.

The INV pin is not only used to receive and regulate PFC output voltage, but can also perform PFC output OVP/ UVP protection. For failure-mode test, this pin can shut down PFC switching if pin floating occurs.



**Figure 32. Internal Block of PFC Over- and Under-Voltage Protection**





## PWM Stage

### HV Startup and Operating Current (HV Pin)

The HV pin is connected to the AC line through a resistor (refer to Figure 1). With a built-in high-voltage startup circuit, when AC voltage is applied to power system, FAN6921ML provides a high current to charge external  $V_{DD}$  capacitor to accelerate controller's startup time and build up normal rated output voltage within three seconds. To save power consumption, after  $V_{DD}$  voltage exceeds turn-on voltage and enters normal operation; this high voltage startup circuit is shut down to avoid power loss from startup resistor.

Figure 36 shows the characteristic curve of  $V_{DD}$  voltage and operating current  $I_{DD}$ . When  $V_{DD}$  voltage is lower than  $V_{DD-PWM-OFF}$ , FAN6921ML stops all switching operation and turns off some unnecessary internal circuit to reduce operating current. By doing so, the period from  $V_{DD-PWM-OFF}$  to  $V_{DD-OFF}$  can be extended and the hiccup mode frequency can be decreased to reduce the input power in case of output short circuit. Figure 37 shows the typical waveforms of  $V_{DD}$  voltage and gate signal at hiccup mode operation.

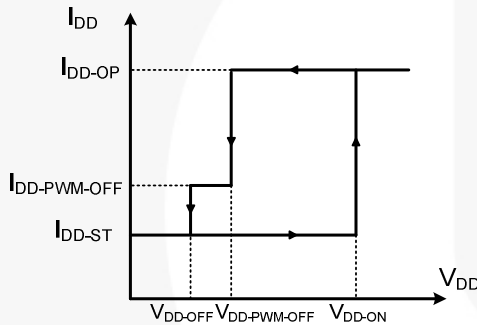


Figure 36.  $V_{DD}$  vs.  $I_{DD-OP}$  Characteristic Curve

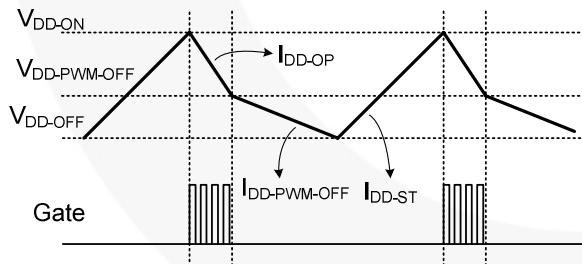


Figure 37. Typical Waveform of  $V_{DD}$  Voltage and Gate Signal in Hiccup Mode Operation

### Green-Mode Operation and PFC-ON / OFF Control (FB Pin)

Green mode is used to further reduce power loss in the system (e.g. switching loss). It uses an off-time modulation technique to regulate switching frequency according to FB pin voltage. When output loading is decreased, FB voltage becomes lower due to secondary feedback movement and the  $t_{OFF-MIN}$  is extended. After  $t_{OFF-MIN}$  (determined by FB voltage), the internal valley detection circuit is activated to detect the valley on the drain voltage of the PWM switch. When the valley signal

is detected, FAN6921ML outputs PWM gate signal to turn on the switch and begin a new switching cycle.

With green mode and valley detection, at light load condition; power system can perform extended valley switching at DCM operation and further reduce switching loss for better conversion efficiency. The FB pin voltage versus  $t_{OFF-MIN}$  time characteristic curve is shown in Figure 38. As Figure 38 shows, FAN6921ML can extend  $t_{OFF}$  time up to 2.5ms, which is around 400Hz switching frequency.

Referring to Figure 1 and Figure 2, FB pin voltage is not only used to receive secondary feedback signal to determine gate on time, but also determines PFC stage on or off status. At no-load or light-load conditions, if PFC stage is set to be off, that can reduce power consumption from PFC stage switching device and increase conversion efficiency. When output loading is decreased, the FB pin voltage becomes lower and, therefore, the FAN6921ML can detect the output loading level according to the FB pin voltage to control the on / off status of the PFC part.

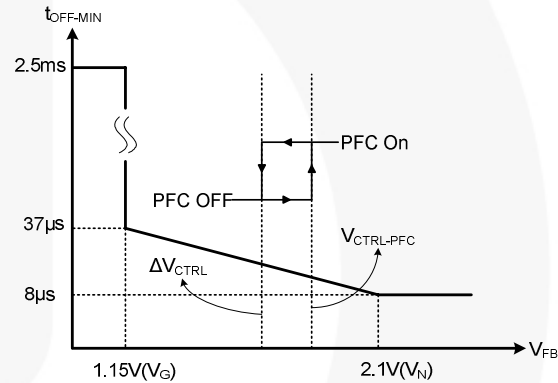
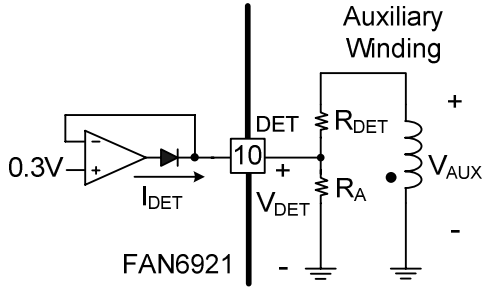


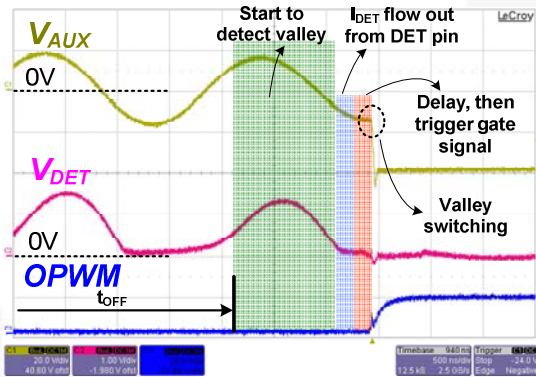
Figure 38.  $V_{FB}$  Voltage vs.  $t_{OFF-MIN}$  Time Characteristic Curve

### Valley Detection (DET Pin)

When FAN6921ML operates in green mode,  $t_{OFF-MIN}$  is determined by the green mode circuit according to FB pin voltage level. After  $t_{OFF-MIN}$ , the internal valley-detection circuit is activated. During the off time of the PWM switch, when transformer inductor current discharges to zero; the transformer inductor and parasitic capacitor of PWM switch start to resonate concurrently. When the drain voltage on the PWM switch falls, the voltage across on auxiliary winding  $V_{AUX}$  also decreases since auxiliary winding is coupled to primary winding. Once the  $V_{AUX}$  voltage resonates and falls to negative,  $V_{DET}$  voltage is clamped by the DET pin (refer to Figure 39) and FAN6921ML is forced to flow out a current  $I_{DET}$ . FAN6921ML reflects and compares this  $I_{DET}$  current. If this source current rises to a threshold current, PWM gate signal is sent out after a fixed delay time (200ns typical).



**Figure 39. Valley Detection**



**Figure 40. Measured Waveform of Valley Detection**

#### High / Low Line Over-Power Compensation (DET Pin)

Generally, when the power switch turns off, there is a delay from gate signal falling edge to power switch off. This delay is produced by an internal propagation delay of the controller and the turn-off delay of the PWM switch due to gate resistor and gate-source capacitor  $C_{ISS}$  of PWM switch. At different AC input voltage, this delay time produces different maximum output power under the same PWM current limit level. Higher input voltage generates higher maximum output power since applied voltage on primary winding is higher and causes higher rising slope inductor current. It results in higher peak inductor current at the same delay. Furthermore, under the same output wattage, the peak switching current at high line is lower than at low line. Therefore, to make the maximum output power close at different input voltages, the controller needs to regulate  $V_{LIMIT}$  of the CSPWM pin to control the PWM switch current.

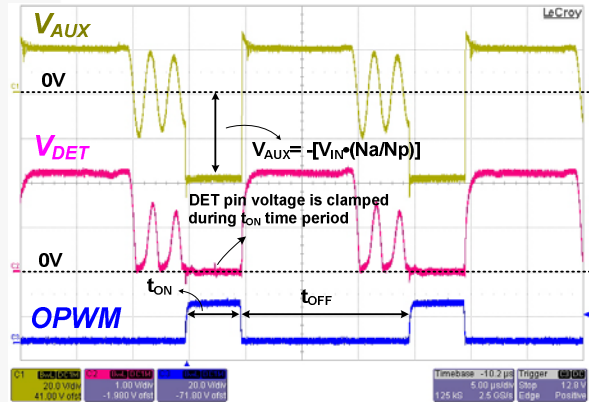
Referring to Figure 41, during the on time of the PWM switch, the input voltage is applied to primary winding and the voltage across on auxiliary winding,  $V_{AUX}$ , is proportional to primary winding voltage. As the input voltage increases, the reflected voltage on auxiliary winding  $V_{AUX}$  rises as well. FAN6921ML also clamps the DET pin voltage and flows out a current  $I_{DET}$ . Since the current,  $I_{DET}$ , is in accordance with  $V_{AUX}$ , FAN6921ML can depend on this current  $I_{DET}$  during PWM on time to regulate the current limit level of the PWM switch to perform high / low line over-power compensation.

As the input voltage increases, the reflected voltage on the auxiliary winding,  $V_{AUX}$ , becomes higher (as well as the current  $I_{DET}$ ) and the controller regulates the  $V_{LIMIT}$  to a lower level.

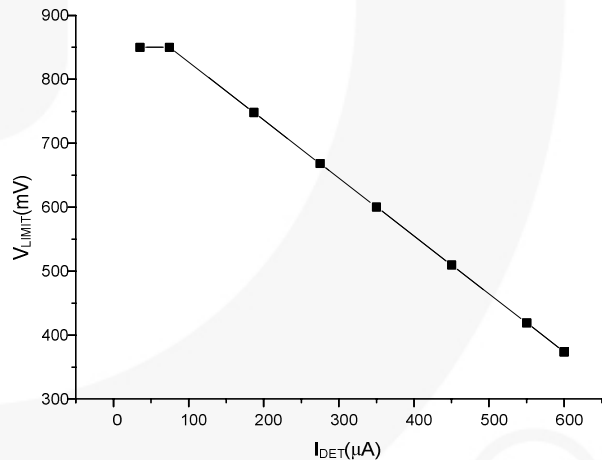
The  $R_{DET}$  resistor is connected from auxiliary winding to the DET pin. Engineers can adjust this  $R_{DET}$  resistor to get proper  $V_{LIMIT}$  voltage to fit power system needs. The characteristic curve of  $I_{DET}$  current vs.  $V_{LIMIT}$  voltage on CSPWM pin is shown in Figure 42.

$$I_{DET} = \left[ V_{IN} \times \left( \frac{N_A}{N_P} \right) \right] / R_{DET} \quad (1)$$

where  $V_{IN}$  is input voltage;  $N_A$  is turn number of auxiliary winding; and  $N_P$  is turn number of primary winding.



**Figure 41. Relationship between  $V_{AUX}$  and  $V_{IN}$**



**Figure 42.  $I_{DET}$  Current vs.  $V_{LIMIT}$  Voltage Characteristic Curve**

#### Leading-Edge Blanking (LEB)

When the PFC or PWM switches are turned on, a voltage spike is induced on the current-sense resistor due to the reciprocal effect by reverse recovery energy of the output diode and  $C_{OSS}$  of power MOSFET. To prevent this spike, a leading-edge blanking time is built-in and a small RC filter is recommended between the CSPWM pin and GND (e.g. 100Ω, 470pF).

## Protection for PWM Stage

### VDD Pin Over-Voltage Protection (OVP)

V<sub>DD</sub> over-voltage protection is used to prevent device damage once V<sub>DD</sub> voltage is higher than device stress rating voltage. In case of V<sub>DD</sub> OVP, the controller stops all switching operation immediately and enters latch-off mode until the AC plug is removed.

### Adjustable Over-Temperature Protection and Externally Latch Triggering (RT Pin)

Figure 43 is a typical application circuit with an internal block of RT pin. As shown, a constant current I<sub>RT</sub> flows out from the RT pin, so the voltage V<sub>RT</sub> on RT pin can be obtained as I<sub>RT</sub> current multiplied by the resistor, which consists of NTC resistor and R<sub>A</sub> resistor. If the RT pin voltage is lower than 0.8V and lasts for a debounce time, latch mode is activated and stops all PFC and PWM switching.

The RT pin is usually used to achieve over-temperature protection with a NTC resistor and provides external latch triggering for additional protection. Engineers can use an external triggering circuit (e.g. transistor) to pull low the RT pin and activate controller latch mode.

Generally, the external latch triggering needs to activate rapidly since it is usually used to protect power system from abnormal conditions. Therefore, the protection debounce time of the RT pin is set to around 100μs once RT pin voltage is lower than 0.5V.

For over-temperature protection, because the temperature would not change immediately; the RT pin voltage is reduced slowly as well. The debounce time for adjustable OTP should not need a fast reaction. To prevent improper latch triggering on the RT pin due to exacting test conditions (e.g. lightning test); when the RT pin triggering voltage is higher than 0.5V, the protection debounce time is set to around 10ms. To avoid improper triggering on the RT pin, it is recommended to add a small value capacitor (e.g. 1000pF) paralleled with NTC and R<sub>A</sub> resistor.

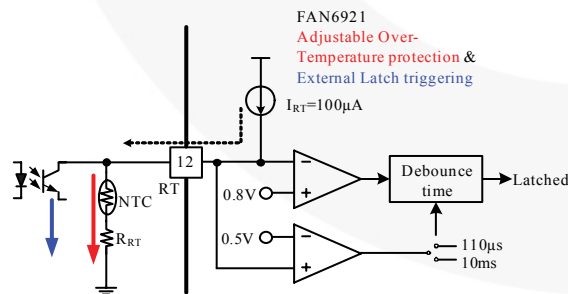


Figure 43. Adjustable Over-Temperature Protection

### Output Over-Voltage Protection (DET Pin)

Referring to Figure 44, during the discharge time of PWM transformer inductor; the voltage across on auxiliary winding is reflected from secondary winding and therefore the flat voltage on the DET pin is proportional to the output voltage. FAN6921ML can sample this flat voltage level after a t<sub>OFF</sub> blanking time to perform output over-voltage protection. This t<sub>OFF</sub> blanking time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampled flat voltage level is compared with internal threshold voltage 2.5V and, once the protection is activated, FAN6921ML enters latch mode.

The controller can protect rapidly by this kind of cycle-by-cycle sampling method in the case of output over voltage. The protection voltage level can be determined by the ratio of external resistor divider R<sub>A</sub> and R<sub>DET</sub>. The flat voltage on DET pin can be expressed by the following equation:

$$V_{DET} = \left( \frac{N_A}{N_S} \right) \times V_o \times \frac{R_A}{R_{DET} + R_A} \quad (2)$$

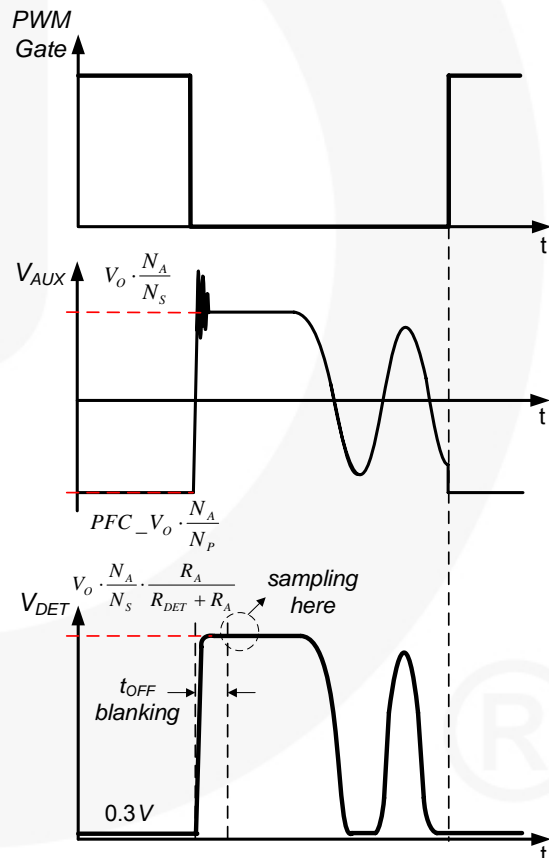
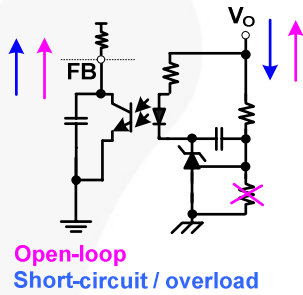


Figure 44. Operation Waveform of Output Over-Voltage Detection

**Open-Loop, Short-Circuit, and Overload Protection (FB Pin)**

Referring to Figure 45, outside of FAN6921ML; the FB pin is connected to the collector of transistor of an opto-coupler. Inside of FAN6921ML, the FB pin is connected to an internal voltage bias through a resistor of ~5kΩ.

As the output loading is increased, the output voltage is decreased and the sink current of transistor of opto-coupler on primary side is reduced. So the FB pin voltage is increased by internal voltage bias. In the case of an open loop, output short circuit, or overload conditions; this sink current is further reduced and the FB pin voltage is pulled to high level by internal bias voltage. When the FB pin voltage is higher than 4.2V for 50ms, the FB pin protection is activated.

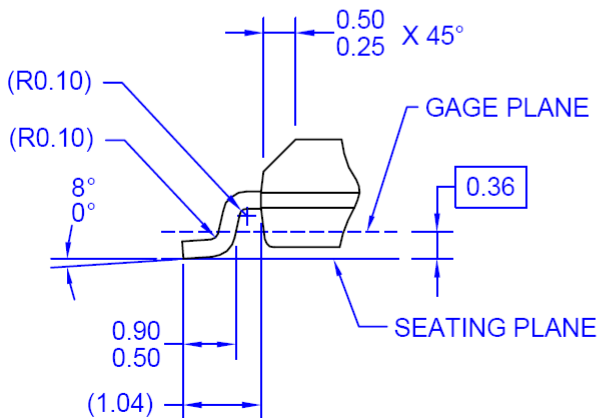
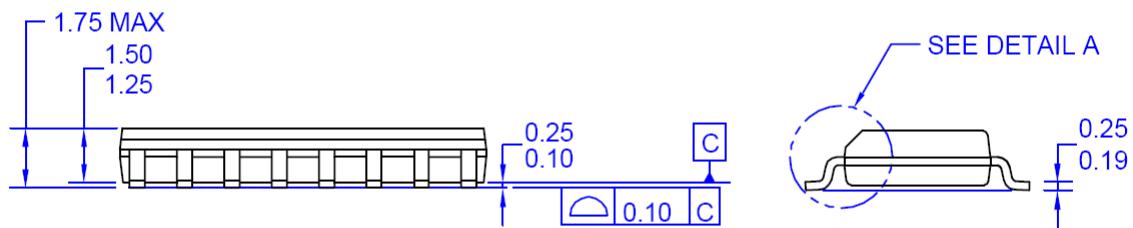
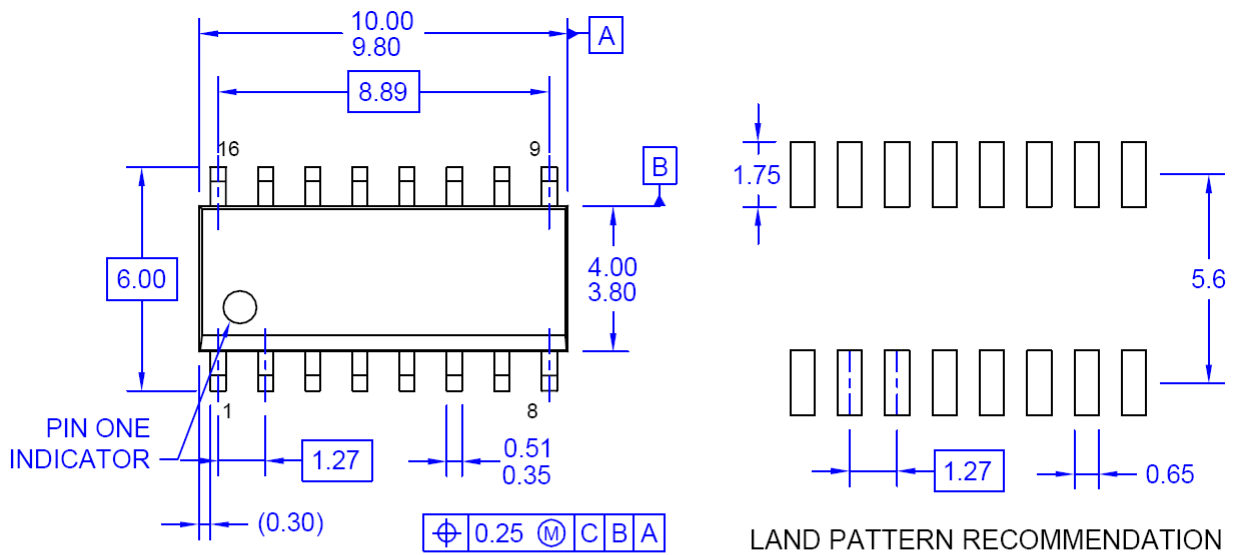


**Figure 45. FB Pin Open-Loop, Short Circuit, and Overload Protections**

**Under-Voltage Lockout (UVLO, VDD Pin)**

Referring to Figure 36 and Figure 37, the turn-on and turn-off  $V_{DD}$  threshold voltages are fixed at 18V and 10V, respectively. During startup, the hold-up capacitor ( $V_{DD}$  capacitor) is charged by the HV startup current until  $V_{DD}$  voltage reaches the turn-on voltage. Before the output voltage rises to rated voltage and delivers energy to the  $V_{DD}$  capacitor from auxiliary winding, this hold-up capacitor has to sustain the  $V_{DD}$  voltage energy for operation. When  $V_{DD}$  voltage reaches turn-on voltage, FAN6921ML starts all switching operation if no protection is triggered before  $V_{DD}$  voltage drops to turn-off voltage  $V_{DD-PWM-OFF}$ .

### Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
- D) CONFORMS TO ASME Y14.5M-1994
- E) LANDPATTERN STANDARD: SOIC127P600X175-16AM
- F) DRAWING FILE NAME: M16AREV12.

**DETAIL A**  
SCALE: 2:1

**Figure 46. 16-Pin Small Outline Package (SOIC)**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
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**Definition of Terms**

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