Data Sheet FN2856.6

3.2μs Sample and Hold Amplifiers

The HA-2420 and HA-2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and JFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note AN517..

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
HA1-2420-2	-55 to 125	14 Ld CERDIP	F14.3
HA3-2425-5	0 to 75	14 Ld PDIP	E14.3

Features

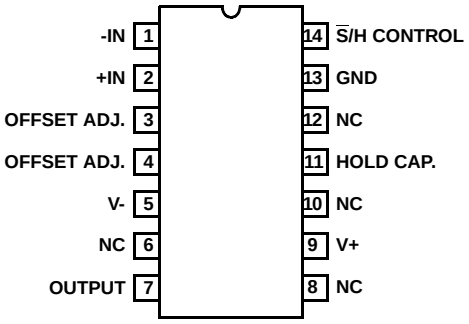
- Maximum Acquisition Time
  - 10V Step to 0.1% . . . . . 4μs (Max)
  - 10V Step to 0.01% . . . . . 6μs (Max)
- Low Droop Rate (C_H = 1000pF). . . . . 5μV/ms (Typ)
- Gain Bandwidth Product . . . . . 2.5MHz (Typ)
- Low Effective Aperture Delay Time . . . . . 30ns (Typ)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Pinout

HA-2420 (CERDIP)
HA-2425 (PDIP)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 24V
Digital Input Voltage (Sample and Hold Pin) . . . . . +8V, -15V
Output Current . . . . . .Short Circuit Protected

Operating Conditions

Temperature Range
HA-2420-2 . . . . . -55^oC to 125^oC
HA-2425-5 . . . . . 0^oC to 75^oC
Supply Voltage Range (Typical) . . . . . ±12V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	95	N/A

Maximum Junction Temperature (Ceramic Packages) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input)

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-2420-2			HA-2425-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Offset Voltage		25	-	2	4	-	3	6	mV
		Full	-	3	6	-	4	8	mV
Bias Current		25	-	40	200	-	40	200	nA
		Full	-	-	400	-	-	400	nA
Offset Current		25	-	10	50	-	10	50	nA
		Full	-	-	100	-	-	100	nA
Input Resistance		25	5	10	-	5	10	-	MΩ
Common Mode Range		Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	R_L = 2kΩ, V_O = $20V_{P-P}$	Full	25	50	-	25	50	-	kV/V
Common Mode Rejection	V_{CM} = ±10V	Full	80	90	-	74	90	-	dB
Hold Mode Feedthrough Attenuation (Note 2)	f_{IN} ≤ 100kHz	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 2)		25	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 2kΩ	Full	±10	-	-	±10	-	-	V
Output Current		25	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Note 2)	V_O = $20V_{P-P}$	25	-	100	-	-	100	-	kHz
Output Resistance	DC	25	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE									
Rise Time (Note 2)	V_O = $200mV_{P-P}$	25	-	75	100	-	75	100	ns
Overshoot (Note 2)	V_O = $200mV_{P-P}$	25	-	25	40	-	25	40	%
Slew Rate (Note 2)	V_O = $10V_{P-P}$	25	3.5	5	-	3.5	5	-	V/µs

Electrical Specifications

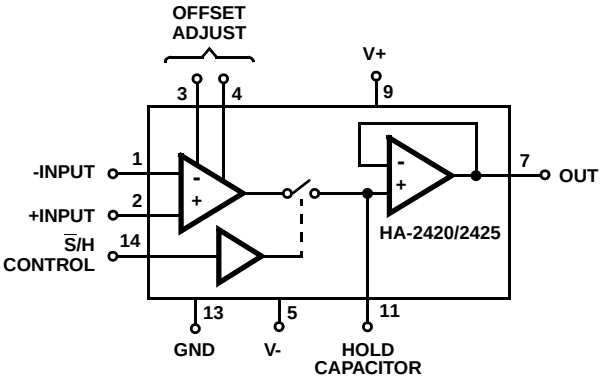
Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input) **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2420-2			HA-2425-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT CHARACTERISTICS									
Digital Input Current	V_{IN} = 0V	Full	-	-	-0.8	-	-	-0.8	mA
	V_{IN} = 5V	Full	-	-	20	-	-	20	µA
Digital Input Voltage	Low	Full	-	-	0.8	-	-	0.8	V
	High	Full	2.0	-	-	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS									
Acquisition Time (Note 2)	To 0.1% 10V Step	25	-	2.3	4	-	2.3	4	µs
Acquisition Time (Note 2)	To 0.01% 10V Step	25	-	3.2	6	-	3.2	6	µs
Hold Step Error	V_{IN} = 0V	25	-	10	20	-	10	20	mV
Hold Mode Settling Time	To ±1mV	25	-	860	-	-	860	-	ns
Aperture Time (Note 3)		25	-	30	-	-	30	-	ns
Effective Aperture Delay Time		25	-	30	-	-	30	-	ns
Aperture Uncertainty		25	-	5	-	-	5	-	ns
Drift Current (Note 2)	V_{IN} = 0V	25	-	5	-	-	5	-	pA
HA1-2420		Full	-	1.8	10	-	-	-	nA
HA1-2425		Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425, HA9P2425		Full	-	-	-	-	7.5	10.0	nA
POWER SUPPLY CHARACTERISTICS									
Supply Current (+)		25	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)		25	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection		Full	80	90	-	74	90	-	dB

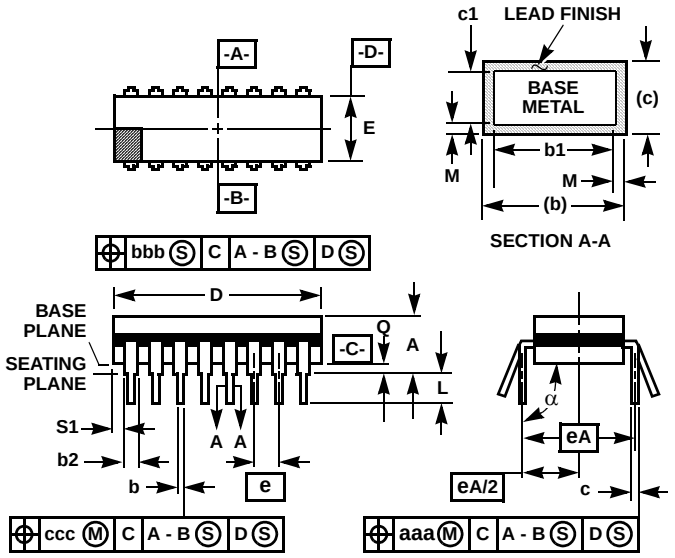
NOTES:

2. A_V = ±1, R_L = 2kΩ, C_L = 50pF.
3. Derived from computer simulation only; not tested.

Functional Diagram



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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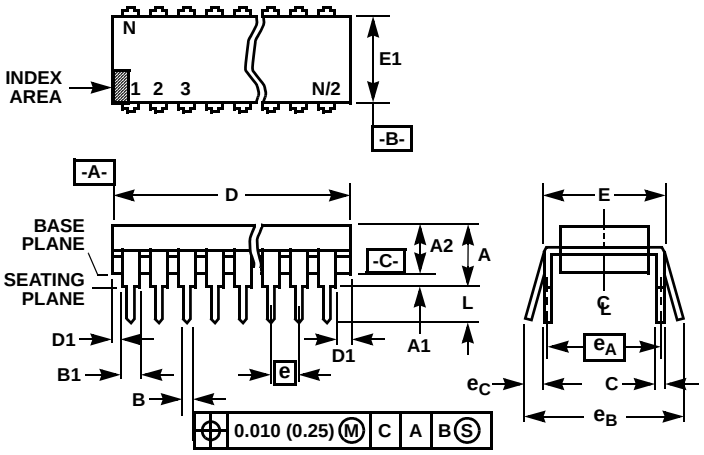
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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