

FEATURES

- Low on resistance (300 Ω typical)
- Fast switching times
 - t_{ON} 250 ns maximum
 - t_{OFF} 250 ns maximum
- Low power dissipation (3.3 mW maximum)
- Fault and overvoltage protection (-40 V to $+55$ V)
- All switches off with power supply off
- Analog output of on channel clamped within power supplies if an overvoltage occurs
- Latch-up proof construction
- Break-before-make construction
- TTL and CMOS compatible inputs

APPLICATIONS

- Existing multiplexer applications (both fault-protected and nonfault-protected)
- New designs requiring multiplexer functions

GENERAL DESCRIPTION

The ADG508F, ADG509F, and ADG528F¹ are CMOS analog multiplexers, with the ADG508F and ADG528F comprising eight single channels and the ADG509F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from -40 V to $+55$ V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources that drive the multiplexer.

The ADG508F and ADG528F switch one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG509F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. The ADG528F has on-chip address and control latches that facilitate microprocessor

FUNCTIONAL BLOCK DIAGRAMS

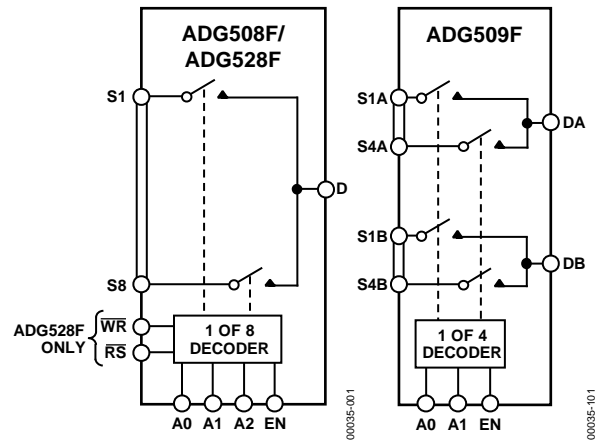


Figure 1.

interfacing. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off.

PRODUCT HIGHLIGHTS

1. Fault Protection.
The ADG508F/ADG509F/ADG528F can withstand continuous voltage inputs from -40 V to $+55$ V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. On channel turns off while fault exists.
3. Low R_{ON} .
4. Fast switching times.
5. Break-before-make switching.
Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench isolation eliminates latch-up.
A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

¹ Protected by U.S. Patent No. 5,389, 811.

Rev. E

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REVISION HISTORY

7/09—Rev. D: Rev. E

Updated Format	Universal
Added TSSOP	Universal
Updated Outline Dimensions	15
Changes to Ordering Guide	18

4/01—Data Sheet Changed from Rev. C to Rev. D.

Changes to Ordering Guide	1
Changes to Specifications Table.....	2
Max Ratings Changed	4
Deleted 16-Lead Cerdip from Outline Dimensions	11
Deleted 18-Lead Cerdip from Outline Dimensions	12

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		$V_{SS} + 3$ $V_{DD} - 1.5$	V min V max	
R_{ON}	300	350	Ω typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$, $I_S = 1\text{ mA}$; $V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$
		400	Ω max	$-10\text{ V} \leq V_S \leq +10\text{ V}$, $I_S = 1\text{ mA}$; $V_{DD} = +15\text{ V} \pm 5\%$, $V_{SS} = -15\text{ V} \pm 5\%$
R_{ON} Drift	0.6		%/°C typ	$V_S = 0\text{ V}$, $I_S = 1\text{ mA}$
R_{ON} Match	5		% max	$V_S = 0\text{ V}$, $I_S = 1\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.02		nA typ	$V_D = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; See Figure 22
	± 1	± 50	nA max	
Drain OFF Leakage I_D (OFF)	± 0.04		nA typ	$V_D = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; See Figure 23
ADG508F/ADG528F	± 1	± 60	nA max	
ADG509F	± 1	± 30	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.04		nA typ	$V_S = V_D = \pm 10\text{ V}$; See Figure 24
ADG508F/ADG528F	± 1	± 60	nA max	
ADG509F	± 1	± 30	nA max	
FAULT				
Output Leakage Current (With Overvoltage)	± 0.02		nA typ	$V_S = \pm 33\text{ V}$, $V_D = 0\text{ V}$, see Figure 23
	± 2	± 2	μA max	
Input Leakage Current (With Overvoltage)	± 0.005		μA typ	$V_S = \pm 25\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 25
	± 2		μA max	
Input Leakage Current (With Power Supplies OFF)	± 0.001		μA typ	$V_S = \pm 25\text{ V}$, $V_D = V_{EN} = A0, A1, A2 = 0\text{ V}$ See Figure 26
	± 2		μA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}		± 1	μA max	$V_{IN} = 0$ or V_{DD}
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS¹				
$t_{TRANSITION}$	200		ns typ	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$; $V_{S1} = \pm 10\text{ V}$, $V_{S8} = \mp 10\text{ V}$; see Figure 27
	300	400	ns max	
t_{OPEN}	50		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 28
	25	10	ns min	
t_{ON} (\overline{EN} , \overline{WR})	200		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 29
	250	400	ns max	
t_{OFF} (\overline{EN} , \overline{RS})	200		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 29
t_{SETT} , Settling Time	250	400	ns max	
0.1%		1	μs typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = 5\text{ V}$
0.01%		2.5	μs typ	
ADG528F Only				
t_W , Write Pulse Width	100	120	ns min	
t_S , Address, Enable Setup Time		100	ns min	
t_H , Address, Enable Hold Time		10	ns min	
t_{RS} , Reset Pulse Width		100	ns min	

ADG508F/ADG509F/ADG528F

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
Charge Injection	4		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 32 $R_L = 1\ \text{k}\Omega$, $C_L = 15\ \text{pF}$, $f = 100\ \text{kHz}$; $V_S = 7\ \text{V rms}$; see Figure 33
OFF Isolation	68		dB typ	
	50		dB min	
C_S (OFF)	5		pF typ	
C_D (OFF)				
ADG508F/ADG528F	50		pF typ	
ADG509F	25		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.1	0.2	mA max	$V_{IN} = 0\text{ V or }5\text{ V}$
I_{SS}	0.1	0.1	mA max	

¹ Guaranteed by design, not subject to production test.

TRUTH TABLES

Table 2. ADG508F Truth Table

A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table 3. ADG509F Truth Table

A1	A0	EN	ON Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

Table 4. ADG528F Truth Table

A2	A1	A0	EN	\overline{WR}	\overline{RS}	ON Switch
X	X	X	X	1	1	Retains previous switch condition
X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

TIMING DIAGRAMS

Figure 2 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while \overline{WR} is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of \overline{WR} .

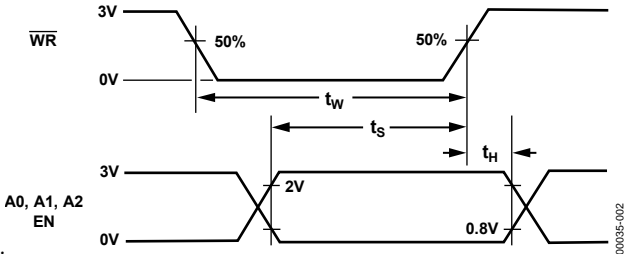


Figure 2. ADG528F Timing Sequence for Latching the Switch Address and Enable Inputs

Figure 3 shows the reset pulsewidth, t_{RS} , and the reset turnoff time, $t_{OFF}(\overline{RS})$. Note that all digital input signals rise and fall times are measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

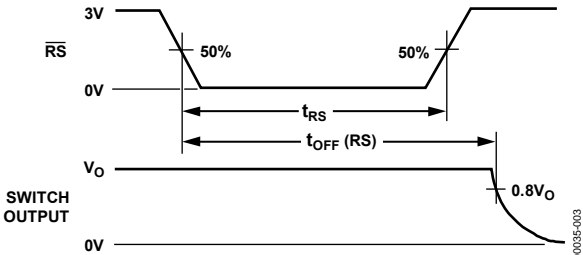


Figure 3. ADG528F Reset Pulse Width

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C unless otherwise noted.

Table 5.

Parameter	Rating
V _{DD} to V _{SS}	44 V
V _{DD} to GND	−0.3 V to +25 V
V _{SS} to GND	+0.3 V to −25 V
Digital Input, EN, Ax	−0.3 V to V _{DD} + 2 V or 20 mA, whichever occurs first
V _S , Analog Input Overvoltage with Power On	V _{SS} − 25 V to V _{DD} + 40 V
V _S , Analog Input Overvoltage with Power Off	−40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature Range Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP	
θ _{JA} , Thermal Impedance Plastic Package	112°C/W
θ _{JA} , Thermal Impedance	
16-Lead	117°C/W
18-Lead	110°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package	
θ _{JA} , Thermal Impedance	
Narrow Body	77°C/W
Wide Body	75°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
PLCC Package	
θ _{JA} , Thermal Impedance	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

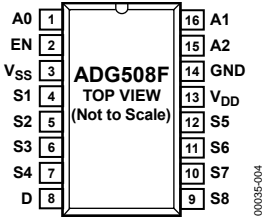


Figure 4. ADG508F Pin Configuration TSSOP/DIP/SOIC

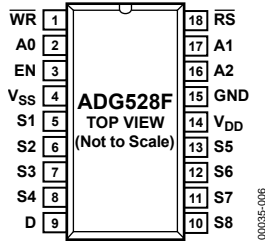


Figure 6. ADG528F Pin Configuration DIP

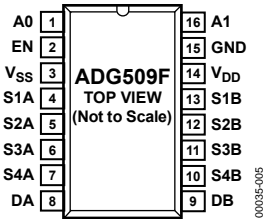


Figure 5. ADG509F Pin Configuration TSSOP/DIP/SOIC

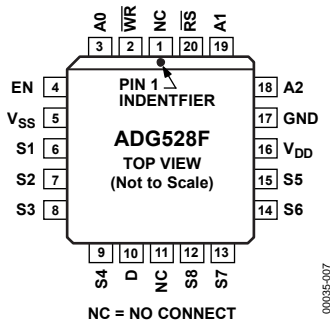


Figure 7. ADG528F Pin Configuration PLCC

TYPICAL PERFORMANCE CHARACTERISTICS

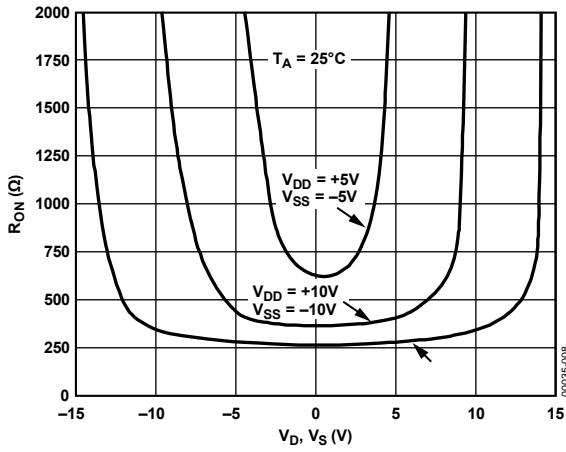


Figure 8. On Resistance as a Function of V_D (V_S)

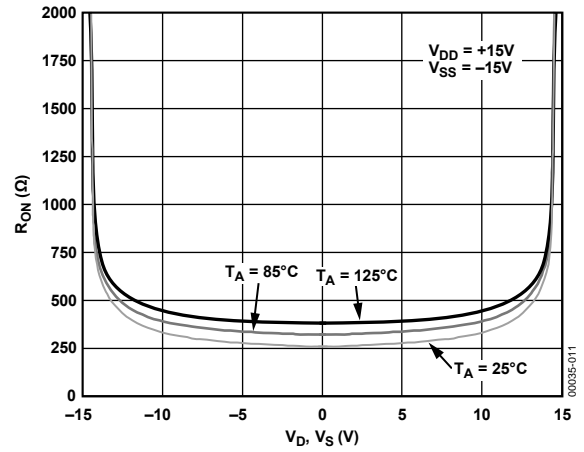


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures

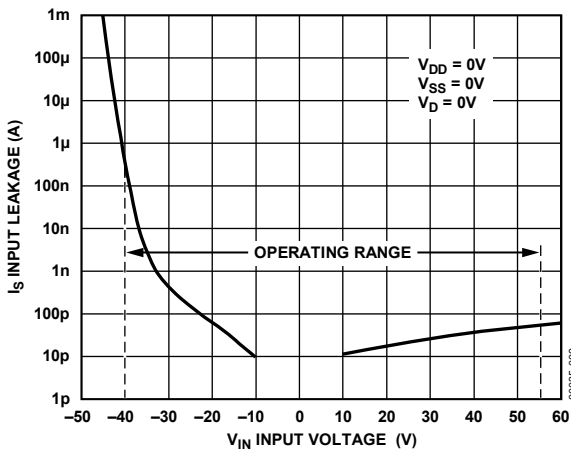


Figure 9. Input Leakage Current as a Function of V_S (Power Supplies Off) During Overvoltage Conditions

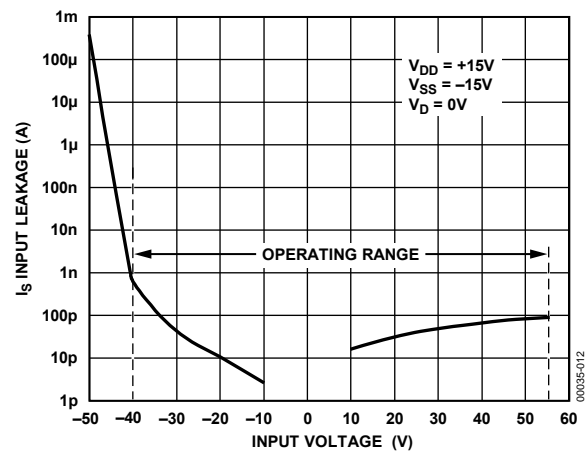


Figure 12. Input Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

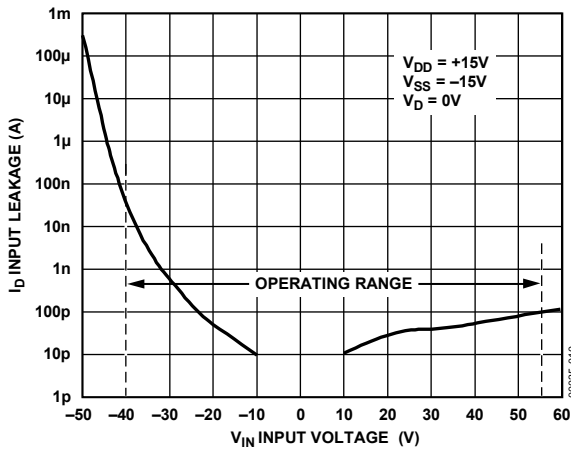


Figure 10. Output Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

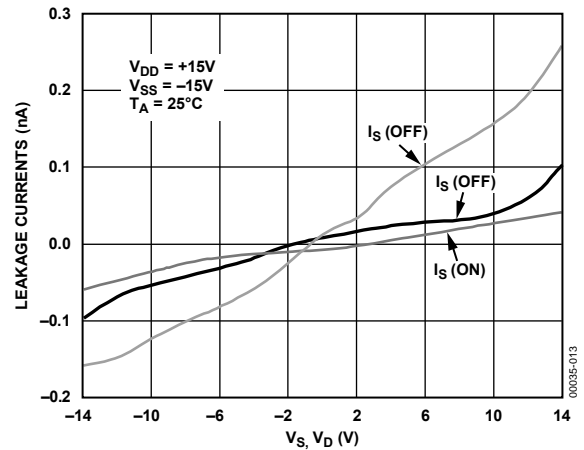


Figure 13. Leakage Currents as a Function of V_D (V_S)

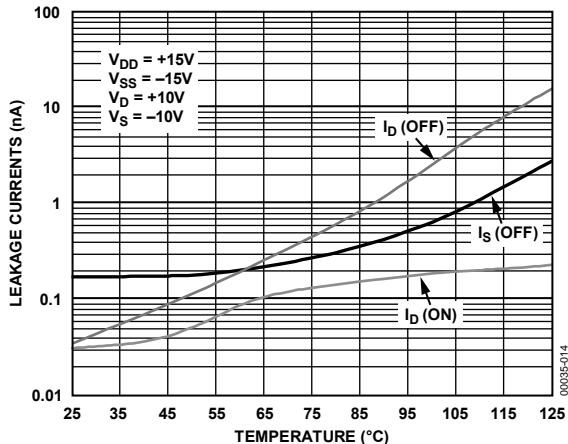


Figure 14. Leakage Currents as a Function of Temperature

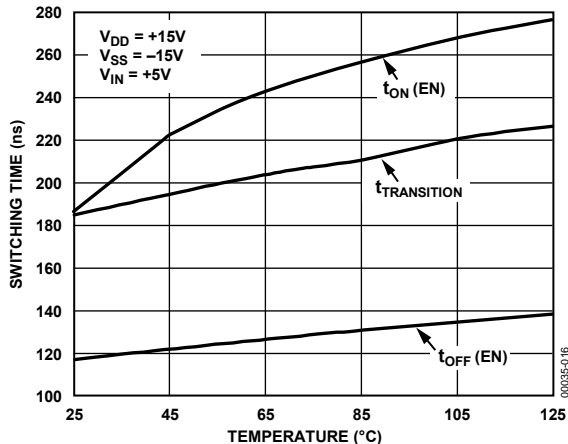


Figure 16. Switching Time vs. Temperature

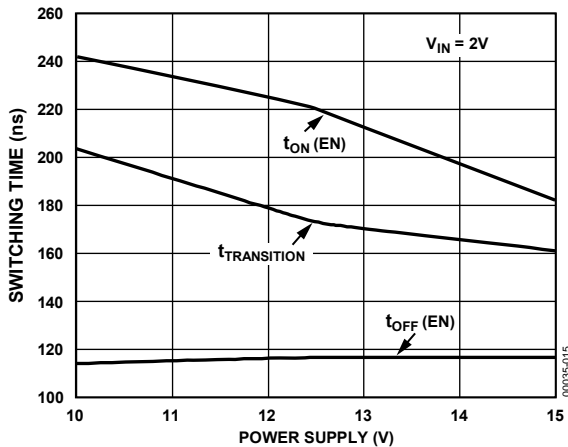


Figure 15. Switching Time vs. Power Supply

TERMINOLOGY

V_{DD} Most Positive Power Supply Potential.	t_{ON} (EN) Delay time between the 50% and 90% points of the digital input and switch on condition.
V_{SS} Most Negative Power Supply Potential.	t_{OFF} (EN) Delay time between the 50% and 90% points of the digital input and switch off condition.
GND Ground (0 V) Reference.	t_{TRANSITION} Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.
R_{ON} Ohmic Resistance between D and S.	t_{OPEN} “OFF” time measured between 80% points of both switches when switching from one address state to another.
R_{ON} Drift Change in R _{ON} when temperature changes by one degree Celsius.	V_{INL} Maximum input voltage for Logic 0.
R_{ON} Match Difference between the R _{ON} of any two channels.	V_{INH} Minimum input voltage for Logic 1.
I_S (OFF) Source leakage current when the switch is off.	I_{INL} (I_{INH}) Input current of the digital input.
I_D (OFF) Drain leakage current when the switch is off.	Off Isolation A measure of unwanted signal coupling through an off channel.
I_D, I_S (ON) Channel leakage current when the switch is on.	Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching.
V_D (V_S) Analog Voltage on Terminals D, S.	I_{DD} Positive Supply Current.
C_S (OFF) Channel input capacitance for off condition.	I_{SS} Negative Supply Current.
C_D (OFF) Channel output capacitance for off condition.	
C_D, C_S (ON) On Switch Capacitance.	
C_{IN} Digital Input Capacitance.	

THEORY OF OPERATION

The ADG508F/ADG509F/ADG528F multiplexers are capable of withstanding overvoltages from -40 V to $+55\text{ V}$, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will switch off, limiting the current to submicroamp levels, thereby preventing the overvoltage from damaging any circuitry following the multiplexer. Figure 17 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of $V_{SS} + 3\text{ V}$ to $V_{DD} - 1.5\text{ V}$ is applied to the ADG508F/ADG509F/ADG528F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is $400\ \Omega$ maximum. However, when an overvoltage is applied to the device, one of the three MOSFETs will turn off.

Figure 17 to Figure 20 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an ON channel approaches the positive power supply line, the n-channel MOSFET turns OFF since the voltage on the analog input exceeds the difference between V_{DD} and the n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET will turn off since the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}). Since V_{TN} is nominally 1.5 V and V_{TP} is typically 3 V , the analog input range to the multiplexer is limited to -12 V to $+13.5\text{ V}$ when a $\pm 15\text{ V}$ power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will turn off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off since the gate to source voltage applied to this MOSFET is negative.

During fault conditions, the leakage current into and out of the ADG508F/ADG509F/ADG528F is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.

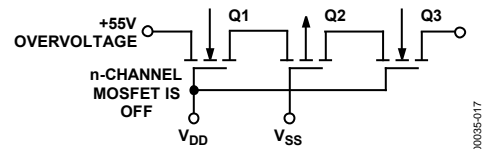


Figure 17. +55 V Overvoltage Input to the On Channel

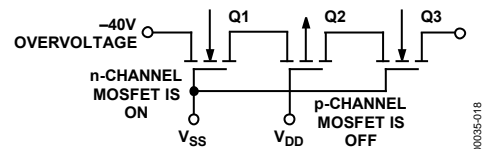


Figure 18. -40 V Overvoltage on an Off Channel with Multiplexer Power On

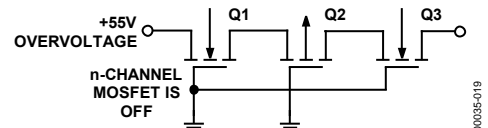


Figure 19. +55 V Overvoltage with Power Off

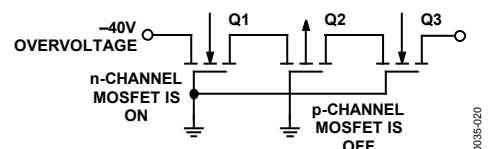


Figure 20. -40 V Overvoltage with Power Off

TEST CIRCUITS

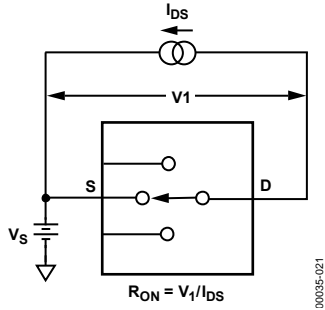


Figure 21. On Resistance

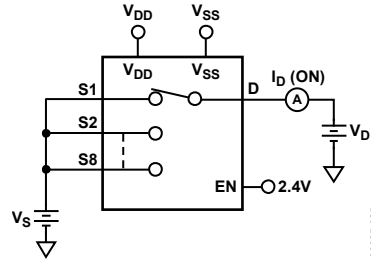


Figure 24. I_D (On)

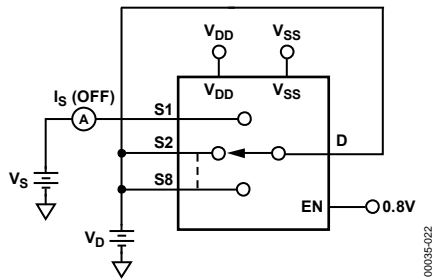


Figure 22. I_S (Off)

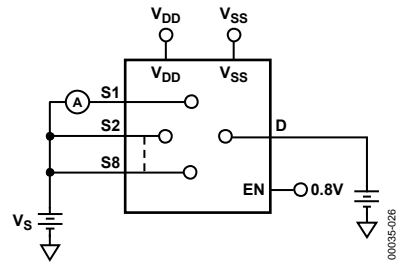


Figure 25. Input Leakage Current (with Overvoltage)

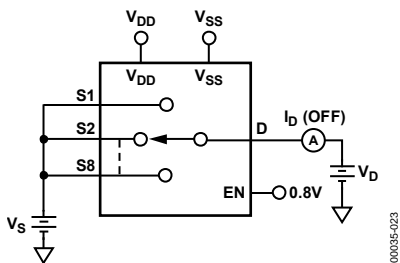


Figure 23. I_D (Off)

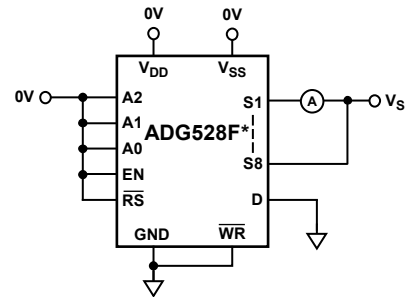


Figure 26. Input Leakage Current (with Power Supplies Off)

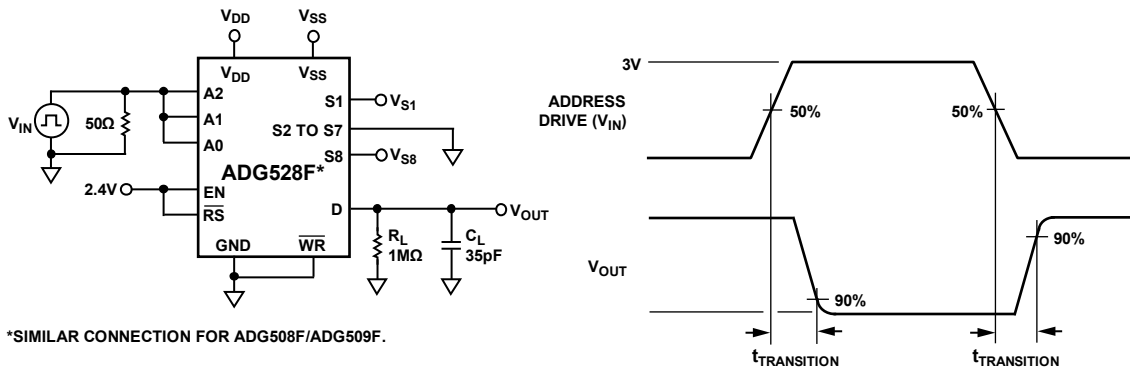


Figure 27. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

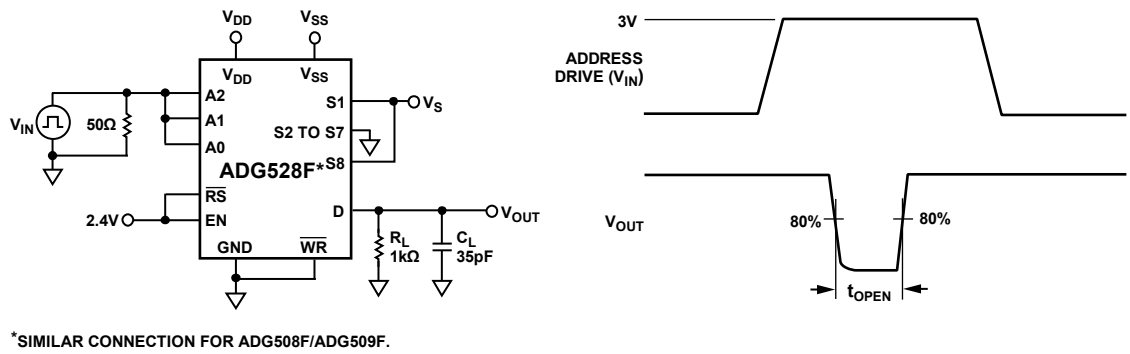


Figure 28. Break-Before-Make Delay, t_{OPEN}

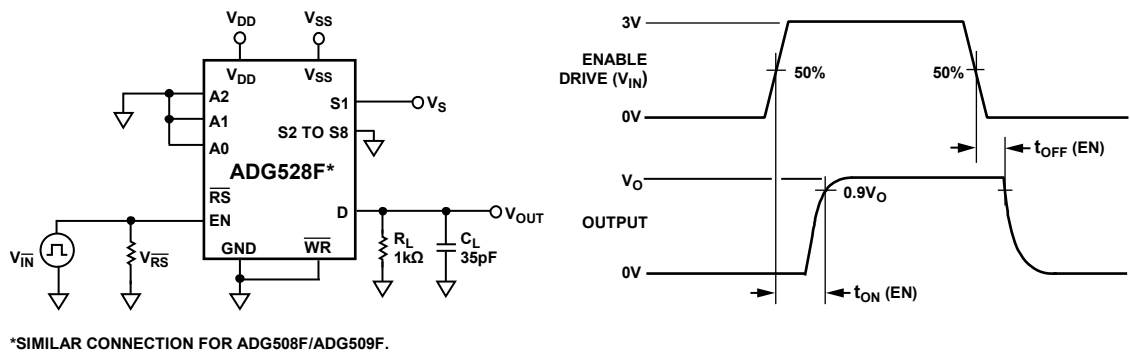


Figure 29. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$

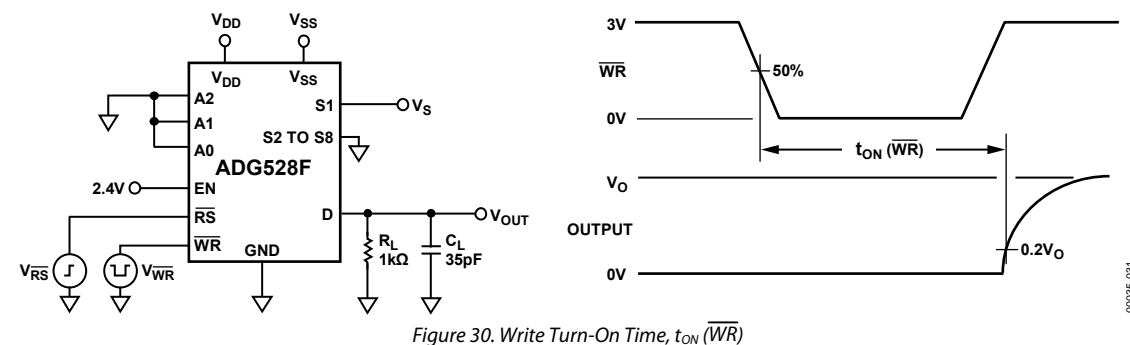
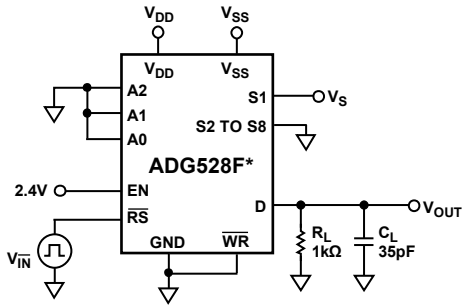


Figure 30. Write Turn-On Time, $t_{\text{ON}}(\overline{\text{WR}})$

ADG508F/ADG509F/ADG528F



*SIMILAR CONNECTION FOR ADG508F/ADG509F.

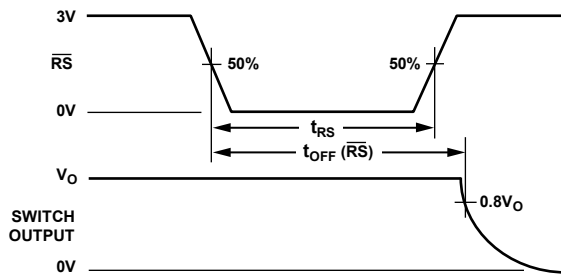
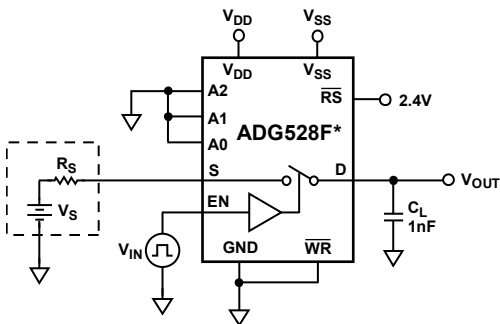


Figure 31. Reset Turn-Off Time, $t_{OFF}(\overline{RS})$

00035-032



*SIMILAR CONNECTION FOR ADG508F/ADG509F.

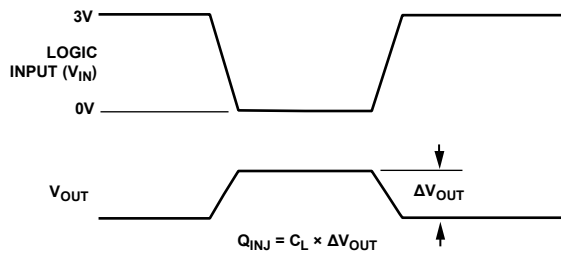
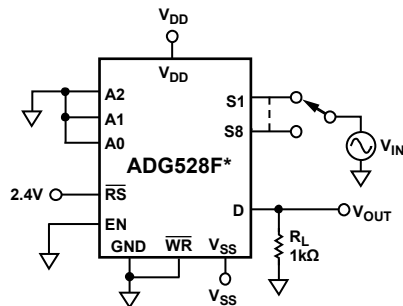


Figure 32. Charge Injection

00035-033

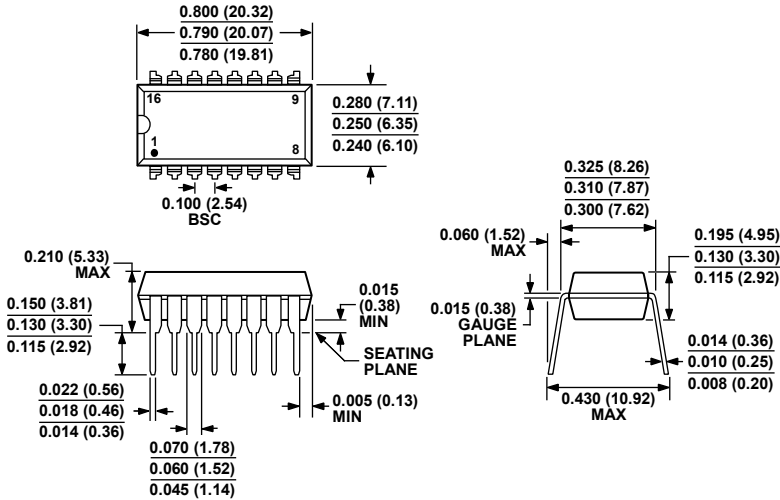


*SIMILAR CONNECTION FOR ADG508F/ADG509F.

Figure 33. Off Isolation

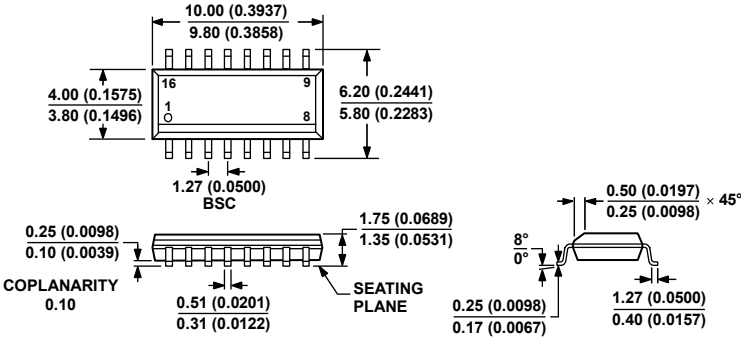
00035-034

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

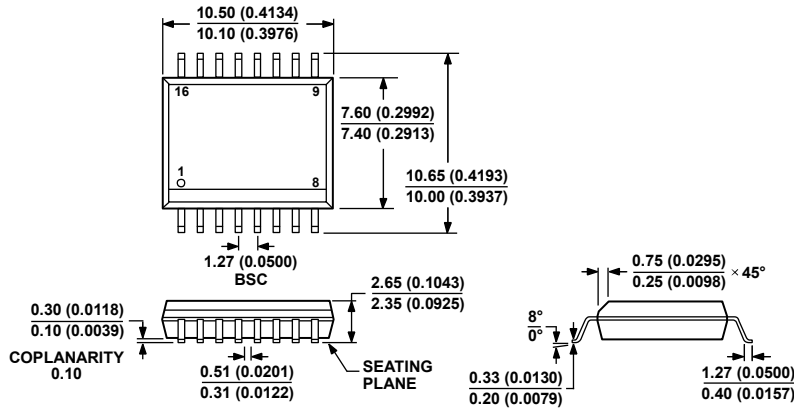
Figure 34. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)
 Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 16-Lead Standard Small Outline Package [SOIC-N] Narrow Body (R-16)
 Dimensions shown in millimeters and (inches)

ADG508F/ADG509F/ADG528F

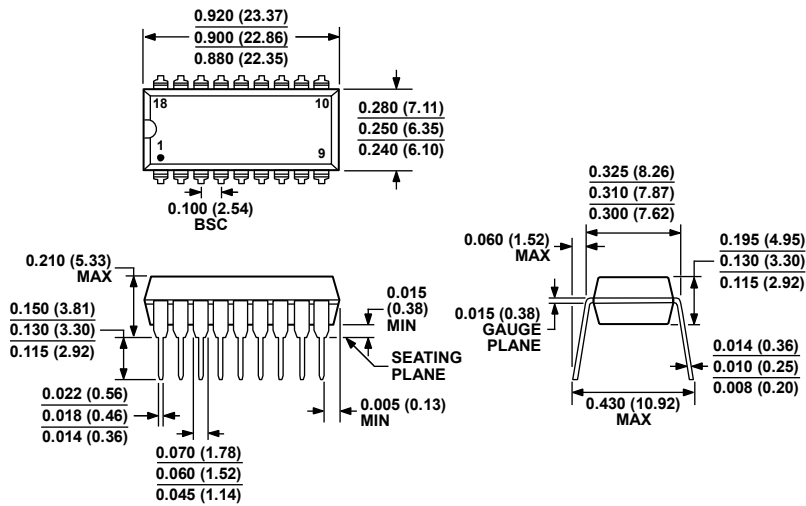


COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 16-Lead Standard Small Outline Package [SOIC-W] Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

032707-B

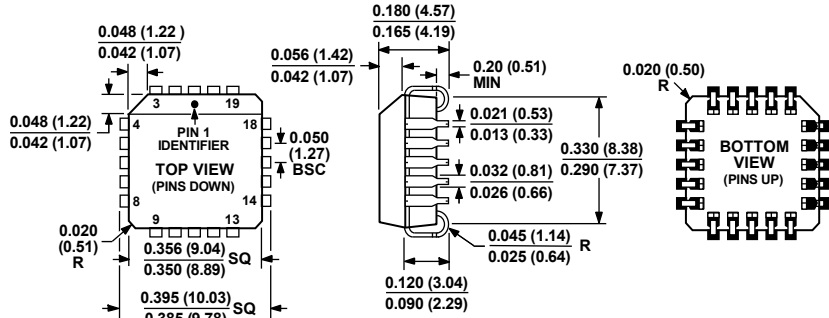


COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 37. 18-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-18)

Dimensions shown in inches and (millimeters)

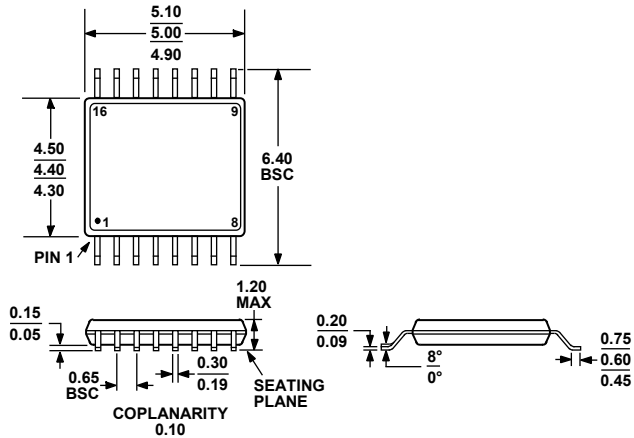
070706-A



COMPLIANT TO JEDEC STANDARDS MO-047-AA
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 20-Lead Plastic Leaded Chip Carrier [PLCC]
 (P-20)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 39. 16-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-16)

Dimensions shown in millimeters

ADG508F/ADG509F/ADG528F

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG508FBN	-40°C to +85°C	16-Lead PDIP	N-16
ADG508FBNZ	-40°C to +85°C	16-Lead PDIP	N-16
ADG508FBRN	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRN-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRW	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRWZ	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRWZ-REEL	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG508FBRUZ-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBN	-40°C to +85°C	16-Lead PDIP	N-16
ADG509FBNZ	-40°C to +85°C	16-Lead PDIP	N-16
ADG509FBRN	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRN-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRW	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRW-REEL	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRWZ	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRWZ-REEL	-40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBRUZ-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG528FBN	-40°C to +85°C	18-Lead PDIP	N-18
ADG528FBNZ	-40°C to +85°C	18-Lead PDIP	N-18
ADG528FBP	-40°C to +85°C	20-Lead PLCC	P-20
ADG528FBP-REEL	-40°C to +85°C	20-Lead PLCC	P-20
ADG528FBPZ	-40°C to +85°C	20-Lead PLCC	P-20

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