International IƏR Rectifier

IRS2184/IRS21844(S)PbF

## HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

Description

The IRS2184/IRS21844 are high voltage, high speed power MOSFET and IGBT drivers with dependent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Packages

8-Lead PDIP
IRS2184

14-Lead PDIP
IRS21844

8-Lead SOIC
IRS2184S

14-Lead SOIC
IRS21844S
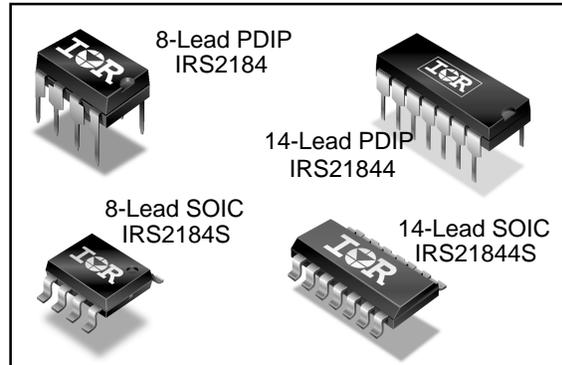
Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	t_{on}/t_{off} (ns)
2181	HIN/LIN	no	none	COM	180/220
21814				Vss/COM	
2183	HIN/$\overline{LIN}$	yes	Internal 400	COM	180/220
21834			Program 400-5000	Vss/COM	
2184	IN/$\overline{SD}$	yes	Internal 400	COM	680/270
21844			Program 400-5000	Vss/COM	

Typical Connection

up to 600 V

IRS2184

(Refer to Lead Assignments for correct configuration).These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

up to 600 V

IRS21844

TO LOAD

IRS2184/IRS21844(S)PbF
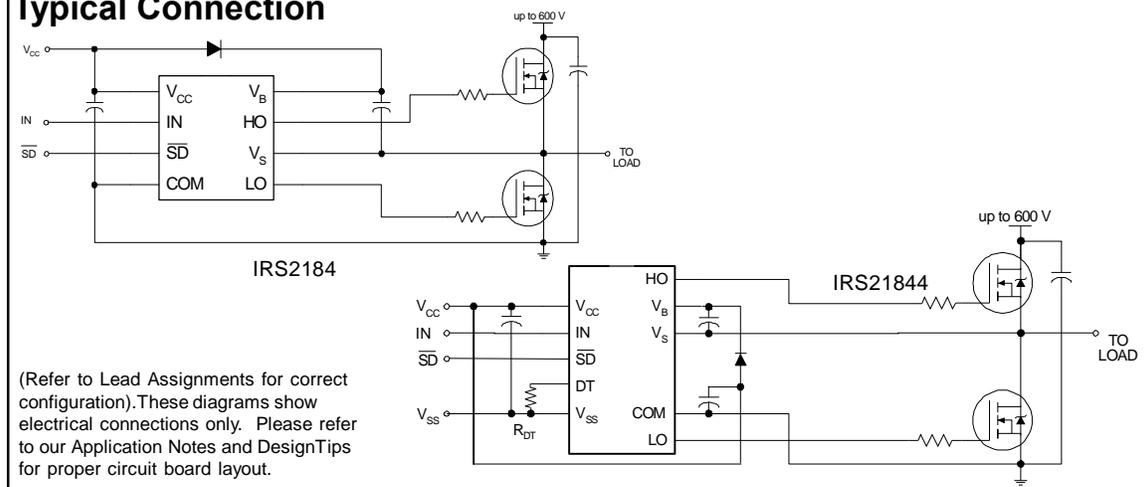
Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	620 (Note 1)	
V_S	High-side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20 (Note 1)	V
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable deadtime pin voltage (IRS21844 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IRS21844 only)		V_{CC} - 20	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$ +25 °C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
$RthJ_A$	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	
T_S	Storage temperature		-50	150	°C
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S + 10	V_S + 20	
V_S	High-side floating supply offset voltage	Note 2	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{CC}	
DT	Programmable deadtime pin voltage (IRS21844 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IRS21844 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25° C, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	900		V_S = 0 V
t_{off}	Turn-off propagation delay	—	270	400		V_S = 0 V or 600 V
t_{sd}	Shut-down propagation delay	—	180	270		
MTon	Delay matching, HS & LS turn-on	—	0	90	ns	
MToff	Delay matching, HS & LS turn-off	—	0	40		
t_r	Turn-on rise time	—	40	60		V_S = 0 V
t_f	Turn-off fall time	—	20	35		
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		R_{DT}= 0 Ω
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µs	R_{DT} = 200 kΩ
MDT	Deadtime matching = $DT_{LO - HO}$ - DT_{HO-LO}	—	0	50	ns	R_{DT}=0 Ω
		—	0	600		R_{DT} = 200 kΩ

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O, and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.5	—	—		V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.5	—	—	V	
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.4		I_O = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.2		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	
I_{IN+}	Logic "1" input bias current	—	25	60	µA	IN = 5 V, $\overline{SD}$ = 0 V
I_{IN-}	Logic "0" input bias current	—	—	5.0		IN = 0 V, $\overline{SD}$ = 5 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V	
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15 V, PW ≤ 10 µs

Functional Block Diagrams
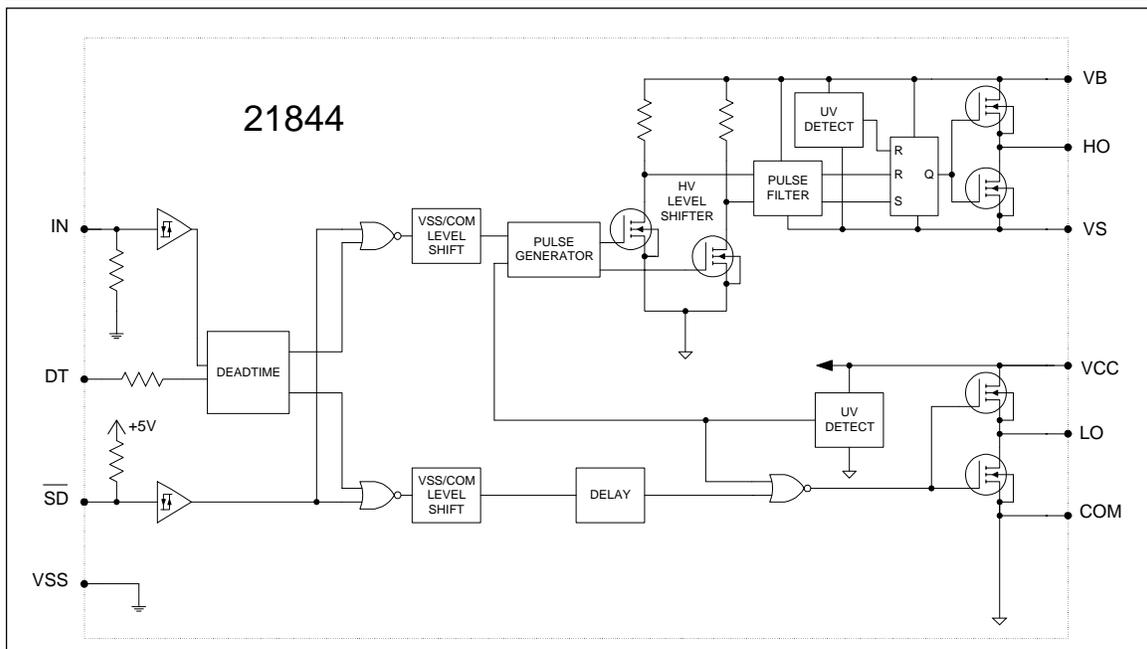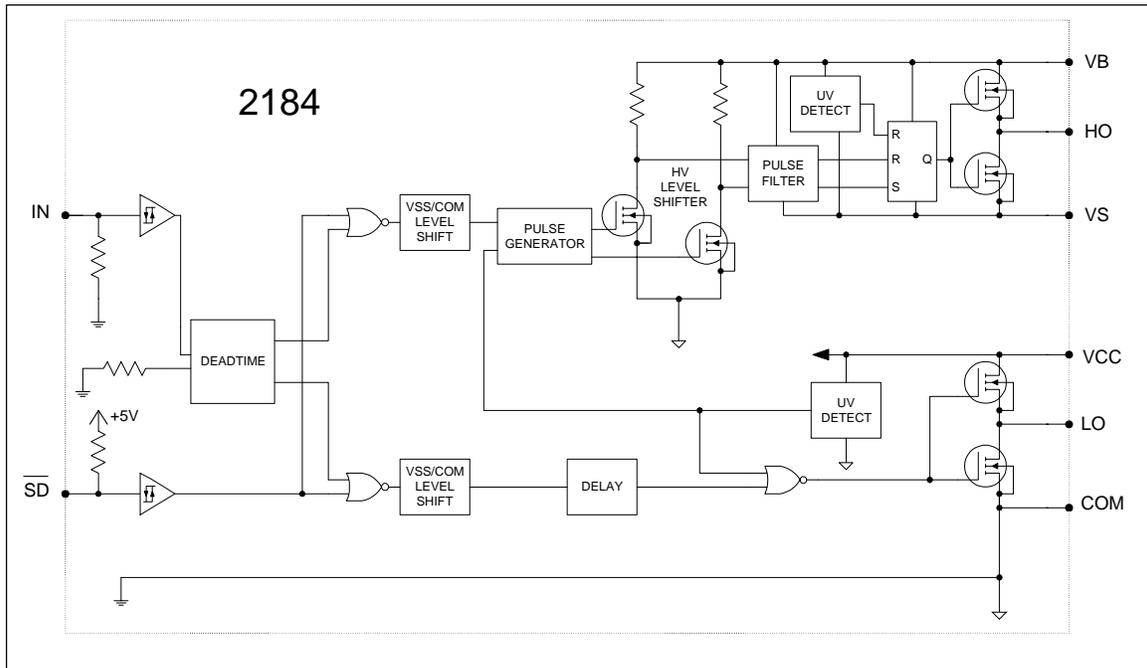
2184

21844

Lead Definitions

Symbol	Description
IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IRS2184 and VSS for IRS21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IRS2184 and VSS for IRS21844)
DT	Programmable deadtime lead, referenced to VSS. (IRS21844 only)
VSS	Logic ground (IRS21844 only)
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments

1 IN — V_B 8 2 $\overline{SD}$ — HO 7 3 COM — V_S 6 4 LO — V_{CC} 5 8-Lead PDIP	1 IN — V_B 8 2 $\overline{SD}$ — HO 7 3 COM — V_S 6 4 LO — V_{CC} 5 8-Lead SOIC
IRS2184PbF	**IRS2184SPbF**
1 IN — 14 2 $\overline{SD}$ — V_B 13 3 VSS — HO 12 4 DT — V_S 11 5 COM — 10 6 LO — 9 7 V_{CC} — 8 14-Lead PDIP	1 IN — 14 2 $\overline{SD}$ — V_B 13 3 VSS — HO 12 4 DT — V_S 11 5 COM — 10 6 LO — 9 7 V_{CC} — 8 14-Lead SOIC
IRS21844PbF	**IRS21844SPbF**
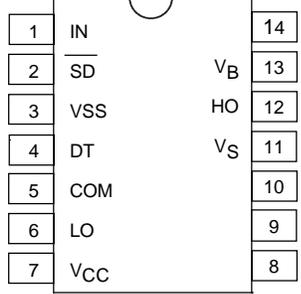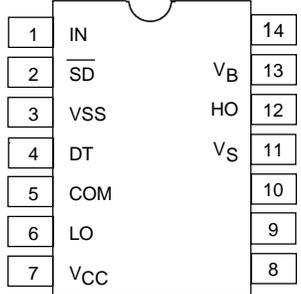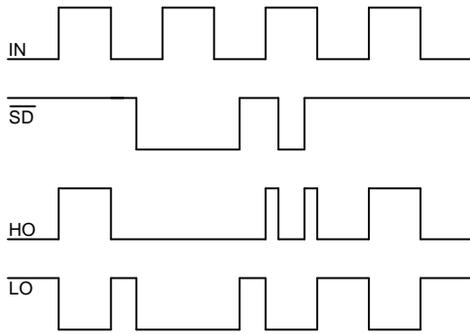
Figure 1. Input/Output Timing Diagram
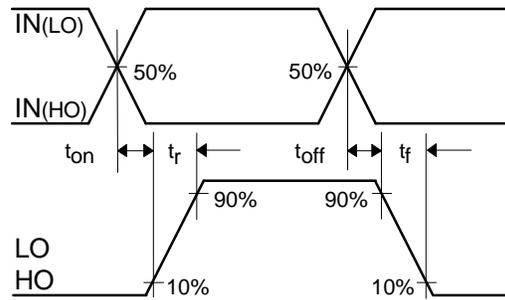
Figure 2. Switching Time Waveform Definitions
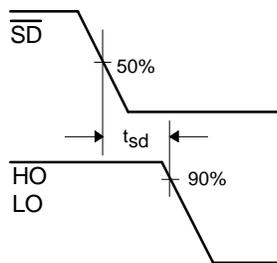
Figure 3. Shutdown Waveform Definitions

$$MDT= \left| DT_{LO-HO} - DT_{HO-LO} \right|$$
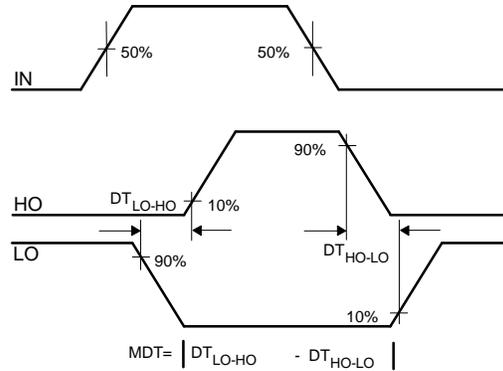
Figure 4. Deadtime Waveform Definitions
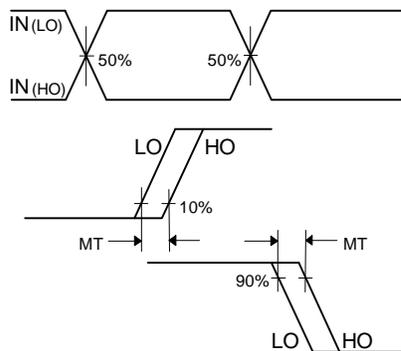
Figure 5. Delay Matching Waveform Definitions
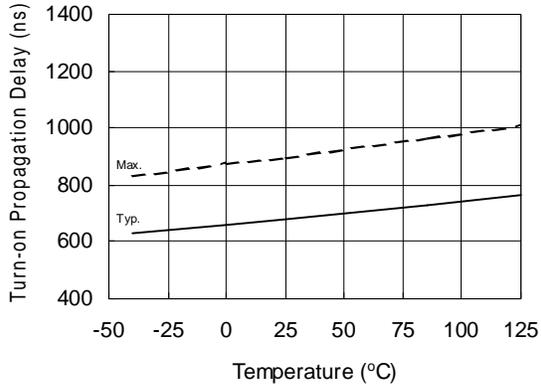
Figure 6A. Turn-On Propagation Delay
vs. Temperature
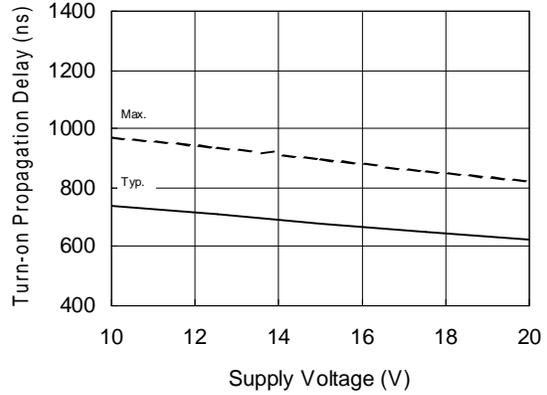
Figure 6B. Turn-On Propagation Delay
vs. Supply Voltage
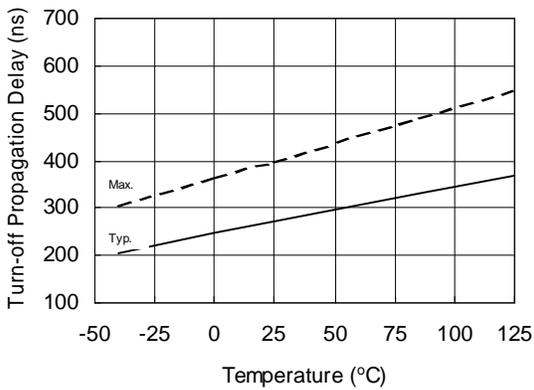
Figure 7A. Turn-Off Propagation Delay
vs. Temperature
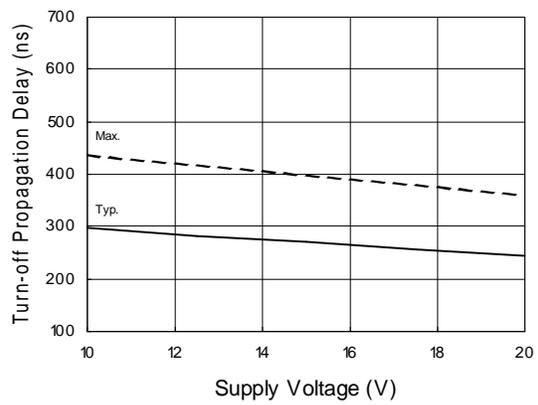
Figure 7B. Turn-Off Propagation Delay
vs. Supply Voltage

IRS2184/IRS21844(S)PbF
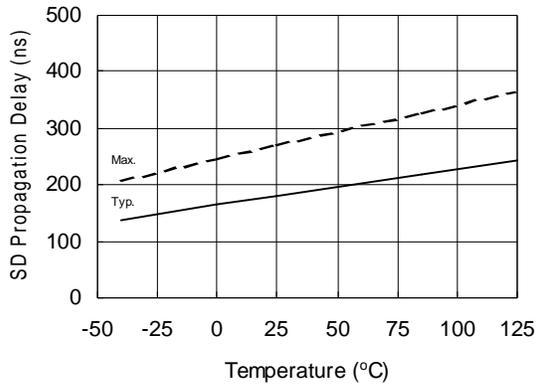
Figure 8A. SD Propagation Delay vs. Temperature
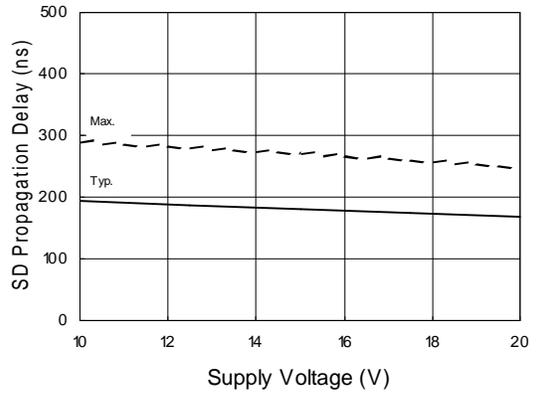
Figure 8B. SD Propagation Delay vs. Supply Voltage
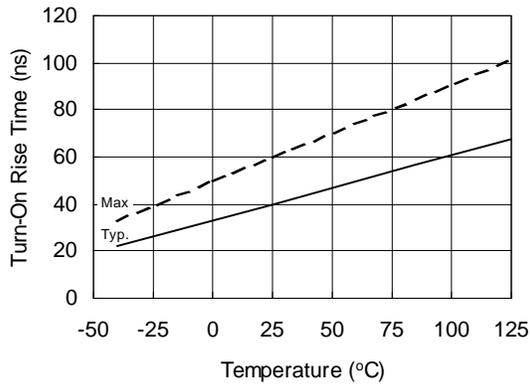
Figure 9A. Turn-On Rise Time vs. Temperature
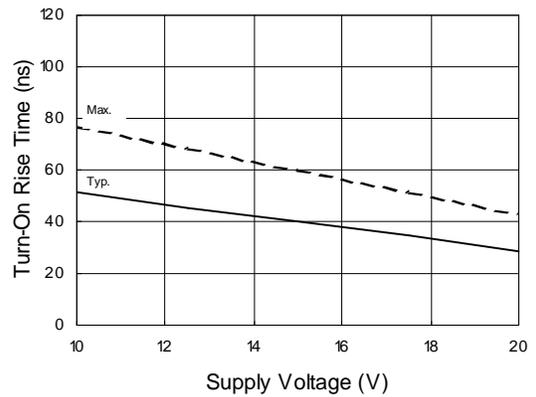
Figure 9B. Turn-On Rise Time vs. Supply Voltage
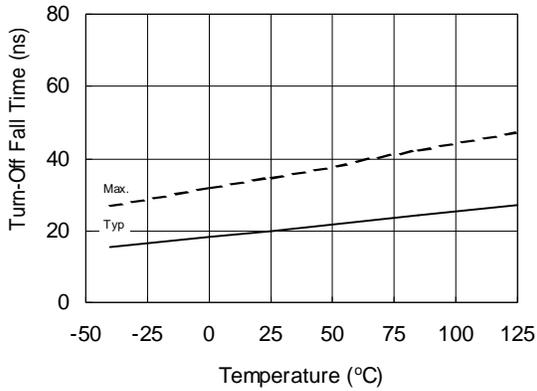
Figure 10A. Turn-Off Fall Time vs. Temperature
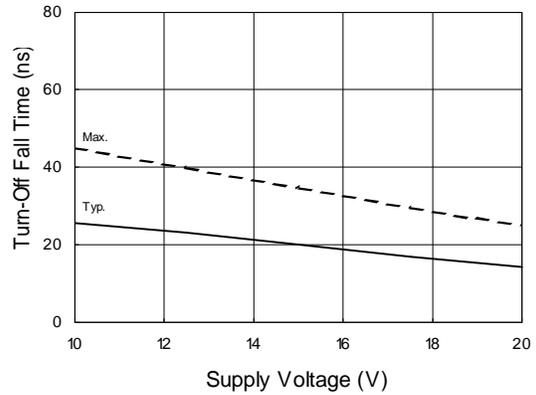
Figure 10B. Turn-Off Fall Time vs. Supply Voltage
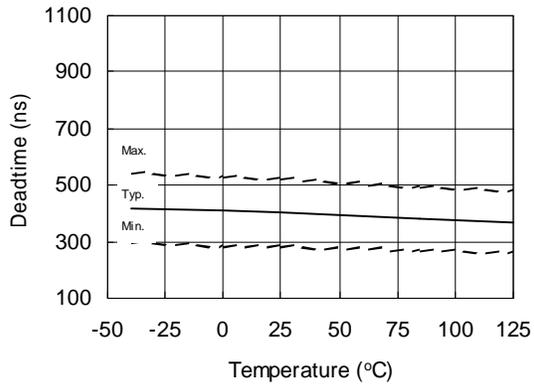
Figure 11A. Deadtime vs. Temperature
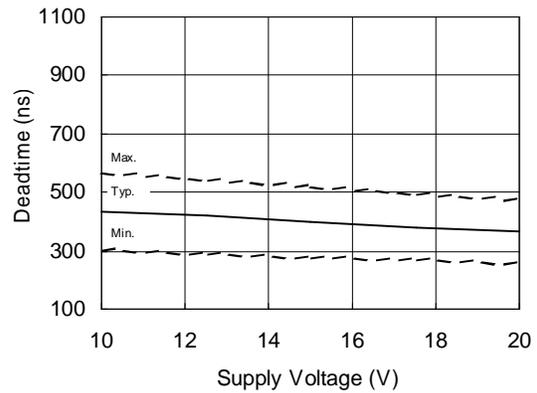
Figure 11B. Deadtime vs. Supply Voltage

IRS2184/IRS21844(S)PbF
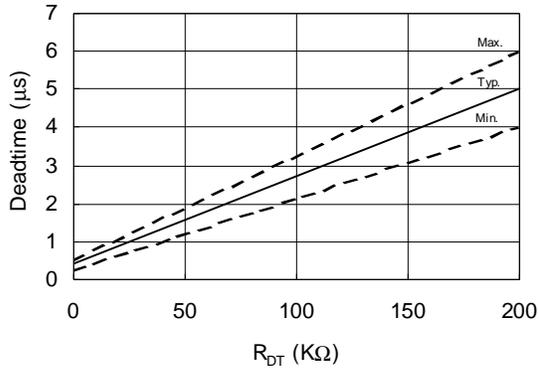
Figure 11C. Deadtime vs. R$_{DT}$
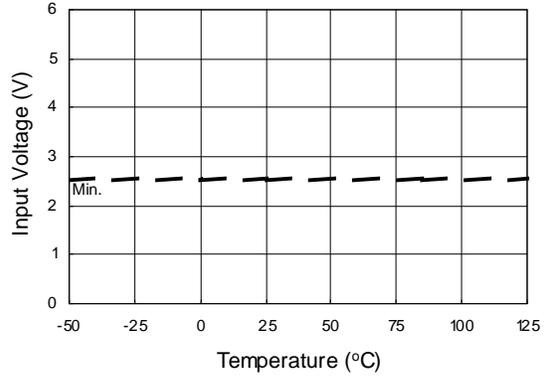
Figure 12A. Logic "1" Input Voltage vs. Temperature
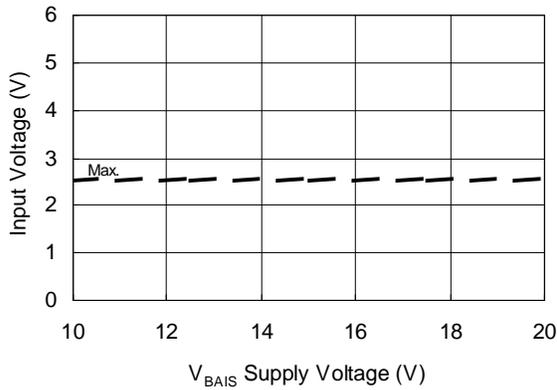
Figure 12B. Logic "1" Input Voltage vs. Supply Voltage
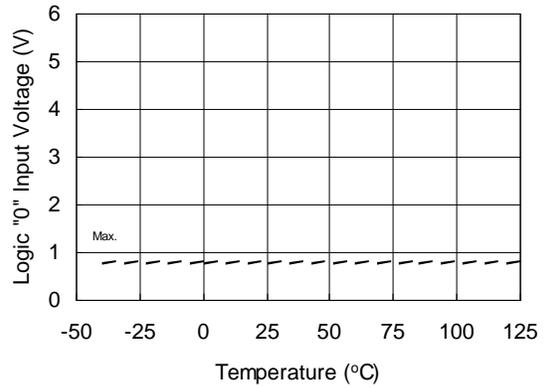
Figure 13A. Logic "0" Input Voltage vs. Temperature
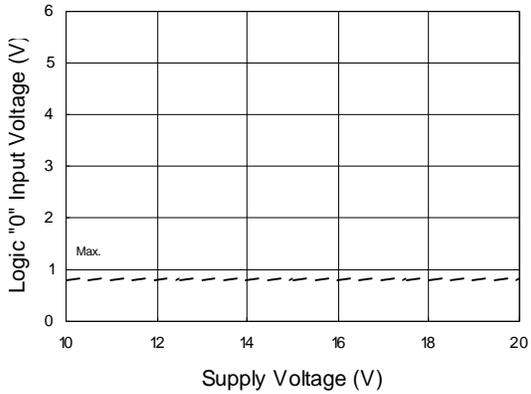
**Figure 13B. Logic "0" Input Voltage
vs. Supply Voltage**
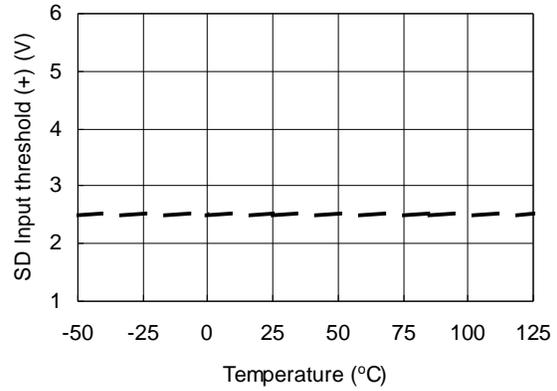
**Figure 14A. SD input positive going threshold (+)
vs. Temperature**
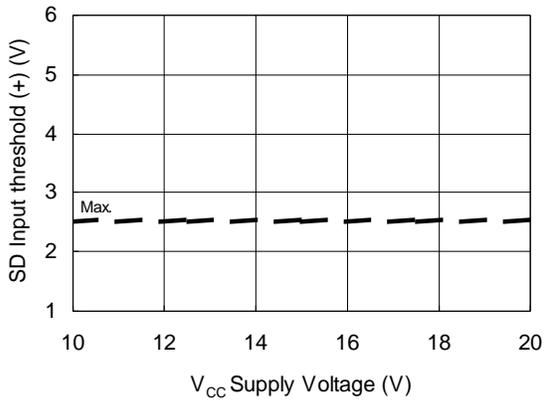
**Figure 14B. SD input positive going threshold (+)
vs. Supply Voltage**
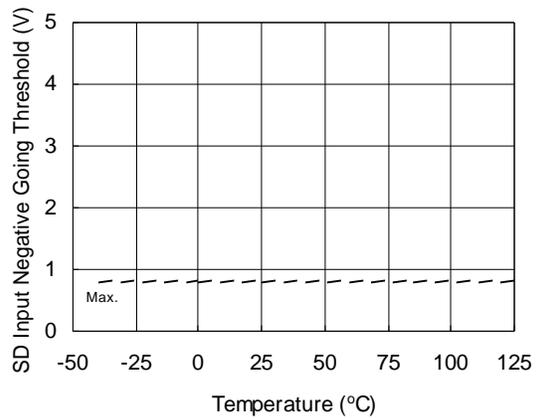
**Figure 15A. SD Input Negative Going
Threshold vs. Temperature**
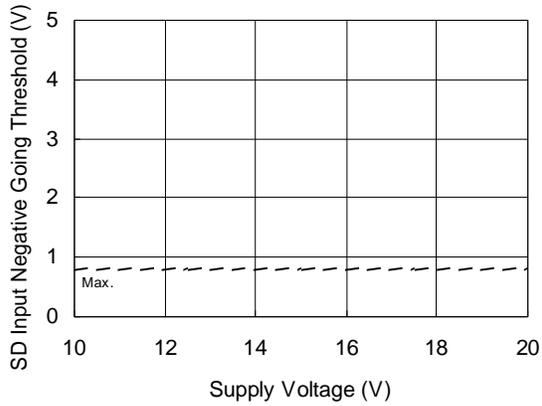
Figure 15B. SD Input Negative Going Threshold
vs. Supply Voltage
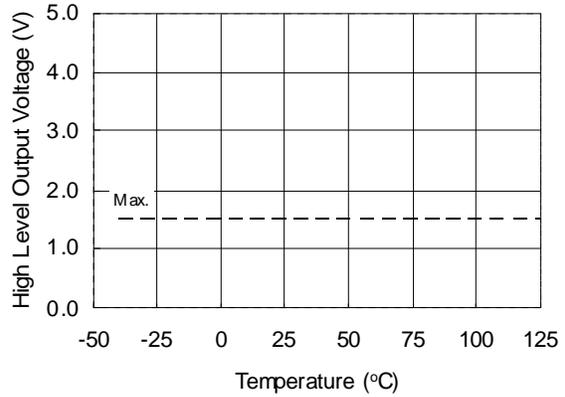
Figure 16A. High Level Output Voltage
vs. Temperature (I_O = 0 mA)
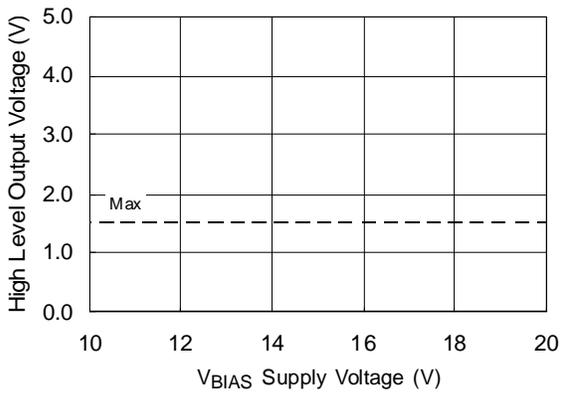
Figure 16B. High Level Output Voltage
vs. Supply Voltage (I_O = 0 mA)
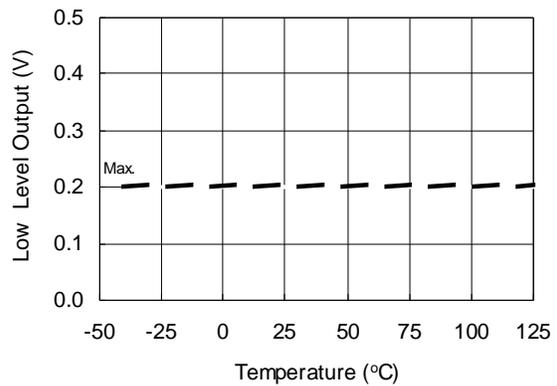
Figure 17A. Low Level Output vs. Temperature

IRS2184/IRS21844(S)PbF
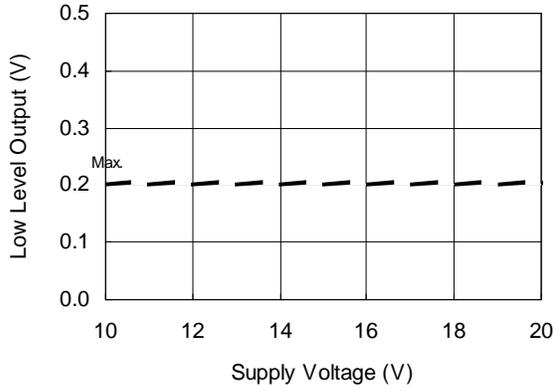
Figure 17B. Low Level Output vs. Supply Voltage
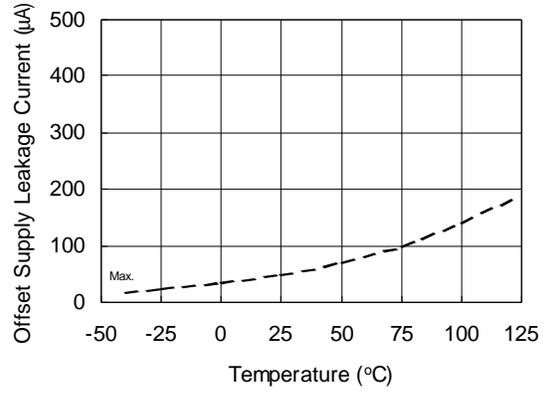
Figure 18A. Offset Supply Leakage Current vs. Temperature
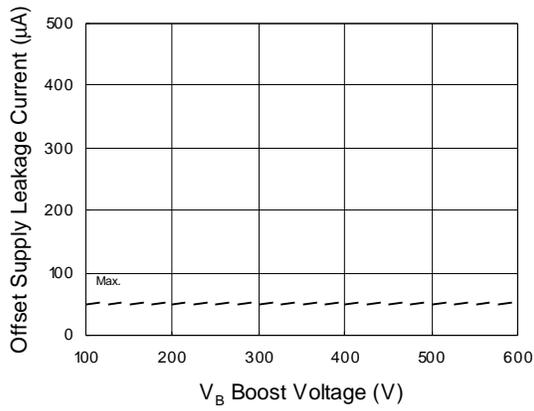
Figure 18B. Offset Supply Leakage Current vs. V_B Boost Voltage
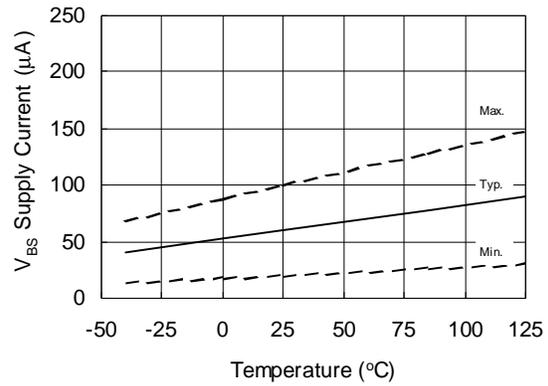
Figure 19A. V_{BS} Supply Current vs. Temperature

IRS2184/IRS21844(S)PbF
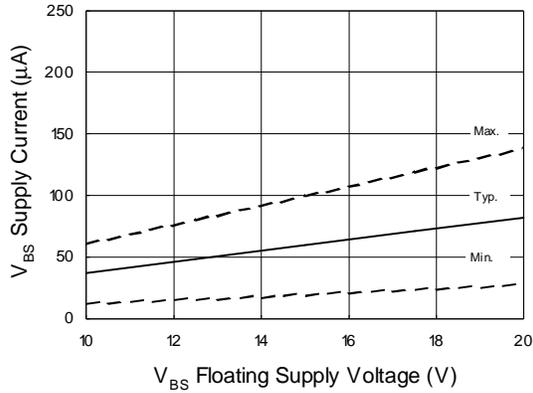
Figure 19B. V$_{BS}$ Supply Current vs. V$_{BS}$ Floating Supply Voltage
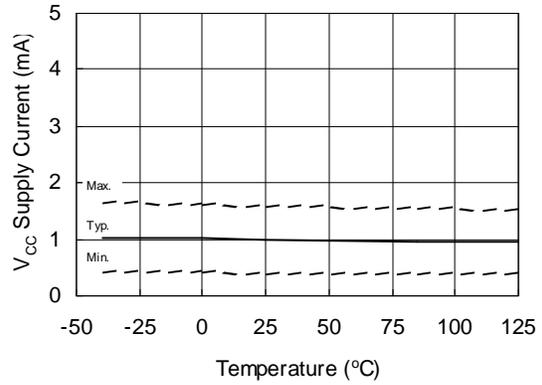
Figure 20A. V$_{CC}$ Supply Current vs. Temperature
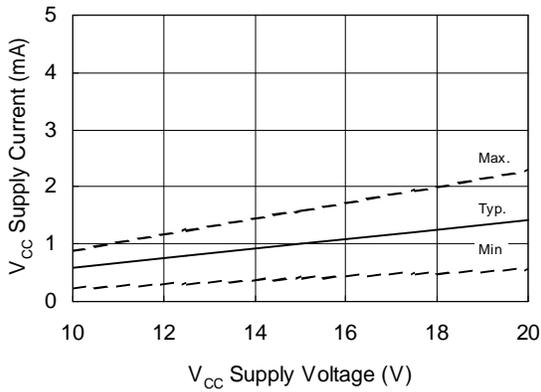
Figure 20B. V$_{CC}$ Supply Current vs. V$_{CC}$ Supply Voltage
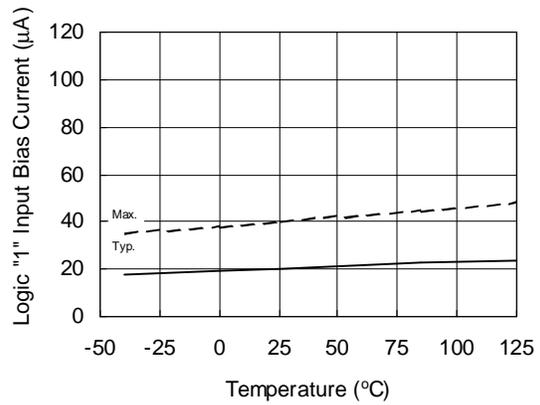
**Figure 21A. Logic "1" Input Bias Current vs. Temperature**
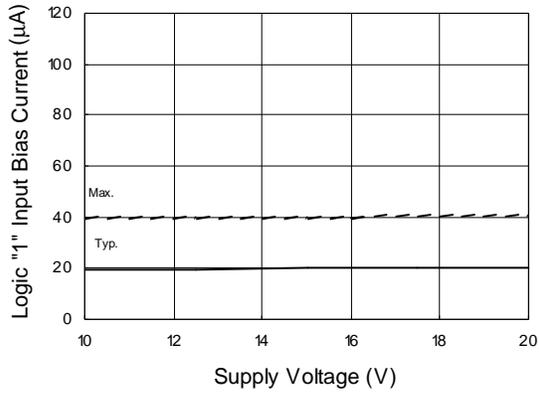
Figure 21B. Logic "1" Input Bias Current vs. Supply Voltage
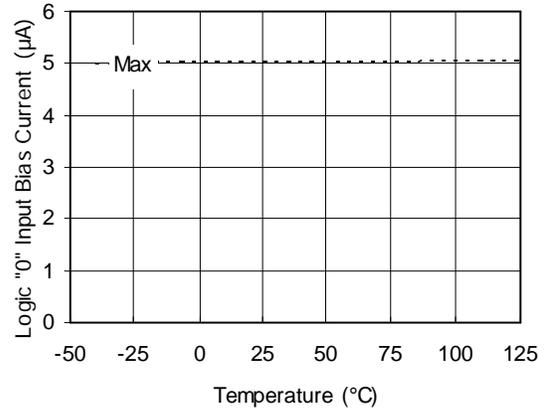
Figure 22A. Logic "0" Input Bias Curremt vs. Temperature
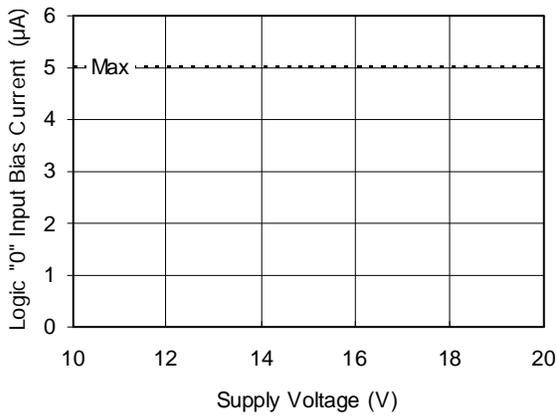
Figure 22B. Logic "0" Input Bias Curremt vs. Voltage
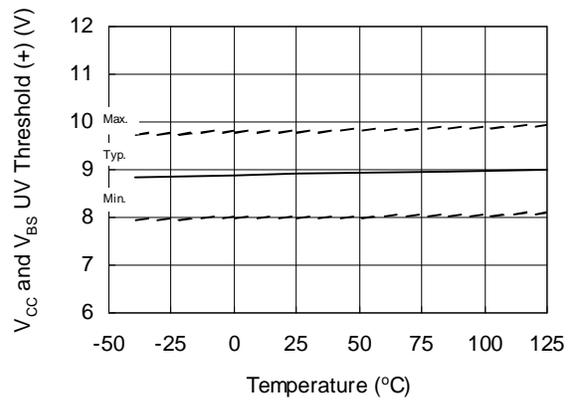
Figure 23. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature
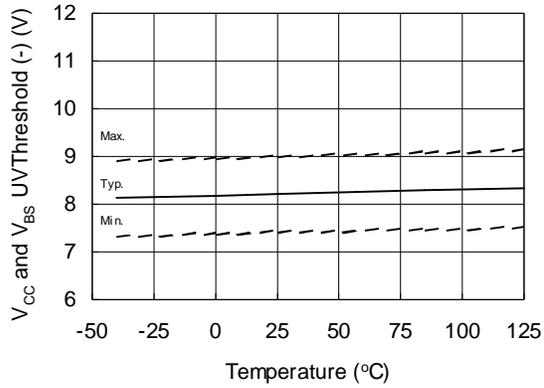
Figure 24. V_{CC} and V_{BS} Undervoltage Threshold (-)
vs. Temperature
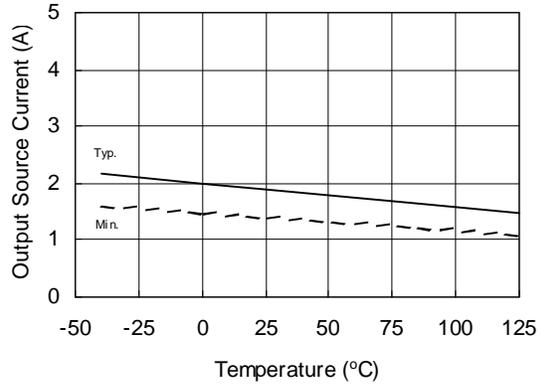
Figure 25A. Output Source Current
vs. Temperature
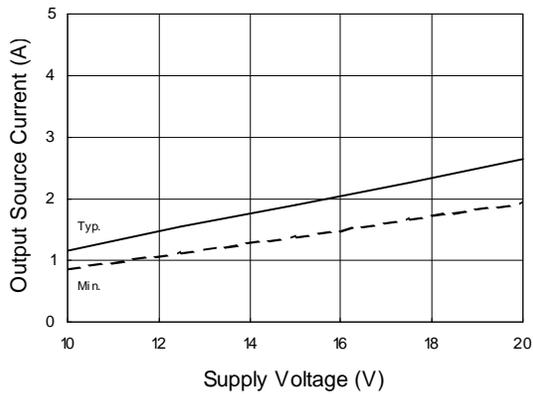
Figure 25B. Output Source Current
vs. Supply Voltage
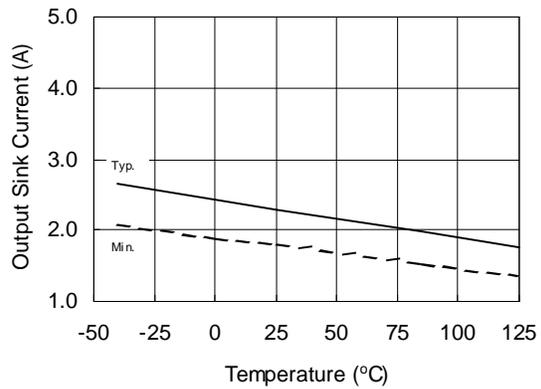
Figure 26A. Output Sink Current
vs. Temperature

IRS2184/IRS21844(S)PbF
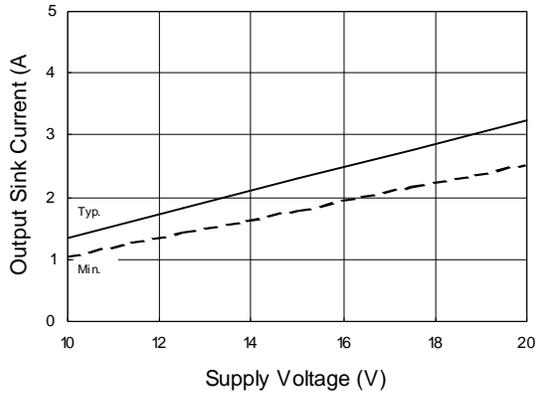
**Figure 26B. Output Sink Current
vs. Supply Voltage**
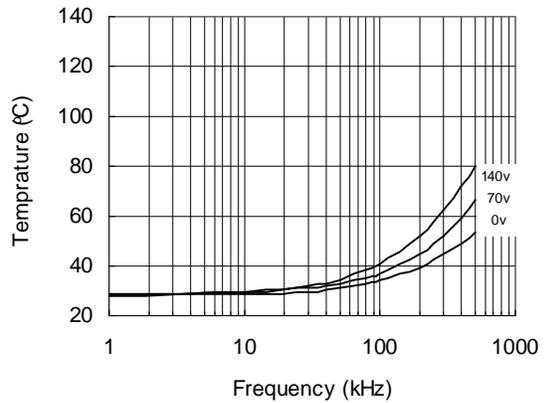
**Figure 27. IRS2181 vs. Frequency (IRFBC20),
R_{gate}=33 Ω, V_{CC}=15 V**
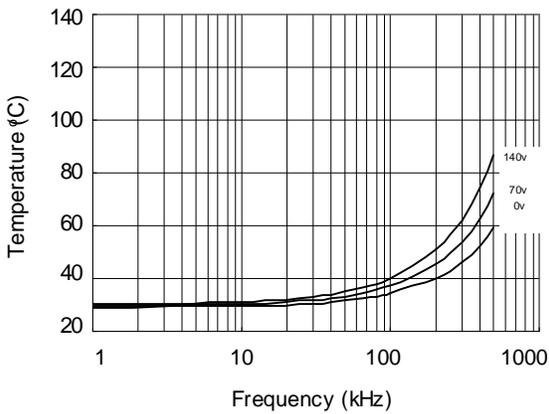
**Figure 28. IRS2181 vs. Frequency (IRFBC30),
R_{gate}=22 Ω, V_{CC}=15 V**
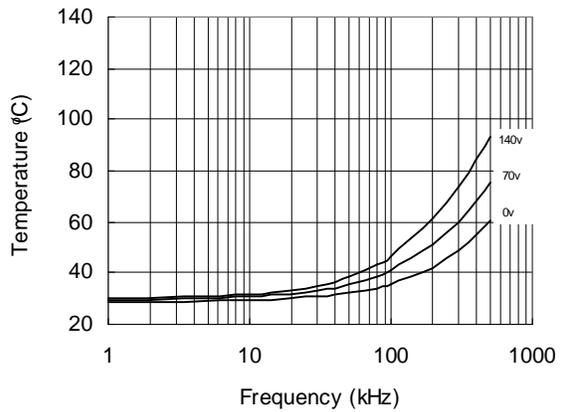
**Figure 29. IRS2181 vs. Frequency (IRFBC40),
R_{gate}=15 Ω, V_{CC}=15 V**
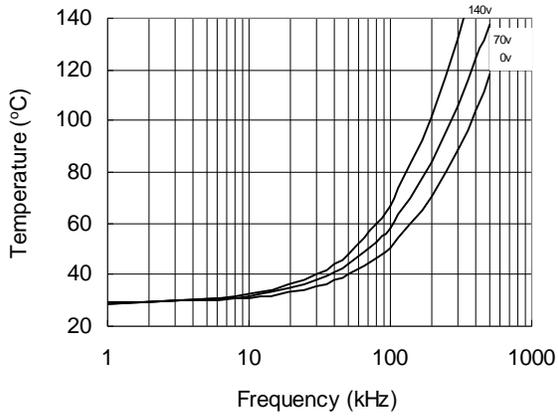
Figure 30. IRS2181 vs. Frequency (IRFPE50), R$_{gate}$=10 W, V$_{CC}$=15 V
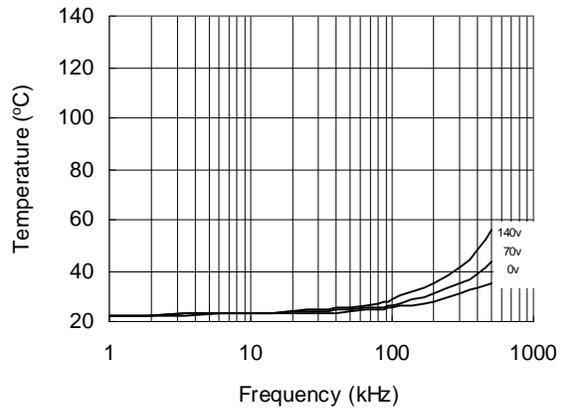
Figure 31. IRS21814 vs. Frequency (IRFBC20), R$_{gate}$=33 W, V$_{CC}$=15 V
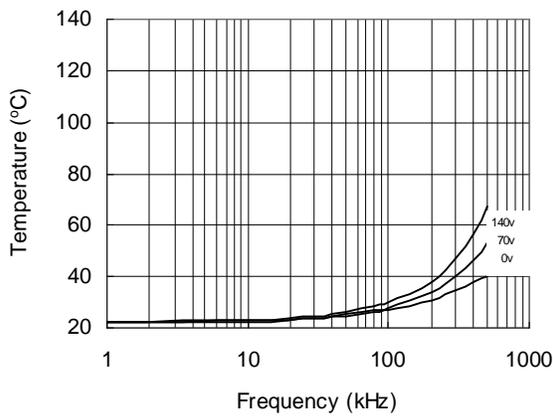
Figure 32. IRS21814 vs. Frequency (IRFBC30), R$_{gate}$=22 W, V$_{CC}$=15 V
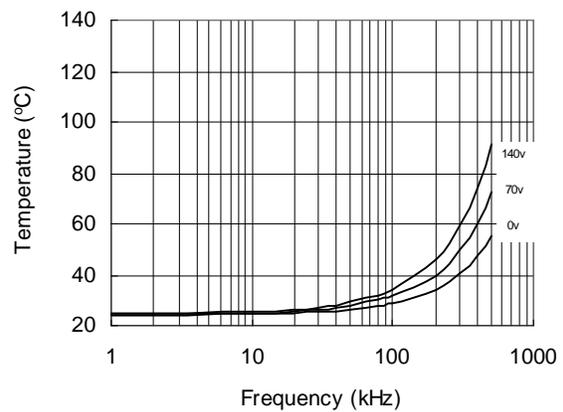
Figure 33. IRS21814 vs. Frequency (IRFBC40), R$_{gate}$=15 W, V$_{CC}$=15 V
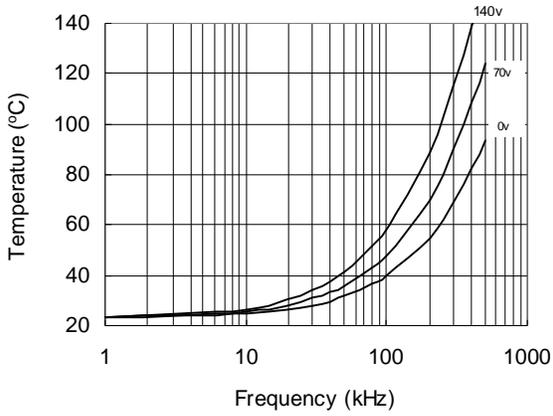
Figure 34. IRS21814 vs. Frequency (IRFPE50),
R$_{gate}$=10 W, V$_{CC}$=15 V
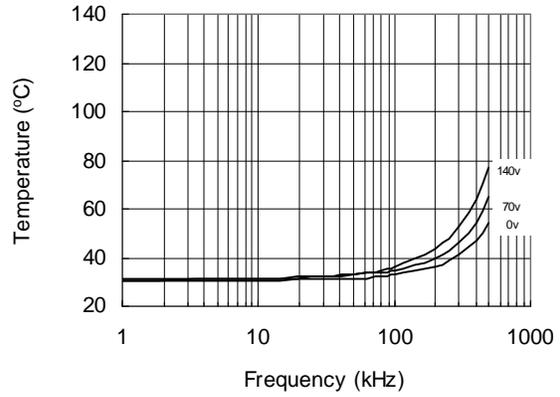
Figure 35. IRS2181s vs. Frequency (IRFBC20),
R$_{gate}$=33 W, V$_{CC}$=15 V
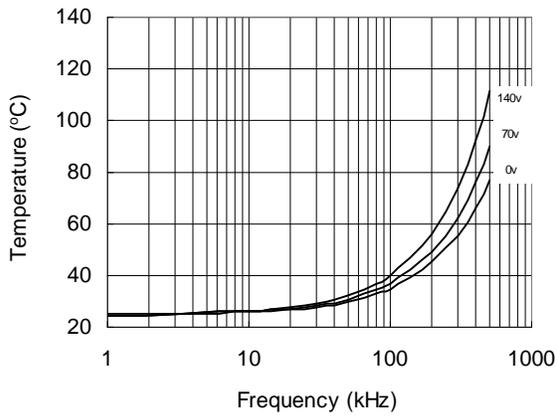
Figure 36. IRS2181s vs. Frequency (IRFBC30),
R$_{gate}$=22 W, V$_{CC}$=15 V
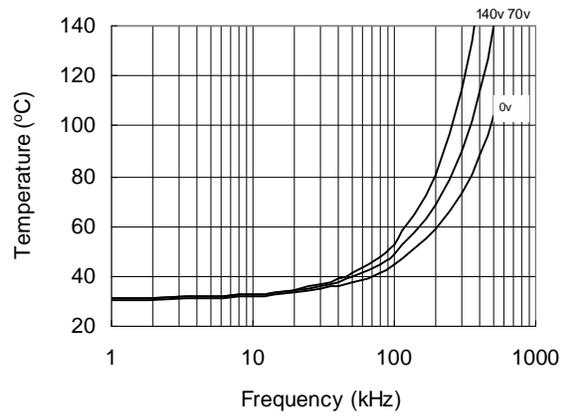
Figure 37. IRS2181s vs. Frequency (IRFBC40),
R$_{gate}$=15 W, V$_{CC}$=15 V
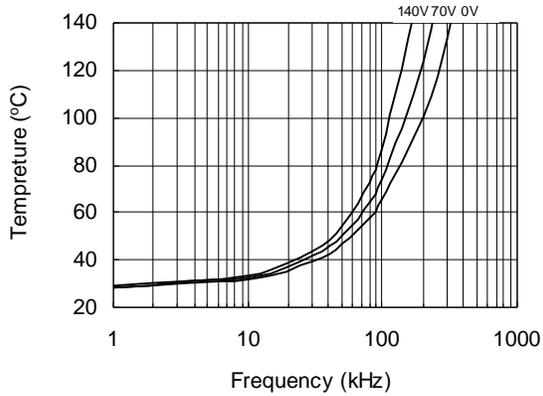
Figure 38. IRS2181s vs. Frequency (IRFPE50), R_{gate}=10 W, V_{CC}=15 V
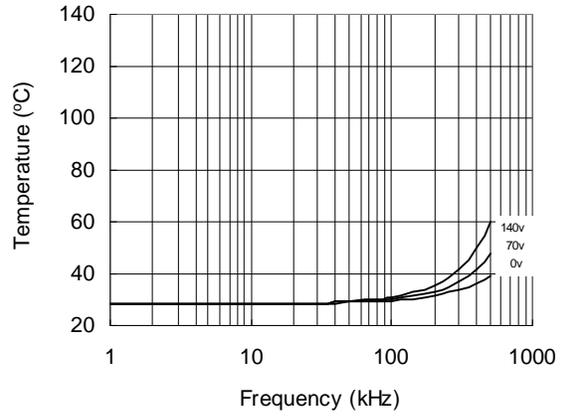
Figure 39. IRS21814s vs. Frequency (IRFBC20), R_{gate}=33 W, V_{CC}=15 V
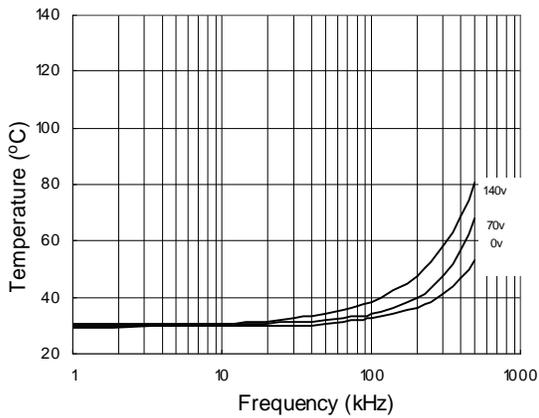
Figure 40. IRS21814s vs. Frequency (IRFBC30), R_{gate}=22 W, V_{CC}=15 V


Figure 41. IRS21814s vs. Frequency (IRFBC40), R_{gate}=15 W, V_{CC}=15 V

**Figure 42. IRS21814s vs. Frequency (IRFPE50),
R_{gate}=10 Ω, V_{CC}=15 V**

International
I⚙R Rectifier

IRS2184/IRS21844(S)PbF

Cast Outlines

8-Lead PDIP

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS−001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

01-6014
01-3003 01 (MS-001AB)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS−001AC.
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

20.19 [.795]
18.42 [.725]

7.11 [.280]
6.10 [.240]

14X 1.77 [.070]
1.15 [.045]

0.39 [.015]
MIN.

5.33 [.210]
MAX

4.06 [.160]
2.93 [.115]

14X 0.558 [.022]
0.356 [.014]

2.54 [.100]
12X

14X 0° − 15°

7.62 [.300]

14X 0.381 [.015]
0.204 [.008]

⊕ 0.25 [.010] Ⓜ C B Ⓢ A Ⓢ

14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS−012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

8.74 [.344]
8.56 [.337]

3.99 [.157]
3.81 [.150]

6.20 [.2440]
5.80 [.2284]

⊕ 0.25 [.010] Ⓜ C B Ⓜ

0.25 [.0098]
0.10 [.0040]

1.27 [.050]
12X

0.46 [.018]
0.36 [.014] 14X

⊕ 0.25 [.010] Ⓜ C B Ⓢ A Ⓢ

0.48 [.019]
0.28 [.011] X 45°

0° − 8°

1.75 [.0688]
1.35 [.0532]

1.27 [.050]
0.41 [.016]

0.25 [.0098]
0.19 [.0075] 14X

14X

14-Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

**Tape & Reel
8-lead SOIC**

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM

CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062
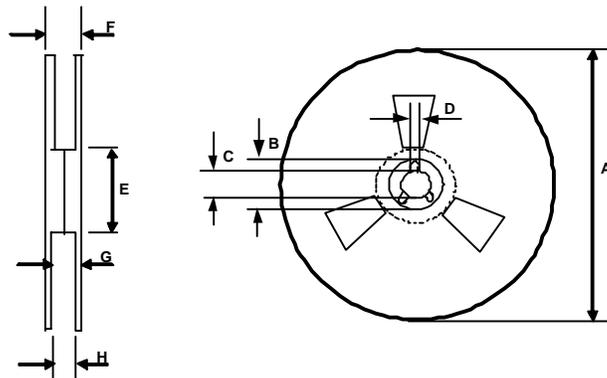
REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

IRS2184/IRS21844(S)PbF

**Tape & Reel
14-lead SOIC**

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM
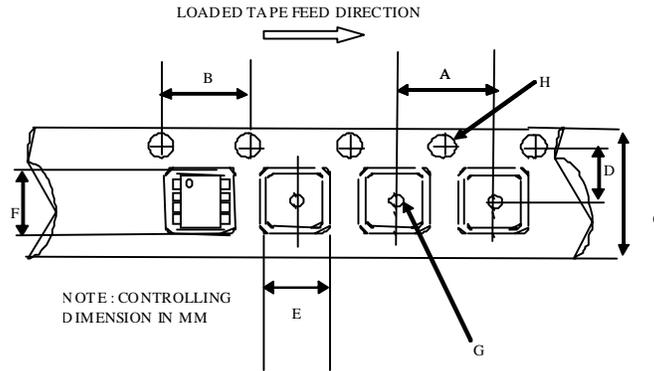
CARRIER TAPE DIMENSION FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062
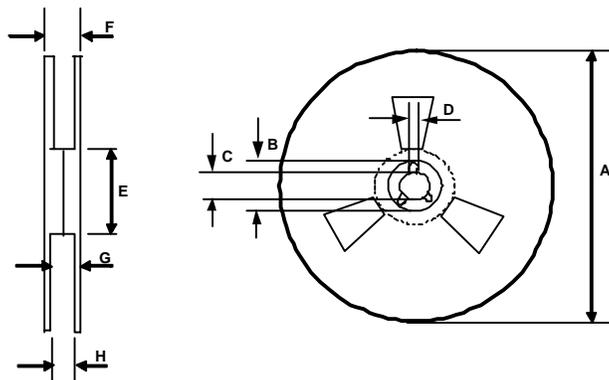
REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

www.irf.com

25

LEADFREE PART MARKING INFORMATION

Part number —— IRSxxxxx

Date code —— YWW?

IR logo

Pin 1 Identifier ●

?XXXX

?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Lot Code
(Prod mode - 4 digit SPN code)

Assembly site code
Per SCOP 200-002
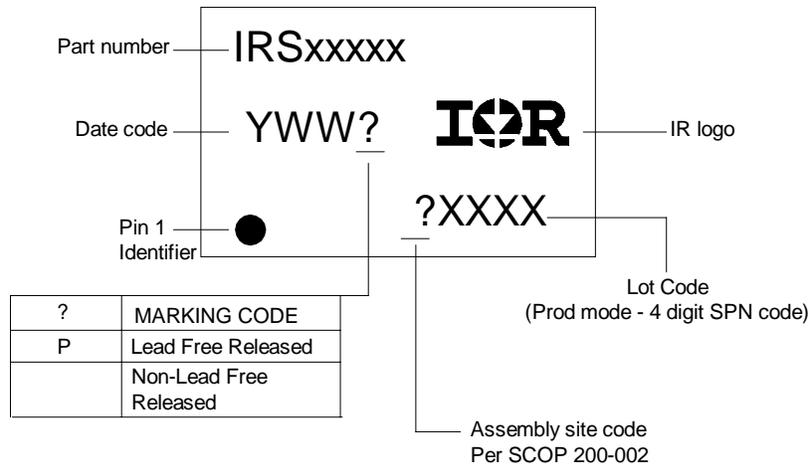
ORDER INFORMATION

8-Lead PDIP IRS2184PbF
8-Lead SOIC IRS2184SPbF
8-Lead SOIC Tape & Reel IRS2184STRPbF

14-Lead PDIP IR2S1844PbF
14-Lead SOIC IRS21844SPbF
14-Lead SOIC Tape & Reel IRS21844STRPbF

International **IOR** Rectifier