

Quad Precision, Low Cost, High Speed, BiFET Op Amp

AD713

FEATURES

Enhanced Replacement for LF347 and TL084

AC PERFORMANCE

1 ms Settling to 0.01% for 10 V Step 20 V/ms Slew Rate 0.0003% Total Harmonic Distortion (THD) 4 MHz Unity Gain Bandwidth

DC PERFORMANCE

0.5 mV max Offset Voltage (AD713K) 20 mV/°C max Drift (AD713K) 200 V/mV min Open Loop Gain (AD713K) 2 mV p-p typ Noise, 0.1 Hz to 10 Hz True 14-Bit Accuracy Single Version: AD711, Dual Version: AD712 Available in 16-Pin SOIC, 14-Pin Plastic DIP and Hermetic Cerdip Packages Standard Military Drawing Available

APPLICATIONS Active Filters Quad Output Buffers for 12- and 14-Bit DACs Input Buffers for Precision ADCs Photo Diode Preamplifier Application

PRODUCT DESCRIPTION

The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single-pole response of the AD713 provides fast settling: l μ s to 0.01%. This feature, combined with its high dc precision, makes the AD713 suitable for use as a buffer amplifier for 12or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713's low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD713 is internally compensated for stable operation at unity gain and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0°C to 70°C. The AD713A and AD713B are rated over the industrial temperature of -40° C to $+85^{\circ}$ C. The AD713S and AD713T are rated over the military temperature range of -55° C to $+125^{\circ}$ C and are available processed to standard microcircuit drawings.

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

CONNECTION DIAGRAMS



The AD713 is offered in a 16-pin SOIC, 14-pin plastic DIP and hermetic cerdip package.

PRODUCT HIGHLIGHTS

- 1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074, TL084, LT1058, LF347 and OPA404.
- 2. Slew rate is 100% tested for a guaranteed minimum of 16 V/ μ s (J, A and S Grades).
- 3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
- 4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

AD713—SPECIFICATIONS ($V_s = \pm 15 V @ T_A = 25^{\circ}C$ unless otherwise noted)

		AD713I/A/S		AD713K/B/T				
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
INPUT OFFSET VOLTAGE ¹ Initial Offset Offset vs. Temp vs. Supply	${ m T_{MIN}}$ to ${ m T_{MAX}}$ ${ m T_{MIN}}$ to ${ m T_{MAX}}$	7 8 76/76/ 76	0.3 0.5 5 95 95	1.5 2/2/2	84 84	0.2 0.4 5 100 100	0.5 0.7/0.7/1.0 20/20/15	mV mV μV/°C dB dB
INDUT DIAS CUDDENIT ²	V = 0 V		10	150		10	75	μν/πιοπιπ
INPUT BIAS CORRENT-	$V_{CM} = 0 V$ $V_{CM} = 0 V @ T_{MAX}$ $V_{CM} = \pm 10 V$		40 55	3.4/9.6/154 200		40 55	/5 1.7/4.8/77 120	pA nA pA
INPUT OFFSET CURRENT	$V_{CM} = 0 V$ $V_{CM} = 0 V @ T_{MAX}$		10	75 1.7/4.8/77		10	35 0.8/2.2/36	pA nA
MATCHING CHARACTERISTICS Input Offset Voltage Input Offset Voltage Drift Input Bias Current Crosstalk	T_{MIN} to T_{MAX} f = 1 kHz f = 100 kHz		0.5 0.7 8 10	1.8 2.3/2.3/2.3 100 -130 -95		0.4 0.6 6 10	0.8 1.0/1.0/1.3 25 35 -130 -95	mV mV μV/°C pA dB dB
FREQUENCY RESPONSE Small Signal Bandwidth Full Power Response Slew Rate Settling Time to 0.01% Total Harmonic Distortion	Unity Gain $V_0 = 20 V p-p$ Unity Gain $f = 1 kHz; R_L \ge 2 k\Omega;$ $V_0 = 3 V rms$	3.0 16	4.0 200 20 1.0 0.0003	1.2	3.4 18	4.0 200 20 1.0 0.0003	1.2	MHz kHz V/µs µs %
INPUT IMPEDANCE Differential Common Mode			3×10 ¹² ∥5.5 3×10 ¹² ∥5.5			3×10 ¹² ∥5.5 3×10 ¹² ∥5.5		Ω∥pF Ω∥pF
INPUT VOLTAGE RANGE Differential ³ Common-Mode Voltage ⁴ Common Mode Rejection Ratio	$T_{MIN} \text{ to } T_{MAX}$ $V_{CM} = \pm 10 \text{ V}$ $T_{MIN} \text{ to } T_{MAX}$ $V_{CM} = \pm 11 \text{ V}$	-11 78 76/76/76 72	±20 +14.5, -11.5 88 84 84	+13	-11 84 82 78	±20 +14.5, -11.5 94 90 90	+13	V V dB dB dB
INPUT VOLTAGE NOISE	$T_{MIN} \text{ to } T_{MAX}$ 0.1 Hz to 10 Hz $f = 10 \text{ Hz}$ $f = 100 \text{ Hz}$	70/70/70	80 2 45 22		74	84 2 45 22		
	f = 1 kHz f = 10 kHz		18 16			18 16		nV/\sqrt{Hz} nV/\sqrt{Hz}
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01		pA/\sqrt{Hz}
OPEN-LOOP GAIN	$V_0 = \pm 10 \text{ V}; \text{R}_L \ge 2 \text{k}\Omega$ T_{MIN} to T_{MAX}	150 100/100/ 100	400		200 100	400		V/mV V/mV
OUTPUT CHARACTERISTICS Voltage Current	$R_L \ge 2 k\Omega$ T_{MIN} to T_{MAX} Short Circuit	+13, -12.5 ±12/±12/ ±12	+13.9, -13.3 +13.8, -13.1 25		+13, -12.5 ±12	+13.9, -13.3 +13.8, -13.1 25		V V mA
POWER SUPPLY								
Rated Performance Operating Range Quiescent Current		±4.5	±15 10.0	±18 13.5	±4.5	±15 10.0	±18 12.0	V V mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES

¹Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = 25^{\circ}C$.

²Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = 25^{\circ}$ C. For higher temperatures, the current doubles every 10°C.

³Defined as voltage between inputs, such that neither exceeds ± 10 V from ground. ⁴Typically exceeding -14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

AD713

ABSOLUTE MAXIMUM RATINGS^{1, 2}

Supply Voltage
Internal Power Dissipation ²
Input Voltage ³ ±18 V
Output Short-Circuit Duration
(For One Amplifier) Indefinite
Differential Input Voltage $\dots + V_S$ and $-V_S$
Storage Temperature Range (Q)65°C to +150°C
Storage Temperature Range (N, R) $\dots -65^{\circ}$ C to $+125^{\circ}$ C
Operating Temperature Range
AD713J/K 0°C to 70°C
AD713A/B40°C to +85°C
AD713S/T
Lead Temperature Range (Soldering 60 sec) $\ldots \ldots 300^{\circ}C$

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Thermal Characteristics:

14-Pin Plastic Package:	$\theta_{IC} = 30^{\circ}C/Watt; \theta_{IA} = 100^{\circ}C$	/Watt
14-Pin Cerdip Package:	$\theta_{IC} = 30^{\circ}C/Watt; \theta_{IA} = 110^{\circ}C$	C/Watt
	16-Pin SOIC Package:	$\theta_{\rm IC} = 30^{\circ} {\rm C}/$

Watt; $\theta_{JA} = 100^{\circ}C/Watt$

 3 For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

	Temperature	Package	Package
Model	Range	Description	Option ¹
AD713AQ	-40° C to $+85^{\circ}$ C	14-Pin Ceramic DIP	Q-14
AD713BQ	-40° C to $+85^{\circ}$ C	14-Pin Ceramic DIP	Q-14
AD713JN	0°C to 70°C	14-Pin Plastic DIP	N-14
AD713JR-16	0°C to 70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL	0°C to 70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL7	0°C to 70°C	16-Pin Plastic SOIC	R-16
AD713KN	0°C to 70°C	14-Pin Plastic DIP	N-14
AD713SQ ²	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ ²	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063301MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063302MCA ²	–55°C to +125°C	14-Pin Ceramic DIP	O-14

¹N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).

²Not for new designs. Obsolete April 2002.

CAUTION_

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD713 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Pin Plastic (N-14A) DIP Package

14-Pin Cerdip (Q-14) Package

16-Pin SOIC (R-16) Package







0.0125 (0.32)